QuickSwitch® Products
Analysis of QuickSwitch® Behavior in Four Operating Regions

Abstract

In this Technical Note, we examine in detail the basics and behavior of an N-FET QuickSwitch in the following operating regions of an input signal to the switch as shown in Figure 1.

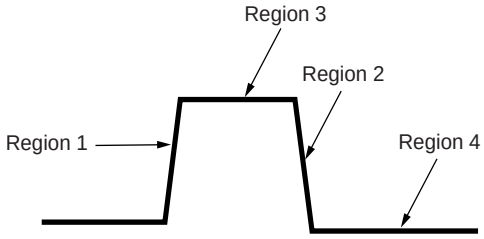

Figure 1. Regions of Operation for QuickSwitch Input Signal

A. Region 1: 'ON' State - Input LOW to HIGH transition
B. Region 2: 'ON' State - Input HIGH to LOW transition
C. Region 3: 'ON' State - Input at Steady-State 'HIGH'
D. Region 4: 'ON' State - Input at Steady-State 'LOW'

At the end, we briefly examine the condition at which the switch turns 'OFF' for the steady-state 'HIGH', Region 3. In addition, the switch impedance characteristics for logic high and low inputs are described and voltage translation feature is clarified.

QuickSwitch Basics

Figure 2 shows a typical QuickSwitch implementation using an NMOS enhancement mode transistor as a switch driven by an active Low enable signal through a CMOS inverter. A logic low on the enable input connects the V_{CC} to the gate of the Enhanced CMOS N-FET transistor. We need to emphasize that the QuickSwitch is bidirectional, therefore, we can call the V_{IN} and V_{OUT} voltages, I/O voltages. The output of a QuickSwitch is normally connected to input of a CMOS logic circuit. Let's call the input gate capacitance of such input C_L. The bias applied to the transistor determines which terminal acts as the drain and which terminal acts as the source. If the gate voltage V_g is zero, then the n-channel transistor is cut off and the output is isolated from the input.

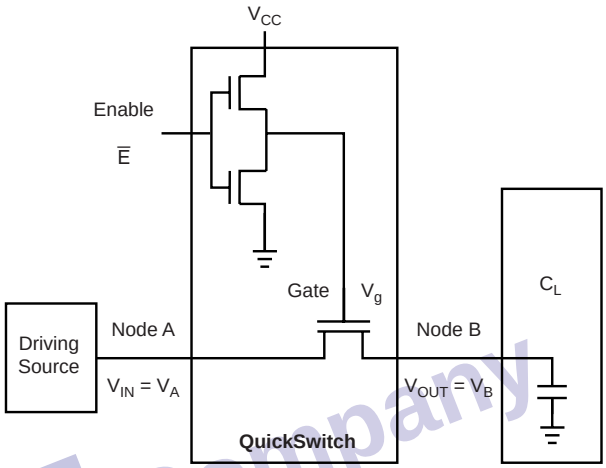

Figure 2. Basic QuickSwitch Schematic

Switch Remains ON: Logic LOW to HIGH Transition (Region 1)

Since the switch is ON, we have: $V_g = V_{CC}$. For Logic LOW to HIGH transition, V_{IN} rises from LOW to HIGH. V_{OUT} is initially zero, then Node A acts as drain since it is connected to a rising edge high voltage, and Node B acts as the source since it is following node A and is charging the capacitor C_L. Current enters the drain from the input, charging the capacitor C_L. The gate to source voltage is

$$VGS = V_g - V_B = V_{CC} - V_{OUT}$$

As the capacitor charges and V_{OUT} increases (V_{OUT} follows V_{IN} closely), the gate to source voltage decreases. The capacitor stops charging when the current goes to zero. This occurs when the gate-to-source voltage VGS becomes equal to the threshold voltage V_t. The maximum output voltage occurs when $VGS = V_t$; therefore:

$$VGS\ (Min.) = V_t = V_{CC} - V_{OUT}\ (Max.)$$
or
$$V_{OUT}\ (Max.) = V_{CC} - V_t$$

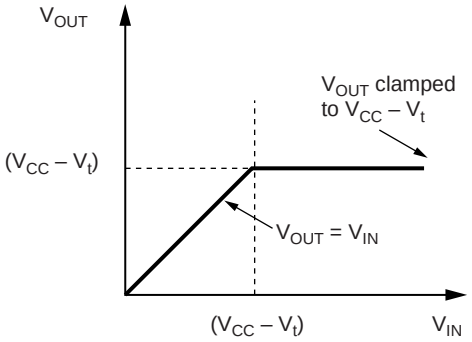

Figure 3. Transfer Characteristic of the QuickSwitch

When $V_{IN} = V_A$ and is below $V_{CC} - V_t$, where V_t is the n-transistor effective threshold voltage, typically 1V, then V_{OUT} is equal to V_{IN}. V_{OUT} and V_{IN} are connected via the resistance (R_{ON}) of the QuickSwitch. The value of this resistance is determined by the lower of the voltages at the nodes. When V_{IN} rises above V_{CC}-V_t, the output voltage stops following the input and remains clamped at a value $V_{CC} - V_t$, i.e. V_{CC} –1 as shown in Figure 3. This voltage clamping feature is useful for voltage translation applications.

Region 1 V-I Characteristics

Now let us examine the behavior of the current through the switch as C_L charges. Figure 4 shows the V-I characteristics. With the help of Figure 4 we can examine the current behavior.

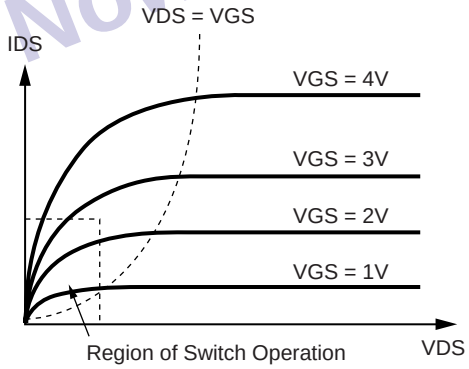

Figure 4. QuickSwitch V-I Characteristics

As C_L charges, VGS decreases and the current through the switch decreases (approaches zero). See Figure 5. This fact basically explains that as VGS decreases the switch ON resistance (R_{ON}) increases since the switch is operating in the linear region. Since the current through the switch is negligible, the voltage drop across the switch is very close to zero, even though the ON resistance increases.

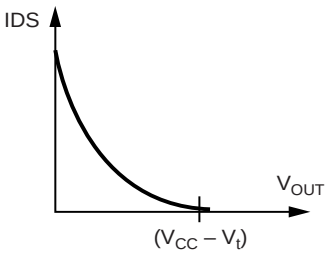

Figure 5. Load Capacitance Charging Current

One of the quantities implied in the drain curves, as shown in Figure 6, is the AC drain resistance, which is defined as:

$$Rds = dVDS/dIDS$$

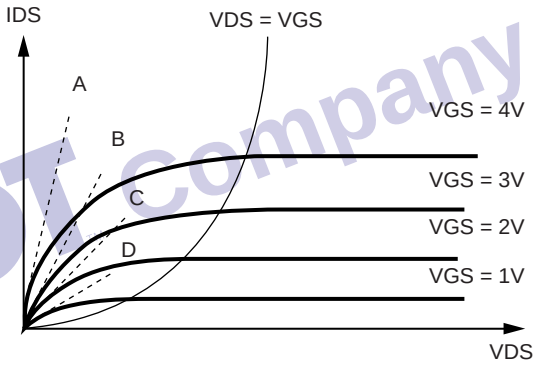

Figure 6: The Change in Slope of Each Curve at its Ohmic Region Represents the Drain Resistance

Where Rds is the derivative of the drain curve at the operating point. As the Figure 6 shows the slope of drain curves decreases as VGS decreases. This slope represents R_{ON} = Rds. Figure 7 shows the locus of R_{ON} for various values of VGS, which in turn, corresponds to different values of V_{IN} (~V_{OUT}).

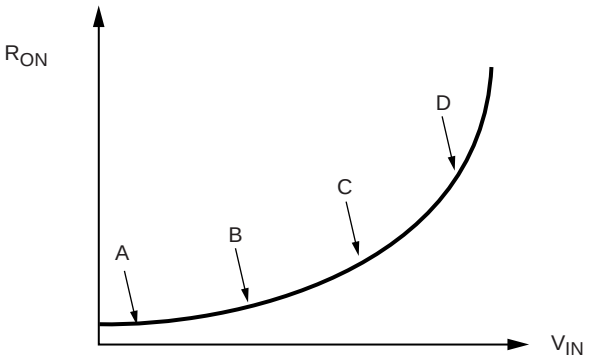

Figure 7. Switch Resistance vs. Input Voltage

Switch Remains ON: Logic HIGH to LOW Transition, Region 2

Now consider a situation where the output is high initially ($V_{OUT} = V_{CC}-V_t$), the switch is on ($V_g = V_{CC}$) and the input goes low . Node B with initial voltage of ($V_B = V_{CC} - V_t$) acts as Drain and Node A acts as Source (going from HIGH to LOW). The analysis of the switch in this region is very similar to Region 1. The gate to source voltage is:

$$VGS = V_g - V_A$$

As $V_A = V_{IN}$ makes the HIGH to LOW transition, C_L discharges through the switch and V_{OUT} follows V_{IN}. As V_A decreases, VGS starts increasing.

As Figure 4. Shows, as VGS increases the value of current through the switch increases. And finally the capacitor discharges completely and V_{OUT} reaches zero. VGS is now a constant at V_{CC}, the drain current goes to zero when the drain to source voltage is zero, which means that the capacitor has completely discharged to zero. As shown, the logic zero is transmitted unattenuated through the switch.

Switch Remains ON: Region 3 and Region 4

In these two regions, we consider the switch in its steady state. Analysis of these two regions should give the reader an insight into drive capability of the device in the two logic states.

Logic High Output, Region 3:

In this case the input is stable at V_{CC}, the switch is ON. The steady state output voltage of the transistor is basically function of input impedance of the device being fed by the QuickSwitch. The switch operates in the “source follower” mode . The V/I characteristic is shown in Figure 8.

Logic Low Output, Region 4:

When the input (Node A) is at steady state logic Low, the transistor operates in the “common source” configuration with VGS = V_{CC}. The V/I characteristic is shown in Figure 9.

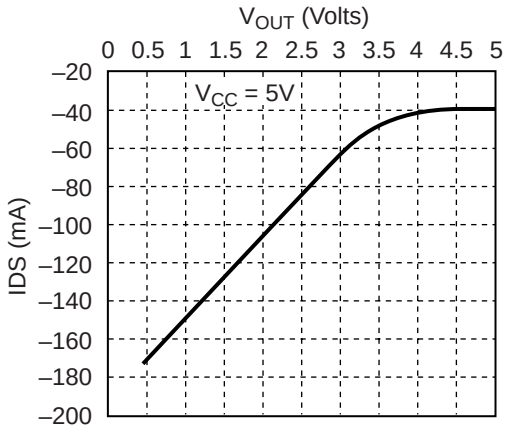

Figure 8. Logic High V/I Characteristic

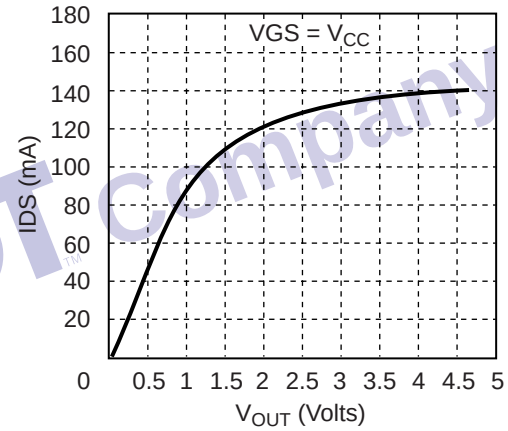

Figure 9. Logic Low V/I Characteristics for Output

Switch Turns OFF

When V_g goes to low and VGS << V_t, the NMOS device turns off and the input and output become isolated. The impedance between the two I/O nodes of the switch is very high and is in order of few MΩ. For the normal voltage range of 0 to V_{CC} at the I/O terminals, the switch maintains high impedance, however, large negative undershoots of greater than 1V magnitude can turn the switch ON, and should be avoided.