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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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R8C/25 Group
Timer RE in Output Compare Mode

1. Abstract
   This document describes how to set up and use timer RE in output compare mode in the R8C/25 Group.

2. Introduction
   The application example described in this document is applied to the following MCU and parameter(s):
   
   • MCU: R8C/25 Group
   • XIN clock: 20 MHz
   
   This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.
3. Descriptions of Applications

3.1 Timer RE

Timer RE has 4-bit and 8-bit counters. Timer RE has the following two modes:

- **Real-time clock mode** Generate a 1-second signal from \( fc4 \) and counts seconds, minutes, hours, and days of the week.
- **Output compare mode** Count a count source and detect compare matches.

3.2 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and the compare value match is detected with the 8-bit counter. Figure 3.1 shows a Block Diagram of Output Compare Mode and Table 3.1 lists the Output Compare Mode Specifications. Figures 3.2 to 3.6 show the Registers Associated with Output Compare Mode, and Figure 3.7 shows the Operation in Output Compare Mode.

---

**Figure 3.1** Block Diagram of Output Compare Mode

![Block Diagram of Output Compare Mode](image-url)
### Table 3.1 Output Compare Mode Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count sources</td>
<td>f4, f8, f32, fC4</td>
</tr>
</tbody>
</table>
| Count operations            | • increment  
  • When the 8-bit counter content matches the TREMIN register content, the value returns to 00h and the count continues. The count value is held while the count stops. |
| Count period                | • When RCS2 = 0 (4-bit counter is not used)  
  \[ \frac{1}{fi} \times 2 \times (n+1) \]  
  • When RCS2 = 1 (4-bit counter is used)  
  \[ \frac{1}{fi} \times 32 \times (n+1) \]  
  fi: Frequency of count source  
  n: Setting value of TREMIN register |
| Count start condition       | 1 (count starts) is written to the TSTART bit in the TRECR1 register. |
| Count stop condition        | 0 (count stops) is written to the TSTART bit in the TRECR1 register. |
| Interrupt request generation timing | When the 8-bit counter content matches the TREMIN register content. |
| TREO pin function           | Select any one of the following:  
  • Programmable I/O ports  
  • Output f2, f4, or f8  
  • Compare output |
| Read from timer             | When reading the TRESEC register, the 8-bit counter value can be read.  
When reading the TREMIN register, the compare value can be read. |
| Write to timer              | Writing to the TRESEC register is disabled.  
When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled. |
| Select functions            | • Select use of 4-bit counter  
  • Compare output function  
  Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. The output level is held by setting the TSTART bit to 0 (count stops). |
Timer RE Counter Data Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRESEC</td>
<td>0118h</td>
<td>00h</td>
<td>RW</td>
</tr>
</tbody>
</table>

8-bit counter data can be read.
Although timer RE stops counting, the count value is held.
The TRESEC register is set to 00h at compare match.

Figure 3.2 TRESEC Register in Output Compare Mode

Timer RE Compare Data Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TREMIN</td>
<td>0119h</td>
<td>00h</td>
<td>RW</td>
</tr>
</tbody>
</table>

8-bit compare data is stored.

Figure 3.3 TREMIN Register in Output Compare Mode
### Timer RE Control Register 1

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRECR1</td>
<td>011Ch</td>
<td>00h</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>After Reset 00h</td>
</tr>
</tbody>
</table>

#### Bit Symbols

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>(b7)</td>
<td>00</td>
<td>0</td>
<td>Nothing assigned. If necessary, set to 0. When read, the content is 0.</td>
<td>—</td>
</tr>
<tr>
<td>b6</td>
<td>TCSTF</td>
<td></td>
<td>0</td>
<td>Timer RE count status flag</td>
<td>RO</td>
</tr>
<tr>
<td>b5</td>
<td>TOENA</td>
<td></td>
<td>0</td>
<td>TREQ pin output enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b4</td>
<td>INT</td>
<td></td>
<td>0</td>
<td>Interrupt request timing bit</td>
<td>RW</td>
</tr>
<tr>
<td>b3</td>
<td>TRERST</td>
<td></td>
<td>0</td>
<td>Timer RE reset bit</td>
<td>RW</td>
</tr>
<tr>
<td>b2</td>
<td>PM</td>
<td></td>
<td>0</td>
<td>A.M./P.M. bit</td>
<td>RW</td>
</tr>
<tr>
<td>b1</td>
<td>H12_H24</td>
<td></td>
<td>0</td>
<td>Operating mode select bit</td>
<td>RW</td>
</tr>
<tr>
<td>b0</td>
<td>TSTART</td>
<td></td>
<td>0</td>
<td>Timer RE count start bit</td>
<td>RW</td>
</tr>
</tbody>
</table>

#### Function Descriptions

- **TRERST**: Timer RE reset bit
  - When setting this bit to 0, after setting it to 1, the following will occur.
  - Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h.
  - Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0.
  - The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.

**Figure 3.4** TRECR1 Register in Output Compare Mode

### Timer RE Control Register 2

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRECR2</td>
<td>011Dh</td>
<td>00h</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>After Reset 00h</td>
</tr>
</tbody>
</table>

#### Bit Symbols

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>(b7)</td>
<td>00</td>
<td>0</td>
<td>Nothing assigned. If necessary, set to 0. When read, the content is 0.</td>
<td>—</td>
</tr>
<tr>
<td>b6</td>
<td>SEIE</td>
<td></td>
<td>0</td>
<td>Periodic interrupt triggered every second enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b5</td>
<td>MINE</td>
<td></td>
<td>0</td>
<td>Periodic interrupt triggered every minute enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b4</td>
<td>HRIE</td>
<td></td>
<td>0</td>
<td>Periodic interrupt triggered every hour enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b3</td>
<td>DYIE</td>
<td></td>
<td>0</td>
<td>Periodic interrupt triggered every day enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b2</td>
<td>WKIE</td>
<td></td>
<td>0</td>
<td>Periodic interrupt triggered every week enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b1</td>
<td>COMIE</td>
<td></td>
<td>0</td>
<td>Compare match interrupt enable bit</td>
<td>RW</td>
</tr>
<tr>
<td>b0</td>
<td></td>
<td></td>
<td>0</td>
<td>Disable compare match interrupt</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Figure 3.5** TRECR2 Register in Output Compare Mode
### Timer RE Count Source Select Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRECSR</td>
<td>011Eh</td>
<td>00001000b</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>RCS0</td>
<td>Count source select bits</td>
<td>0/1: f4, 0: f8, 1: f32, 11: fC4</td>
<td>RW</td>
</tr>
<tr>
<td>RCS1</td>
<td></td>
<td></td>
<td>RW</td>
</tr>
<tr>
<td>RCS2</td>
<td>4-bit counter select bit</td>
<td>0: Not used, 1: Used</td>
<td>RW</td>
</tr>
<tr>
<td>RCS3</td>
<td>Real-time clock mode select bit</td>
<td>Set to 0 in output compare mode</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td>(b4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RCS5</td>
<td>Clock output select bits$^{(1)}$</td>
<td>0/1: f2, 0: f4, 1: f8, 11: Compare output</td>
<td>RW</td>
</tr>
<tr>
<td>RCS6</td>
<td></td>
<td></td>
<td>RW</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Write to bits RCS5 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

---

Figure 3.6  **TRECSR Register in Output Compare Mode**
Figure 3.7 Operation in Output Compare Mode

- **TREMIN register** setting value
- **TSTART bit** in **TRECR1 register**
- **TCSTF bit** in **TRECR1 register**
- **IR bit** in **TREIC register**
- **TREO output**

The above applies under the following conditions:
- **TOENA bit** in **TRECR1 register** = 1 (enable clock output)
- **COMIE bit** in **TRECR2 register** = 1 (enable compare match interrupt)
- RCS6 to RCS5 bits in **TRECSR register** = 11b (compare output)

Count starts
- **Matched**
- **Matched**
- **Matched**

Set to 1 by a program

Set to 0 by acknowledgement of interrupt request or a program

Output polarity is inverted when the compare matches
3.3 Notes on Timer RE

3.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.

Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to two cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR.

3.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped:

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
4. Program Outline

Every time a compare match is detected, the TREO output polarity is reversed. The output width for “H” period and “L” period is set to 100 μs.

\[100 \mu s = 20 \text{ MHz} \times 8 \times (\text{4-bit counter is not used}) \times (\text{TREMIN} + 1) = 50 \text{ ns} \times 8 \times 2 \times 125\]

Figure 4.1 shows an Assigned Pin.

![Assigned Pin Diagram]

**Figure 4.1 Assigned Pin**

### 4.1 Function Table

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void timer_re_init (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Timer RE associated SFR initial setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td>Variable used (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td>Function</td>
<td>Timer RE associated SFR register settings are initialized.</td>
</tr>
</tbody>
</table>
4.2 Flow Chart

4.2.1 Main Function

```
main()

asm("FCLR I")

prc0 ← 1

cm13 ← 1

cm15 ← 1

cm05 ← 0

while(i <= 255) i++

ocd2 ← 0

cm16 ← 0

cm17 ← 0

cm06 ← 0

prc0 ← 0

Timer RE associated SFR initial setting handling

timer_re_init()
```

Interrupt disabled

System control register protect disabled

XIN-XOUT pin

XIN-XOUT drive capacity select: Set High

Main clock oscillates

Wait until oscillation stabilizes

Select main clock

Main clock: No division

Main clock division: CM16, CM17 enabled

System control register protect

Timer RE associated SFR initial setting handling (output compare mode setting)
4.2.2 Timer RE Associated SFR Initial Setting

```
timer_re_init()
tstart_trecr1 ← 0

No
tcstf_trecr1 = 0?
    Yes
        treic ← 0x00

    No
        treic ← 0x00

    Yes
        timer_re_operation_stops

    No
        Timer RE operation stops

    Yes
        Timer RE interrupt disabled

        Timer RE register and control circuit reset

        Count source: Select f8
        4-bit counter: Not used
        Set to 0 in output compare mode
        Clock output: Select compare output

        Count period: Set 100 ms (50 ns x 8 x 2 x 125 = 100 ms)

    No
        toena_trecr1 ← 1

    Yes
        TREO pin: Select clock output enable

        Timer RE operation starts
```

return
5. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
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6. Reference Documents

Hardware Manual
R8C/25 Group Hardware Manual
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csc@renesas.com

<table>
<thead>
<tr>
<th>REVISION HISTORY</th>
<th>R8C/25 Group Timer RE in Output Compare Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev.</td>
<td>Date</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>1.00</td>
<td>Dec 01, 2006</td>
</tr>
<tr>
<td>1.10</td>
<td>Feb 29, 2008</td>
</tr>
</tbody>
</table>
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