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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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1. Abstract

This document describes a program for timer RD in the input capture and output compare functions.

2. Introduction

The application example described in this document applies to the following MCU and parameter(s):

- MCU : R8C/25 Group

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.
3. Application Example Description

Timer RD has two 16-bit timers (channels 0 and 1). Each channel has four I/O pins.

Timer mode consists of two functions: Input capture and output compare. In the input capture and output compare functions, channels 0 and 1 have the equivalent functions, and functions can be selected individually for each pin. Also, a combination of these functions can be used in one channel.

The input capture function measures the width or period of an external signal. An external signal input to the TRDIOji (i = 0 or 1, j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRDi register (counter) to the TRDGRji register (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected individually for each pin.

The TRDGRA0 register can also select FOCO128 as the input capture trigger input.

The output compare function detects matches (compare match) between the content of the TRDi (i = 0 or 1) register (counter) and the content of the TRDGRji (j = A, B, C, or D) register. When the contents match, a given level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected individually for each pin.

The setting conditions for this program are as follows:

- Channel used : This program uses only channel 0. Channel 1 is not used.
- Input capture input pin : TRDIOA0
- Output compare output pins : TRDIOB0 and TRDIOD0
- Timer RD synchronization : TRD0 and TRD1 operate independently
- TRDGRC0 register function : Buffer register of TRDGRA0 register
- TRDGRD0 register function : General register
- External clock input : Disabled
- Pin output enable : TRDIOB0 and TRDIOD0 pin output enabled; TRDIOA0 and TRDIOC0 pin output disabled
- Pulse output forced cutoff input : Disabled
- TRDIOB0 output level : Initial output “L”
- TRDIOD0 output level : Initial output “L”
- TRDIOA pin digital filter : Function is used; Clock is set as count source.
- Count source : f1
- TRD0 counter clear : Clear disabled (free-running operation)
- TRDGRA0 control : Input capture to TRDGRA0 at both edges
- Input capture input switch : TRDIOA0 pin input
- TRDGRB0 control : “H” output at TRDGRB0 compare match
- TRDGRD0 control : “H” output at TRDGRD0 compare match
- Interrupt enable : Interrupt by bits IMFA and OVF enabled; Interrupt by bits IMFB and IMFD disabled
- TRDGRB0 compare value : 20000 − 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms
  Compare match when 1 ms elapses after the TRD0 count starts
- TRDGRD0 compare value : 40000 − 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms
  Compare match when 2 ms elapses after the TRD0 count starts

Figure 3.1 shows an Operating Example of Input Capture Function and Figure 3.2 shows an Operating Example of Output Compare Function.
Figure 3.1  Operating Example of Input Capture Function

The above applies under the following conditions:
- Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (the TRDi register is set to 0000h at the TRDGRAi register input capture).
- Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
- Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
- The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register).

The above applies under the following conditions:
This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

Figure 3.2 Operating Example of Output Compare Function

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDI register does not stop at the counter clear compare match).
Bits BF3 and BF1 in the TRDMR register are set to 0 (registers TRDGRCi and TRDGROi do not operate as buffers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (TRDIOAi, TRDIOBi, and TRDIOCi output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (the TRDI register is set to 000h at the TRDGRAi register compare match).
Bits TOAi and TOBi in the TRDOCR register are set to 0 ("L" initial output until compare match) and the TOCi bit is set to 1 ("H" initial output until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b ("H" TRDIOBi output at TRDGROi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b ("L" TRDIOCi output at TRDGRCi register compare match).
The IOC3 bit in the TRDIORCi register is set to 1 (the TRDGRCi register does not control the TRDIOBi pin output).
3.1 Pins Used

Table 3.1 Pins Used and Their Function

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2_0/TRDIOA0/</td>
<td>Input</td>
<td>Input capture input pin</td>
</tr>
<tr>
<td>TRDCLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2_1/TRDIOB0</td>
<td>Output</td>
<td>Output compare output pin</td>
</tr>
<tr>
<td>P2_3/TRDIOD0</td>
<td>Output</td>
<td>Output compare output pin</td>
</tr>
</tbody>
</table>

Figure 3.3 Pins Used

3.2 Memory Usage

Table 3.2 Memory Usage

<table>
<thead>
<tr>
<th>Memory Usage</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>281 bytes</td>
<td>In main.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>11 bytes</td>
<td>In main.c module</td>
</tr>
<tr>
<td>Maximum user stack usage</td>
<td>10 bytes</td>
<td>main function: 7 bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>timer_rd_init function: 3 bytes</td>
</tr>
<tr>
<td>Maximum interrupt stack usage</td>
<td>18 bytes</td>
<td>TRD0_int function: 18 bytes</td>
</tr>
</tbody>
</table>

Memory usage varies depending on the C compiler version and the compile option.
The above applies under the following conditions:
• C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
• Compile option: -c -finfo; NOTE: -dir "$CONFIGDIR" -R8C
  NOTE: Unavailable in the R8C/Tiny-exclusive free version.
4. Setup

This section shows the initial setting procedures and values to perform the example described in 3. Application Example Description. Refer to the R8C/25 Group Hardware Manual for details on individual registers.

4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

PRC0 [Address 000Ah]
Protect bit 0
Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

CM1 [Address 0007h]
CM14 Low-speed on-chip oscillator oscillates
Low-speed on-chip oscillator oscillates

(3) Set the division ratio of the high-speed on-chip oscillator clock.

High-Speed On-Chip Oscillator Control Register 2

<table>
<thead>
<tr>
<th>b7-b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

FRA2 [Address 0025h]
FRA22 to FRA20 High-speed on-chip oscillator frequency switch bits
Divide-by-2 mode
(b7-b3) Reserved bits
Set to 0.

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

FRA0 [Address 0023h]
FRA00 High-speed on-chip oscillator enable bit
High-speed on-chip oscillator oscillates
(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

```
<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
```

FRA0 [Address 0023h]

FRA01 High-speed on-chip oscillator select bit
High-speed on-chip oscillator selected

(7) Set system clock division select bits 1.

```
<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

CM1 [Address 0007h]

CM17 and CM16 System clock division select bits 1
No division mode

(8) Set system clock division select bit 0.

```
<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

CM0 [Address 0006h]

CM06 System clock division select bit 0
CM16 and CM17 enabled

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

```
<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>
```

PRC0 [Address 000Ah]

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 disabled
4.2 Timer Mode (Input Capture and Output Compare Functions) Setting

(1) Set the port P2 direction register.

Port P2 Direction Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PD2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[Address 00E6h]</td>
</tr>
</tbody>
</table>

PD2_0 Port P2_0 direction bit
Input mode

(2) Set timer RD start register (TRD0 count stops).

Timer RD Start Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>TRDSTR [Address 0137h]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRD0 count start flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Count stops</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRD1 count start flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Unavailable. Set to 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRD0 count operation select bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Set to 1 in the input capture function.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRD1 count operation select bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Unavailable. Set to 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Nothing is assigned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b7-b4)</td>
<td></td>
<td></td>
<td></td>
<td>Set to 0.</td>
</tr>
</tbody>
</table>

NOTE:
1. Use the MOV instruction to set the TRDSTR register (do not use the bit handling instruction).

(3) Set the timer RD (channel 0) interrupt control register.

Timer RD (Channel 0) Interrupt Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>TRD0IC [Address 0048h]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Interrupt priority level select bits 2 to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Level 0 (interrupt disabled)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Interrupt request bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No interrupt request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(b7-b4)</td>
<td></td>
<td></td>
<td></td>
<td>Nothing is assigned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Set to 0.</td>
</tr>
</tbody>
</table>
(4) Set the timer RD mode register.

**Timer RD Mode Register**

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**TRDMR** [Address 0138h]
- **SYNC** Timer RD synchronous bit
  - TRD0 and TRD1 operate independently
- (b3-b1) Nothing is assigned.
  - Set to 0.
- **BFC0** TRDGRC0 register function select bit
  - Buffer register of TRDGRA0 register
- **BFD0** TRDGRO0 register function select bit
  - General register
- **BFC1** TRDGRC1 register function select bit
  - Unavailable. Set to 0.
- **BFD1** TRDGRO1 register function select bit
  - Unavailable. Set to 0.

(5) Set the timer RD PWM mode register.

**Timer RD PWM Mode Register**

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**TRDPMR** [Address 0139h]
- **PWMB0** TRDIOB0 PWM mode select bit
  - Set to 0 in timer mode.
- **PWMC0** TRDIOC0 PWM mode select bit
  - Set to 0 in timer mode.
- **PWMD0** TRDIOD0 PWM mode select bit
  - Set to 0 in timer mode.
- (b3) Nothing is assigned.
  - Set to 0.
- **PWMB1** TRDIOB1 PWM mode select bit
  - Unavailable. Set to 0.
- **PWMC1** TRDIOC1 PWM mode select bit
  - Unavailable. Set to 0.
- **PWMD1** TRDIOD1 PWM mode select bit
  - Unavailable. Set to 0.
- (b7) Nothing is assigned.
  - Set to 0.
(6) Set the timer RD function control register.

**Timer RD Function Control Register**

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- **TRDFCR** [Address 013Ah]
  - **CMD1 and CMD0** Combination mode select bits
    - Set to 00b in timer mode.
  - **OLS0** Normal-phase output level select bit
    - This bit is disabled in timer mode.
  - **OLS1** Counter-phase output level select bit
    - This bit is disabled in timer mode.
  - **ADTRG** A/D trigger enable bit
    - This bit is disabled in timer mode.
  - **ADEG** A/D trigger edge select bit
    - This bit is disabled in timer mode.
  - **STCLK** External clock input select bit
    - External clock input disabled
  - **PWM3** PWM3 mode select bit
    - Set to 1 in timer mode.

(7) Set timer RD output master enable register 1.

**Timer RD Output Master Enable Register 1**

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- **TRDOER1** [Address 013Bh]
  - **EA0** TRDIOA0 output disable bit
    - This bit is disabled for use as input capture input
  - **EB0** TRDIOB0 output disable bit
    - Output enabled
  - **EC0** TRDIOC0 output disable bit
    - Output disabled (TRDIOC0 pin used as a programmable I/O port)
  - **ED0** TRDIOD0 output disable bit
    - Output enabled
  - **EA1** TRDIOA1 output disable bit
    - Output disabled (TRDIOA1 pin used as a programmable I/O port)
  - **EB1** TRDIOB1 output disable bit
    - Output disabled (TRDIOB1 pin used as a programmable I/O port)
  - **EC1** TRDIOC1 output disable bit
    - Output disabled (TRDIOC1 pin used as a programmable I/O port)
  - **ED1** TRDIOD1 output disable bit
    - Output disabled (TRDIOD1 pin used as a programmable I/O port)
(8) Set timer RD output master enable register 2.

![Timer RD Output Master Enable Register 2](image)

(9) Set the timer RD output control register.

![Timer RD Output Control Register](image)
(10) Set timer RD digital filter function select register 0.

![Timer RD Digital Filter Function Select Register 0](image)

(11) Set timer RD control register 0.

![Timer RD Control Register 0](image)
(12) Set timer RD I/O control register A0.

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**TRDIOA0 [Address 0141h]**

- **IOA1 and IOA0**: TRDGRA control bits
  - Input capture to TRDGRA0 at both edges
- **IOA2**: TRDGRA mode select bit
  - Set to 1 in the input capture function.
- **IOA3**: Input capture input switch bit
  - TRDIOA0 pin input
- **IOB1 and IOB0**: TRDGRB control bits
  - "H" output at TRDGRB0 compare match
- **IOB2**: TRDGRB mode select bit
  - Set to 0 in the output compare function.
- **(b7)**: Nothing is assigned.
  - Set to 0.

(13) Set timer RD/IO control register C0.

<table>
<thead>
<tr>
<th>b7</th>
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<tbody>
<tr>
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<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**TRDIORC0 [Address 0142h]**

- **IOC1 and IOC0**: TRDGRC control bits
  - Unavailable.
- **IOC2**: TRDGRC mode select bit
  - To select 1 (buffer register of TRDGRA0 register) by the BFC0 bit in the TRDMR register, set the IOC2 bit in the TRDIORC0 register to the same value as the IOA2 bit in the TRDIOA0 register.
- **IOC3**: TRDGRC register function select bit
  - Set to 1 in the input capture function.
- **IOD1 and IOD0**: TRDGRD control bits
  - "H" output at TRDGRD0 compare match
- **IOD2**: TRDGRD mode select bit
  - Set to 0 in the output compare function.
- **IOD3**: TRDGRD register select bit
  - General register or buffer register
(14) Set timer RD counter 0.

Timer RD Counter 0

(b15) b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 0 0
TRD0 [Address 0147h to 0146h]

Initialization
0 (0x0000) setting

(15) Set timer RD general register A0.

Timer RD General Register A0

(b15) b7 b6 b5 b4 b3 b2 b1 b0
1 1 1 1 1 1 1 1 1
TRDGRA0 [Address 0149h to 0148h]

Initialization
0xFFFF setting

(16) Set timer RD general register B0.

Timer RD General Register B0

(b15) b7 b6 b5 b4 b3 b2 b1 b0
0 1 0 1 1 0 0 1 1 1
TRDGRC0 [Address 014Dh to 014Ch]

The compare value with the TRD0 register (counter) is stored
20000 – 1 (0x4E1F) setting

(17) Set timer RD general register C0.

Timer RD General Register C0

(b15) b7 b6 b5 b4 b3 b2 b1 b0
1 1 1 1 1 1 1 1 1 1
TRDGRB0 [Address 014Bh to 014Ah]

Initialization
0xFFFF setting
(18) Set timer RD general register D0.

TRDGRD0 [Address 014F to 014Eh]

The compare value with the TRD0 register is stored
40000 – 1 (0x9C3F) setting

(19) Set timer RD interrupt enable register 0.

TRDIER0 [Address 0144h]

IMIEA  Input capture/compare match interrupt enable bit A
        Interrupt (IMIA) by IMFA bit enabled
IMIEB  Input capture/compare match interrupt enable bit B
        Interrupt (IMIB) by IMFB bit disabled
IMIEC  Input capture/compare match interrupt enable bit C
        Interrupt (IMIC) by IMFC bit disabled
IMIED  Input capture/compare match interrupt enable bit D
        Interrupt (IMID) by IMF D bit disabled
OVI E  Overflow/underflow interrupt enable bit
        Interrupt (OVI) by OVF bit enabled

(b15) (b8) (b7) (b0)  
1 0 0 1 1 1 0 0 0 1 1 1 1 1

(b7-b5) Nothing is assigned.
Set to 0.
(20) Set timer RD status register 0.

Timer RD Status Register 0

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **IMFA**: Input capture/compare match flag A
  - Set to 0.
- **IMFB**: Input capture/compare match flag B
  - Set to 0.
- **IMFC**: Input capture/compare match flag C
  - Set to 0.
- **IMFD**: Input capture/compare match flag D
  - Set to 0.
- **OVF**: Overflow flag
  - Set to 0.
- **(b7-b5)**: Nothing is assigned.
  - Set to 0.

(21) Set the timer RD (channel 0) interrupt control register.

Timer RD (Channel 0) Interrupt Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

- **TRD0IC**: [Address 0048h]
  - **ILVL2 to ILVL0**: Interrupt priority level select bits 2 to 0
    - Level 7
- **IR**: Interrupt request bit
  - No interrupt request
- **(b7-b4)**: Nothing is assigned.
  - Set to 0.
(22) Set the timer RD start register (TRD0 count starts).

NOTE:
1. Use the MOV instruction to set the TRDSTR register (do not use the bit handling instruction).
5. Flowchart

5.1 Main Function

5.1.1 Main Function 1

```c
asm ("FCLR I")
prc0 ← 1
cm14 ← 0
fra2 ← 0x00
fra00 ← 1

Repeat
(i <= 255)

i++;,

fra01 ← 1
cm16 ← 0

No system clock division

cm17 ← 0
cm06 ← 0
prc0 ← 0

Timer RD associated SFR initial setting processing
(timer_rd_init())
asm("FSET I")

1
```

Disable interrupts
Disable system control register protect
Start the low-speed on-chip oscillator
High-speed on-chip oscillator clock: Divide-by-2 mode
Start the high-speed on-chip oscillator
Wait until oscillation stabilizes
Select the high-speed on-chip oscillator
Enable CM16 and CM17
Enable system control register protect
Timer RD associated SFR initial setting processing (input capture and output compare functions)
Enable interrupts
5.1.2 Main Function 2

1

f_capture = 1?
  Yes
  ovf_cnt = 0?
    Yes
    measurement_value ←
    general_register − buffer_register
    f_capture ← 0
  No
  ovf_cnt = 0?
    Yes
    measurement_value ←
    0x00010000 * ovf_cnt
    − buffer_register + general_register
    ovf_cnt ← 0
    Clear the overflow counter
    measurement_value ←
    general_register − buffer_register
  No
  Check the capture
    Yes
  No
  Check the overflow
    Yes
    Calculate the measurement value
  No

measurement_value ←
general_register − buffer_register

Clear the capture flag
5.2 Timer RD Associated SFR Initial Setting Processing

5.2.1 Timer RD Associated SFR Initial Setting Processing 1

```
<table>
<thead>
<tr>
<th>Function</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>timer_rd_init()</td>
<td></td>
<td></td>
</tr>
<tr>
<td>pd2 ← pd2&amp;0xFE</td>
<td></td>
<td>Stop the TRD0 count</td>
</tr>
<tr>
<td>trdstr ← 0x0C</td>
<td></td>
<td>TRD0 interrupt: Interrupt level 0 (interrupt disabled)</td>
</tr>
<tr>
<td>trd0ic ← 0x00</td>
<td></td>
<td>Operate TRD0 and TRD1 independently</td>
</tr>
<tr>
<td>trdmr ← 0x10</td>
<td></td>
<td>Operate the TRDGRC0 register as a buffer register of the TRDGRA0 register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Operate the TRDGRD0 register as a general register</td>
</tr>
<tr>
<td>trdpmr ← 0x00</td>
<td></td>
<td>Initialization</td>
</tr>
<tr>
<td>trdfcr ← 0x80</td>
<td></td>
<td>Disable the external clock input</td>
</tr>
<tr>
<td>trdoer1 ← 0xF5</td>
<td></td>
<td>TRDIOA0 pin: Disable output</td>
</tr>
<tr>
<td>trdocr ← 0x00</td>
<td></td>
<td>TRDIOB0 pin: Enable output</td>
</tr>
<tr>
<td>trddf0 ← 0xC1</td>
<td></td>
<td>TRDIOC0 pin: Disable output</td>
</tr>
<tr>
<td>trdocr0 ← 0x00</td>
<td></td>
<td>TRDIOD0 pin: Enable output</td>
</tr>
<tr>
<td>pto_trdoer2 ← 0</td>
<td></td>
<td>Disable the pulse output forced cutoff input</td>
</tr>
<tr>
<td>trdocr ← 0x00</td>
<td></td>
<td>TRDIOB0 pin: Initial output &quot;L&quot;</td>
</tr>
<tr>
<td>trddf0 ← 0xC1</td>
<td></td>
<td>TRDIOA pin: Digital filter function used</td>
</tr>
<tr>
<td>trdocr0 ← 0x00</td>
<td></td>
<td>Digital filter function clock: Select the count source</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>Count source: Select f1</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>TRDIOA0 input: Input capture to TRDGRA0 at both edges</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>Input capture input: TRDIA0 pin</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>Output &quot;H&quot; at the TRDGRB0 compare match</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>To select 1 (buffer register of TRDGRA0 register) by the BFC0 bit in the</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>the TRDMR register, set the IOA2 bit in the TRDIORC0 register to the same</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>value as the IOA2 bit in the TRDIOA0 register.</td>
</tr>
<tr>
<td>trdioa0 ← 0x2E</td>
<td></td>
<td>Output “H” at the TRDGRD0 compare match</td>
</tr>
</tbody>
</table>
```
5.2.2 Timer RD Associated SER Initial Setting Processing 2

1. Initialize the TRD0 register count value to 0x0000.

2. Initialize the TRDGRA0 register count value to 0xFFFF.

3. Count period: Set to 1 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms)

4. Initialize the TRDGRC0 register count value to 0xFFFF.

5. Count period: Set to 2 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms)

6. Enable interrupt (IMIA) by the IMFA bit

7. Disable interrupt (IMIB) by the IMFB bit

8. Disable interrupt (IMIC) by the IMFC bit

9. Disable interrupt (IMID) by the IMFD bit

10. Enable interrupt (OVI) by the OVF bit

11. Initialize timer RD status register 0

12. TRD0 interrupt: Interrupt priority level 7

13. Start the TRD0 count

return
5.3 Timer RD0 Interrupt Handling

TRD0_int()

Is an input capture signal to the TRDIOA0 pin detected?

Yes

imfa_trdsr0 = 1?

No

imfa_trdsr0 ← 0

Clear input capture flag A

Yes

general_register ← trdgra0

Read the TRDGRA0 register

buffer_register ← trdgrc0

Read the TRDGRC0 register

f_capture ← 1

Set the capture flag

Yes

ovf_trdsr0 = 1?

No

ovf_trdsr0 ← 0

Overflow?

Yes

Clear the overflow flag

ovf_cnt++

Increment the overflow counter

return
6. **Sample Programming Code**

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Series page.

7. **Reference Documents**

   Hardware Manual
   R8C/25 Group Hardware Manual
   The latest version can be downloaded from the Renesas Technology website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Technology website.
Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

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<table>
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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>1.00</td>
<td>June 29, 2007</td>
<td>– First Edition issued</td>
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