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1. Abstract

This document describes how to set up and use the timer RB in timer mode on the R8C/25 Group device.

2. Introduction

The application example described in this document is applied to the following:

- MCU: R8C/25 Group
- XIN clock: 20 MHz

This program can be used with other R8C/Tiny Series which have the same SFR (special function register) as the R8/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.
3. Applications

3.1 Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler. The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address (refer to Table 3.1 Timer Mode Specifications for access to the reload register and counter). Timer RB has timer RB primary and timer RB secondary as reload registers.

The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.

Figure 3.1 shows a Block Diagram of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

![Figure 3.1 Block Diagram of Timer RB](image-url)
3.2 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to Table 3.1). Registers TRBOCR and TRBSC are not used in timer mode.

Figure 3.2 shows Registers TRBCR and TRBIOC in Timer Mode, and Figure 3.3 shows Registers TRBMR, TRBPRE, and TRBPR in Timer Mode.

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count sources</td>
<td>f1, f2, f8, timer RA underflow</td>
</tr>
<tr>
<td>Count operations</td>
<td>• Decrement</td>
</tr>
<tr>
<td></td>
<td>• When the timer underflows, it reloads the reload register contents before</td>
</tr>
<tr>
<td></td>
<td>the count continues (when timer RB underflows, the contents of timer RB</td>
</tr>
<tr>
<td></td>
<td>primary reload register is reloaded).</td>
</tr>
<tr>
<td>Divide ratio</td>
<td>1/(n+1)(m+1)</td>
</tr>
<tr>
<td></td>
<td>n: setting value in TRBPRE register, m: setting value in TRBPR register</td>
</tr>
<tr>
<td>Count start condition</td>
<td>1 (count starts) is written to the TSTART bit in the TRBCR register.</td>
</tr>
<tr>
<td>Count stop conditions</td>
<td>• 0 (count stops) is written to the TSTART bit in the TRBCR register.</td>
</tr>
<tr>
<td></td>
<td>• 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.</td>
</tr>
<tr>
<td>Interrupt request</td>
<td>• When timer RB underflows [timer RB interrupt].</td>
</tr>
<tr>
<td>generation timing</td>
<td></td>
</tr>
<tr>
<td>TRBO pin function</td>
<td>Programmable I/O port</td>
</tr>
<tr>
<td>INT0 pin function</td>
<td>Programmable I/O port or INT0 interrupt input</td>
</tr>
<tr>
<td>Read from timer</td>
<td>The count value can be read out by reading registers TRBPR and TRBPRE.</td>
</tr>
<tr>
<td>Write to timer</td>
<td>• When registers TRBPRE and TRBPR are written while the count is stopped,</td>
</tr>
<tr>
<td></td>
<td>values are written to both the reload register and counter.</td>
</tr>
<tr>
<td></td>
<td>• When registers TRBPRE and TRBPR are written to while count operation is</td>
</tr>
<tr>
<td></td>
<td>in progress:</td>
</tr>
<tr>
<td></td>
<td>If the TWRC bit in the TRBMR register is set to 0, the value is written to</td>
</tr>
<tr>
<td></td>
<td>both the reload register and the counter.</td>
</tr>
<tr>
<td></td>
<td>If the TWRC bit is set to 1, the value is written to the reload register</td>
</tr>
<tr>
<td></td>
<td>only. (Refer to 3.3 Timer Write Control during Count Operation.)</td>
</tr>
</tbody>
</table>
### Timer RB Control Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRBCR</td>
<td>0108h</td>
<td>00h</td>
<td>TSTART</td>
<td>Timer RB count start bit(1)</td>
<td>0 : Count stops 1 : Count starts</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TCSTF</td>
<td>Timer RB count status flag(1)</td>
<td>0 : Count stops 1 : During count(2)</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSTOP</td>
<td>Timer RB count forcible stop bit(1,2)</td>
<td>When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(b7-b3)</td>
<td>Nothing is assigned. If necessary, set to 0. When read, the content is 0.</td>
<td>—</td>
</tr>
</tbody>
</table>

### Timer RB I/O Control Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRBIOC</td>
<td>010Ah</td>
<td>00h</td>
<td>TOPL</td>
<td>Timer RB output level select bit</td>
<td>Set to 0 in timer mode.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TOCNT</td>
<td>Timer RB output switch bit</td>
<td>Set to 0 in timer mode.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>INOSTG</td>
<td>One-shot trigger control bit</td>
<td>Set to 0 in timer mode.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>INOSEG</td>
<td>One-shot trigger polarity select bit</td>
<td>Set to 0 in timer mode.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(b7-b4)</td>
<td>Nothing is assigned. If necessary, set to 0. When read, the content is 0.</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Refer to 3.4 Notes on Timer RB.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

Figure 3.2 Registers TRBCR and TRBIOC in Timer Mode
### Timer RB Mode Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRBMR</td>
<td>010Bh</td>
<td>00h</td>
<td>b7 b6 b5 b4 b3 b2 b1 b0</td>
<td>Timer RB operating mode select bits&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 0</td>
<td>Timer mode</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>b2</td>
<td>Nothing assigned. If necessary, set to 0.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, the content is 0.</td>
<td>—</td>
</tr>
<tr>
<td>TWRC</td>
<td></td>
<td></td>
<td>b7 b6</td>
<td>Timer RB write control bit</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 0</td>
<td>Writes to reload both register and counter</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 1</td>
<td>Writes to reload only register</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 0</td>
<td>Timer RB underflow</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 1</td>
<td>Timer RA underflow</td>
<td>RW</td>
</tr>
<tr>
<td>TCK0</td>
<td></td>
<td></td>
<td>b7 b6</td>
<td>Timer RB count source select bits&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 0</td>
<td>f1</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 1</td>
<td>f8</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 0</td>
<td>Timer RA underflow</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 1</td>
<td>Timer RB underflow</td>
<td>RW</td>
</tr>
<tr>
<td>TCK1</td>
<td></td>
<td></td>
<td>b7 b6</td>
<td>Nothing assigned. If necessary, set to 0.</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, the content is 0.</td>
<td>—</td>
</tr>
<tr>
<td>TCKCUT</td>
<td></td>
<td></td>
<td>b7 b6</td>
<td>Timer RB count source cutoff bit&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 0</td>
<td>Provides count source</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 1</td>
<td>Cuts off count source</td>
<td>RW</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).

### Timer RB Prescaler Register<sup>(1)</sup>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
<th>Setting Range</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRBPRE</td>
<td>010Ch</td>
<td>FFh</td>
<td>Counts an internal count source or timer RA underflow s</td>
<td>00h to FFh</td>
<td>RW</td>
</tr>
</tbody>
</table>

**NOTE:**
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

### Timer RB Primary Register<sup>(1)</sup>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Address</th>
<th>After Reset</th>
<th>Function</th>
<th>Setting Range</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRBPR</td>
<td>010Eh</td>
<td>FFh</td>
<td>Counts timer RB prescaler underflow s</td>
<td>00h to FFh</td>
<td>RW</td>
</tr>
</tbody>
</table>

**NOTE:**
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

---

**Figure 3.3** Registers TRBMR, TRBPRE, and TRBPR in Timer Mode
When the TWRC bit is set to 0 (write to reload register and counter)

Set 01h to the TRBPRE register and 25h to the TRBPR register by a program.

Count source

Reloads register of timer RB prescaler

Previous value

New value (01h)

Counter of timer RB prescaler

06h 05h 04h 03h 02h 01h 00h 01h 00h 01h 00h

Reloads register of timer RB

Previous value

New value (25h)

Counter of timer RB

03h 02h 25h 24h

IR bit in TRBIC register

0

The IR bit remains unchanged until underflow is generated by a new value.

When the TWRC bit is set to 1 (write to reload register only)

Set 01h to the TRBPRE register and 25h to the TRBPR register by a program.

Count source

Reloads register of timer RB prescaler

Previous value

New value (01h)

Counter of timer RB prescaler

06h 05h 04h 03h 02h 01h 00h 01h 00h 01h 00h

Reloads register of timer RB

Previous value

New value (25h)

Counter of timer RB

03h 02h 01h 00h 25h

IR bit in TRBIC register

0

Only the prescaler values are updated, extending the duration until timer RB underflow.

The above applies under the following conditions.
Both bits TSTART and TCSTF in the TRBCR register are set to 0 (During count).

Figure 3.4 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation
3.3 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 14.17 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

3.4 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped. During this time, do not access registers associated with timer RB(1) other than the TCSTF bit. The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. During this time, do not access registers associated with timer RB(1) other than the TCSTF bit. Timer RB counting is stopped when the TCSTF bit is set to 0.

NOTE:

1. Registers associated with timer RB: TRBCR, TRBOCR, TRBMR, TRBPRE, TRBSC, and TRRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSS or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSS bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSS bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
4. Program Overview

This program can be used on timer RB to underflow at 1 ms.

\[
1 \text{ ms} = 20 \text{ MHz} \times f_2 \times (\text{TRBPRE register setting value} + 1) \times (\text{TRBPR register setting value} + 1)
\]
\[
= 50 \text{ ns} \times 2 \times (199 + 1) \times (49 + 1)
\]

4.1 Function Table

Table 4.1

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void timer_rb_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overview</td>
<td>SFR initial setting associated with timer RB</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td>Variable used (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td>Return value</td>
<td>Type</td>
</tr>
<tr>
<td>Function</td>
<td>Initialize the SFR registers associated with timer RB</td>
</tr>
</tbody>
</table>
### 4.2 Flow Chart

#### 4.2.1 Main functions

```
main()
asm("FCLR I")
prc0 ← 1
cm13 ← 1
cm15 ← 1
cm05 ← 0
while(i <= 255) I++
ocd2 ← 0
cm16 ← 0
cm17 ← 0
cm06 ← 0
prc0 ← 0

Timer RB SFR initial setting
  timer_rb_init()

asm("FSET I")

if ir_trbic ≠ 0
  trbic ← 0x00
```

- **Interrupt disabled**
- **System control register protect cancelled**
- **XIN-XOUT pin**
- **Select XIN-XOUT drive capacity: HIGH**
- **Main clock oscillation starts**
- **Wait until oscillation stabilizes**
- **Select main clock**
- **Main clock frequency: no divide**
- **CM16 and CM17 enabled**
- **System control register protect**
- **Initialize timer RB SFR setting (Set to timer mode)**
4.2.2 Timer RB SFR Initial Setting

```
4.2.2 Timer RB SFR Initial Setting

--- Diagram ---

timer_rb_init()

- tstart_trbcr ← 0

  No

  tcstf_trbcr = 0 ?

  Yes

  trbic ← 0x00

  tstop_trbcr ← 1

  trbpre ← 200 - 1

  trbpr ← 50 - 1

  topl_trbioc ← 0

  tocnt_trbioc ← 0

  inostg_trbioc ← 0

  inoseg_trbioc ← 0

  tmod0_trbmr ← 0

  tmod1_trbmr ← 0

  twrc_trbmr ← 0

  tck0_trbmr ← 1

  tck1_trbmr ← 1

  tckcut_trbmr ← 0

  tstart_trbcr ← 1

  No

  tcstf_trbcr = 1 ?

  Yes

  return

--- Explanation ---

**Timer RB operation stops**

**Timer RB interrupt disabled**

- Initialize registers TRBPRE and TRBPR, and bits TSTART and TCSTF in TRBCR register

**Underflow period: set to 1 ms (20 MHz × f2₀ × 200 × 50 = 1 ms)**

**Set to 0 in timer mode**

- Set to 0 in timer mode
- Set to 0 in timer mode
- Set to 0 in timer mode
- Set to 0 in timer mode
- Set to 00 in timer mode

**Timer RB write control: set writing to reload register and counter**

- Timer RB count source: f2

**Provide count source**

- Timer RB operation starts**
```
5. **Sample Programming Code**

   Download a sample program from the Renesas Technology website.
   To download, click “Application Notes” in the left-hand side menu on the top page of the R8C/Tiny Series.

6. **Reference Document**

   Hardware Manual
   R8C/25 Group Hardware Manual
   (Download the latest version from the Renesas Technology website.)

   Technical News/Technical Update
   (Download the latest information from the Renesas Technology website.)
# Website and Support

Renesas Technology website  
http://www.renesas.com/

Inquiries  
http://www.renesas.com/inquiry  
csc@renesas.com

## REVISION HISTORY

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