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R8C/25 Group

Timer RB in Programmable Waveform Generation Mode

1. Abstract

This document describes how to set up and use the timer RB in programmable waveform generation mode on the R8C/25 Group device.

2. Introduction

The application example described in this document is applied to the following:

- MCU: R8C/25 Group
- XIN clock: 20 MHz

This program can be used with other R8C/Tiny Series which have the same SFR (special function register) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Applications

3.1 Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address (refer to Table 3.1 Programmable Waveform Generation Mode Specifications for access to the reload register and counter).
Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 3.1 shows a Block Diagram of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

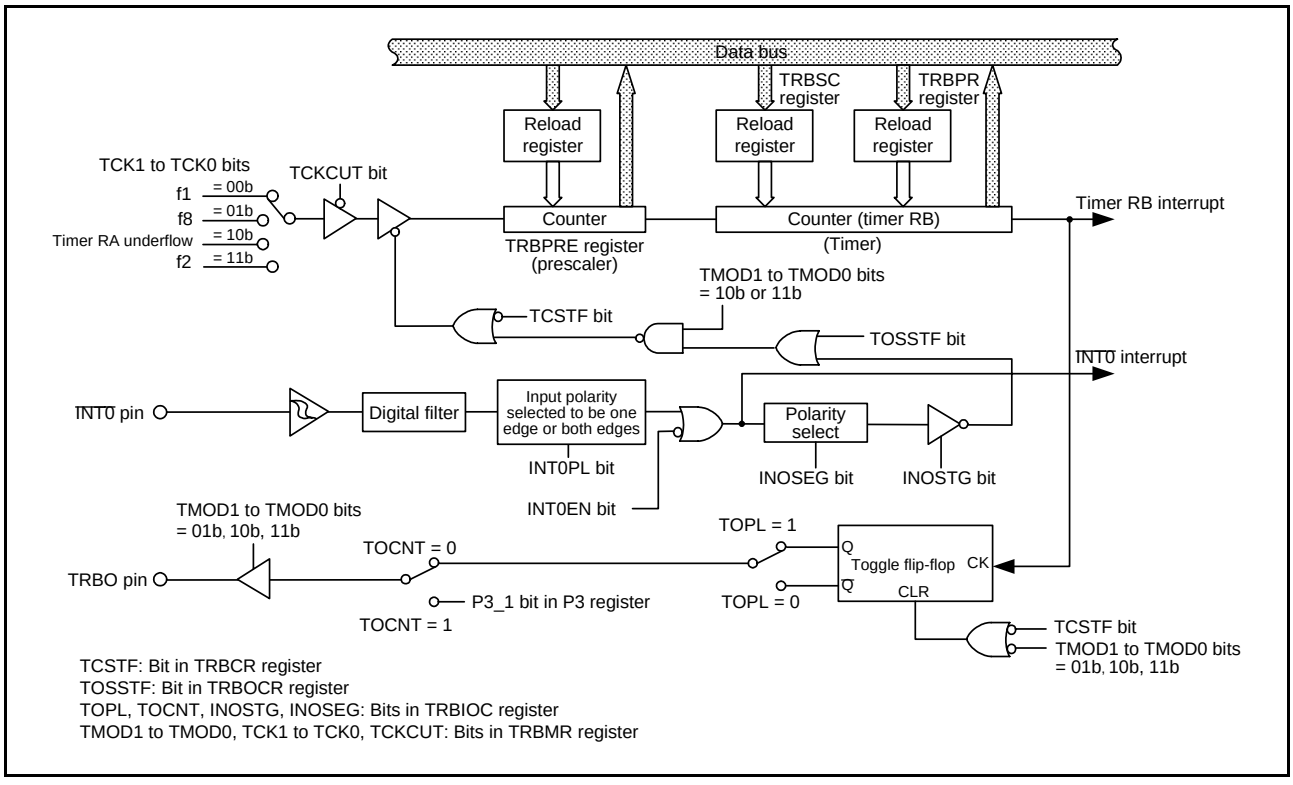


Figure 3.1 Block Diagram of Timer RB

3.2 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to Table 3.1). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.

Figure 3.2 shows the TRBCR Register in Programable Waveform Generation Mode, and Figure 3.3 shows Registers TRBIOC and TRBMR in Programable Waveform Generation Mode, Figure 3.4 shows Registers TRBPRE, TRBSC, and TRBPR in Programable Waveform Generation Mode. Figure 3.5 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

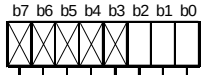
Table 3.1 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: count source frequency n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	• In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
INT0 pin function	Programmable I/O port or INT0 interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE(1).
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(2)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level during primary and secondary periods. • TRBO pin output switch function Timer RB pulse output or P3_1 latch output is selected by the TOCNT bit in the TRBIOC register.(3)

NOTES:

1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   - When count starts.
   - When a timer RB interrupt request is generated.
     The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

Timer RB Control Register



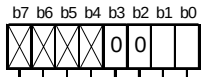
Symbol	Address	After Reset
TRBCR	0108h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RB count start bit(1)	0 : Count stops 1 : Count starts	RW
TCSTF	Timer RB count status flag(1)	0 : Count stops 1 : During count(3)	RO
TSTOP	Timer RB count forcible stop bit(1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **3.3 Notes on Timer RB**.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable w aveform mode. In programmable one-shot generation mode or programmable w ait one-shot generation mode, indicates that a one-shot pulse trigger has been acknow ledged.

Figure 3.2 TRBCR Register in Programable Waveform Generation Mode

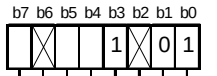
Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0: Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1: Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB output switch bit	0: Outputs timer RB waveform 1: Outputs value in P3_1 port register	RW
INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	RW
INOSEG	One-shot trigger polarity select bit	Set to 0 in programmable waveform generation mode.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Timer RB Mode Register



Symbol	Address	After Reset
TRBMR	010Bh	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RB operating mode select bits(1)	b1 b0 0 1: Programmable waveform generation mode	RW
TMOD1			RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TWRC	Timer RB write control bit	Set to 1 in programmable waveform generation mode.	RW
TCK0	Timer RB count source select bits(1)	b5 b4 0 0 : f1 0 1 : f8 1 0 : Timer RA underflow 1 1 : f2	RW
TCK1			RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCKCUT	Timer RB count source cutoff bit(1)	0: Provides count source 1: Cuts off count source	RW

NOTES:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).

Figure 3.3 Registers TRBIOC and TRBMR in Programable Waveform Generation Mode

Timer RB Prescaler Register(1)

b7 b0

Symbol	Address	After Reset
TRBPRE	010Ch	FFh

Function	Setting Range	RW
Counts an internal count source or timer RA underflows	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

Timer RB Secondary Register(3, 4)

b7 b0

Symbol	Address	After Reset
TRBSC	010Dh	FFh

Function	Setting Range	RW
Counts timer RB prescaler underflows(1)	00h to FFh	WO(2)

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.
3. When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
4. To write to the TRBSC register, perform the following steps.
   (1) Write the value to the TRBSC register.
   (2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

Timer RB Primary Register(2)

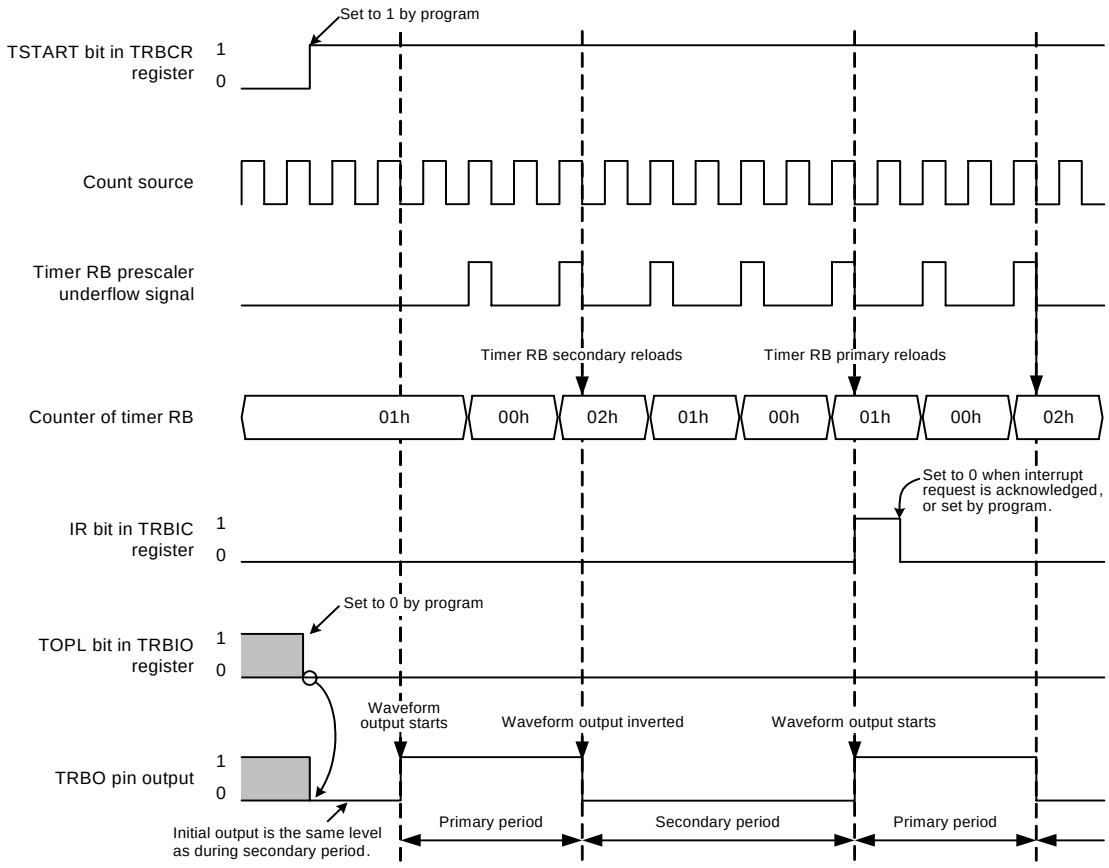
b7 b0

Symbol	Address	After Reset
TRBPR	010Eh	FFh

Function	Setting Range	RW
Counts timer RB prescaler underflows(1)	00h to FFh	RW

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

Figure 3.4 Registers TRBPRE, TRBSC, and TRBPR in Programable Waveform Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 3.5 Operating Example of Timer RB in Programmable Waveform Generation Mode

3.3 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RB[(1)]other than the TCSTF bit.
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress.

  During this time, do not access registers associated with timer RB[(1)] other than the TCSTF bit.
  Timer RB counting is stopped when the TCSTF bit is set to 0.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBMR, TRBPRE, TRBSC, and TRRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

4. Program Overview

By starting the count operation, a signal will be output from the TRBO pin as follows.

- Primary period: 1 ms
  1 ms = 20 MHz × f2 × (TRBPRE + 1) × (TRBPR + 1)
  = 50 ns × 2 × (199 + 1) × (49 + 1)
- Secondary period: 2 ms
  1 ms = 20 MHz × f2 × (TRBPRE + 1) × (TRBSC + 1)
  = 50 ns × 2 × (199 + 1) × (99 + 1)
- "H" output during primary period, "L" output during secondary period, and "L" output when the timer stops

Figure 4.1 shows the Pin Used.

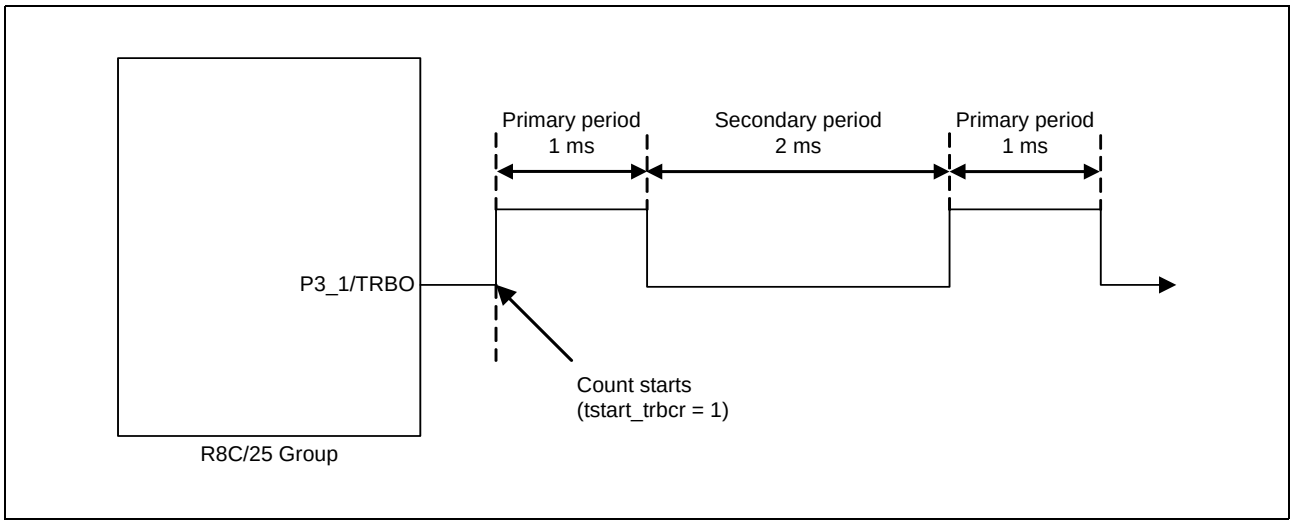


Figure 4.1 Pin Used

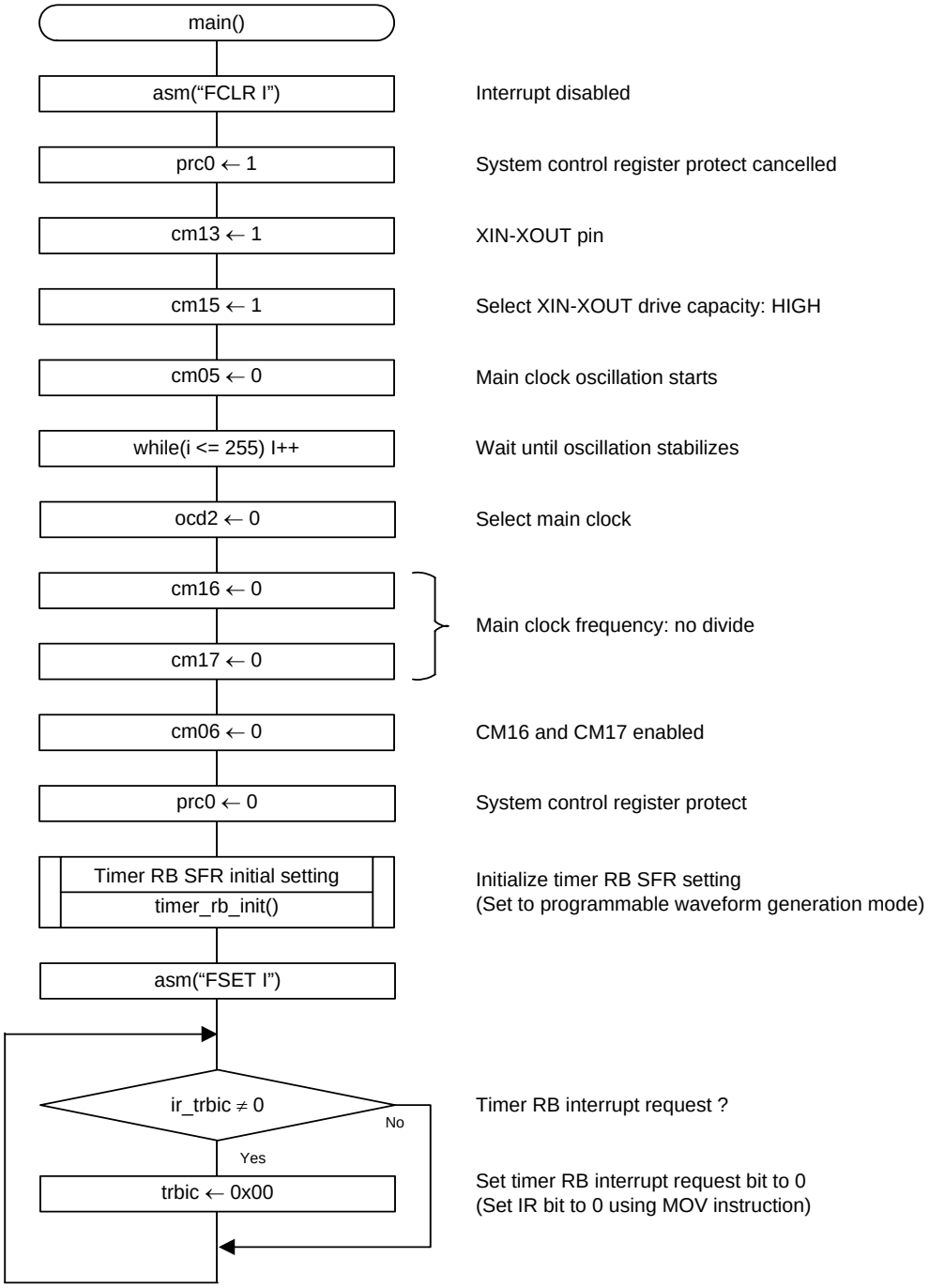
4.1 Faction Table

Table 4.1

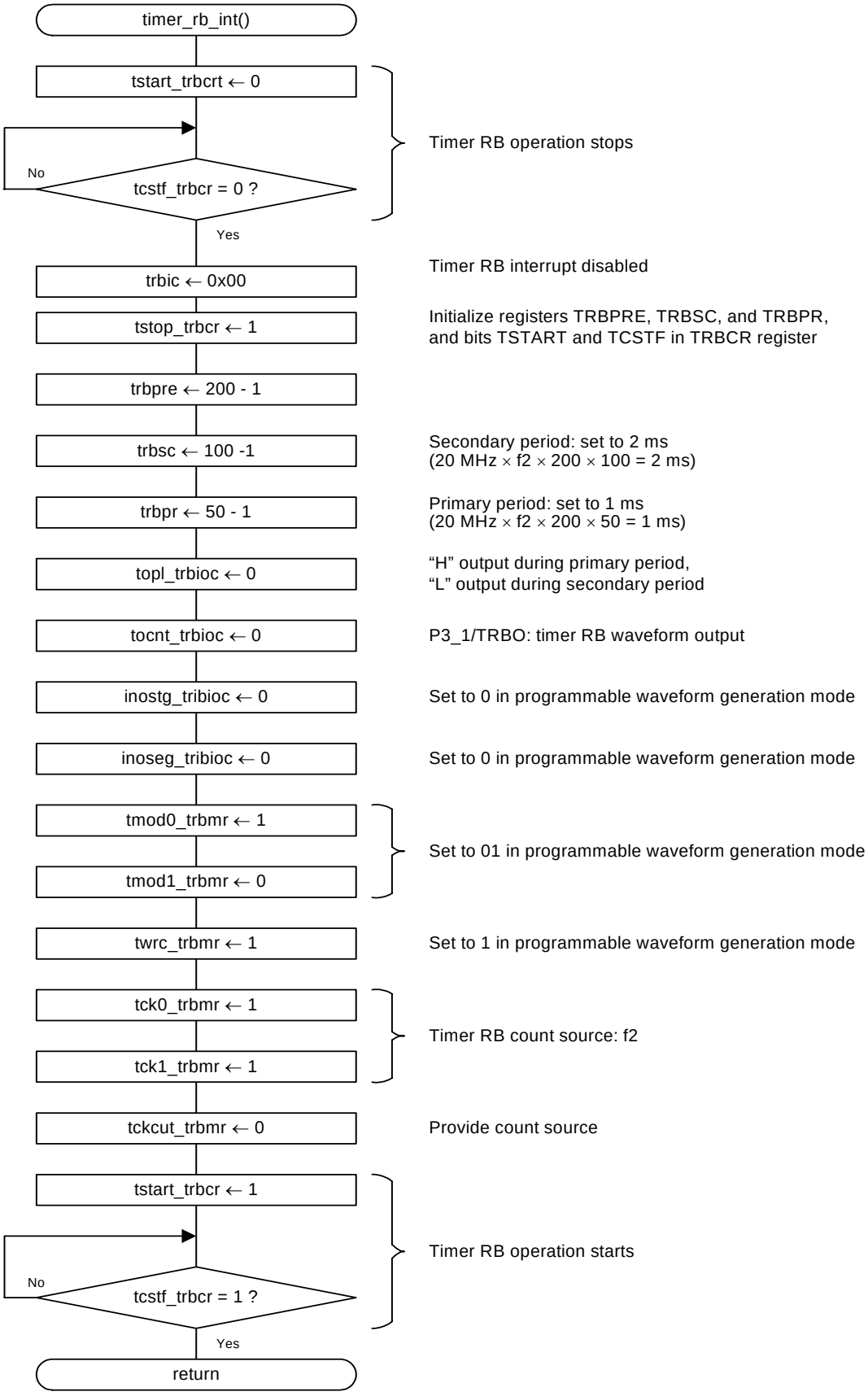
Declaration	void timer_rb_init(void)		
Overview	SFR initial setting associated with timer RB		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Usage
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with time RB		

4.2 Flow Chart

4.2.1 Main functions



4.2.2 Timer RB SFR Initial Setting



5. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu from the top page of the R8C/Tiny Series.

6. Reference Document

Hardware Manual
R8C/25 Group Hardware Manual
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