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April 1st, 2010
Renesas Electronics Corporation

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1. Abstract

This document describes a program for timer RA in pulse period measurement mode.

2. Introduction

The application example described in this document applies to the following MCU and parameter(s):

- **MCU**: R8C/25 Group

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.
3. Application Example Description

In pulse period measurement mode, the pulse period of an external signal input from the INT1/TRAIO pin is measured.

The setting conditions for this program are as follows:

- **Count source**: \( f_8 \)
- **Measurement period**: The period from one rising edge to the next rising edge of the measured pulse
- **Input pin**: INT1/TRAIO pin (P1_7)
- **TRAIO input filter**: No filter
- **Timer RA prescaler underflow period**: 10 μs

\[
40 \text{ MHz (fOCO)} \times f_2 (\text{FRA2}) \times f_8 (\text{TCK0 to TCK2}) \times 25 (\text{TRAPRE register}) = 10 \mu s
\]

Figure 3.1 shows an Operating Example in Pulse Period Measurement Mode.
This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.
3.1 Pin Used

Table 3.1 Pin Used and Its Function

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1_7/TRAIO/INT1</td>
<td>Input</td>
<td>Measurement pulse input</td>
</tr>
</tbody>
</table>

![Diagram showing the period from one rising edge to the next rising edge of the measured pulse is measured.]

Figure 3.2 Pin Used

3.2 Memory Usage

Table 3.2 Memory Usage

<table>
<thead>
<tr>
<th>Memory Usage</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>246 bytes</td>
<td>In main.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>5 bytes</td>
<td>In main.c module</td>
</tr>
<tr>
<td>Maximum user stack usage</td>
<td>10 bytes</td>
<td>main function: 7 bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>timer_ra_init function: 3 bytes</td>
</tr>
<tr>
<td>Maximum interrupt stack usage</td>
<td>18 bytes</td>
<td>TRA_int function: 18 bytes</td>
</tr>
</tbody>
</table>

Memory usage varies depending on the C compiler version and the compile option. The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
- Compile option: -c -finfo; NOTE: -dir "$(CONFIGDIR)" -R8C
  NOTE: Unavailable in the R8C/Tiny-exclusive free version.
4. Setup

This section shows the initial setting procedures and values to perform the example described in 3. Application Example Description. Refer to the R8C/25 Group Hardware Manual for details on individual registers.

4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

PRCR [Address 000Ah]

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

CM1 [Address 0007h]

CM14 Low-speed on-chip oscillator oscillation stop bit
Low-speed on-chip oscillator oscillates

(3) Set the division ratio of the high-speed on-chip oscillator clock.

High-Speed On-Chip Oscillator Control Register 2

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

FRA2 [Address 0025h]

FRA22 to FRA20 High-speed on-chip oscillator frequency switch bit
Divide-by-2 mode

(57-53) Reserved bits
Set to 0.

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

FRA0 [Address 0023h]

FRA00 High-speed on-chip oscillator enable bit
High-speed on-chip oscillator oscillates
(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

![High-Speed On-Chip Oscillator Control Register 0](image)

(7) Set system clock division select bits 1.

![System Clock Control Register 1](image)

(8) Set system clock division select bit 0.

![System Clock Control Register 0](image)

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

![Protect Register](image)
4.2 Pulse Period Measurement Mode Setting

(1) Set the port P1 direction register.

Port P1 Direction Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD1</td>
<td>[Address 00E3h]</td>
</tr>
<tr>
<td>PD1_7</td>
<td>Port P1_7 direction bit</td>
</tr>
<tr>
<td>Input mode</td>
<td></td>
</tr>
</tbody>
</table>

(2) Stop the timer RA count.

Timer RA Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRACR</td>
<td>[Address 0100h]</td>
</tr>
<tr>
<td>TSTART</td>
<td>Timer RA count start bit</td>
</tr>
<tr>
<td>Count stops</td>
<td></td>
</tr>
</tbody>
</table>

(3) Wait until the TCSTF bit in the TRACR register is set to 0.

(4) Set the timer RA interrupt control register (timer RA interrupt disabled).

Timer RA Interrupt Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAIC</td>
<td>[Address 0056h]</td>
</tr>
<tr>
<td>ILVL2 to ILVL0</td>
<td>Interrupt priority level select bits 2 to 0</td>
</tr>
<tr>
<td>Level 0 (interrupt disabled)</td>
<td></td>
</tr>
<tr>
<td>IR</td>
<td>Interrupt request bit</td>
</tr>
<tr>
<td>No interrupt request</td>
<td></td>
</tr>
<tr>
<td>(b7-b4)</td>
<td>Nothing is assigned.</td>
</tr>
<tr>
<td>Set to 0.</td>
<td></td>
</tr>
</tbody>
</table>

(5) Forcibly stop the timer RA count.

Timer RA Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRACR</td>
<td>[Address 0100h]</td>
</tr>
<tr>
<td>TSTOP</td>
<td>Timer RA count forcibly stop bit</td>
</tr>
<tr>
<td>Count forcibly stopped</td>
<td></td>
</tr>
</tbody>
</table>
(6) Set the timer RA prescaler register.

Timer RA Prescaler Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

TRAPRE [Address 0103h]
Timer RA underflow period setting
25 – 1 (0 x 18) setting

(7) Set the timer RA register.

Timer RA Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TRA [Address 0104h]
Timer RA register initial value setting
0xFF setting

(8) Set the timer RA control register.

Timer RA Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TRACR [Address 0100h]

- **TSTART** Timer RA count start bit
  - Count stops
- **TCSTF** Timer RA count status flag
  - Unavailable. Set to 0.
- **TSTOP** Timer RA count forcible stop bit
  - Unavailable. Set to 0.
- **(b3)** Nothing is assigned.
  - Set to 0.
- **TEDGF** Timer RA edge judgment flag
  - No active edge
- **TUNDF** Timer RA underflow flag
  - No underflow
- **(b7-b6)** Nothing is assigned.
  - Set to 0.
(9) Set the timer RA I/O control register.

Timer RA I/O Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **TRAIOC** [Address 0101h]  
  - TEDGSEL  
    - **TRAIO** polarity switch bit  
      - The period from one rising edge to the next rising edge of the measured pulse is measured.

- **TOPCR**  
  - **TRAIO** output control bit  
    - Set to 0 in pulse period measurement mode.

- **TOENA**  
  - **TRAIO** output enable bit  
    - Set to 0 in pulse period measurement mode.

- **TIOSEL**  
  - **INT1/TRAIO** select bit  
    - **INT1/TRAIO** pin (P1_7)

- **TIPF1 and TIPF0**  
  - **TRAIO** input filter select bits  
    - No filter  
    - Set to 0.

(10) Set the timer RA mode register.

Timer RA Mode Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **TRAMR** [Address 0102h]  
  - **TMOD2 to TMOD0**  
    - Timer RA operating mode select bits  
      - Pulse period measurement mode

- **TCK2 to TCK0**  
  - Timer RA count source select bit  
    - f8 selected

- **TCKCUT**  
  - Timer RA count source cutoff bit  
    - Count source provided
(11) Set the timer RA interrupt control register.

Timer RA Interrupt Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TRAIC  [Address 0056h]
- ILVL2 to ILVL0: Interrupt Priority Level Select Bits 2 to 0
- IR: Interrupt request bit
  - No interrupt request
  - Set to 0.

(12) Start the timer RA count.

Timer RA Control Register

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

TRACR  [Address 0100h]
- TSTART: Timer RA count start bit
  - Count starts

(13) Wait until the TCSTF bit in the TRACR register is set to 1.

(14) Immediately after the count starts, allow two cycles or more of the timer RA prescaler.
(15) Set the TEDGF bit in the TRACR register to 0 before use.

**NOTE:**
In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. Write 1 to bits TEDGF and TUNDF to avoid their values being changed.
5. Flowchart

5.1 Main Function

5.1.1 Main Function 1

```
main()
asm("FCLR I")
prc0 ← 1
cm14 ← 0
fra2 ← 0x00
fra00 ← 1
Repeat
(i <= 255)
  i++;
  fra01 ← 1
  cm16 ← 0
  cm17 ← 0
  cm06 ← 0
  prc0 ← 0
Timer RA SFR initial setting processing
timer_ra_init()
asm("FSET I")
```

- Disable interrupts
- Disable system control register protect
- Start the low-speed on-chip oscillator
- High-speed on-chip oscillator clock: Divide-by-2 mode
- Start the high-speed on-chip oscillator
- Wait until oscillation stabilizes
- Select the high-speed on-chip oscillator
- No system clock division
- Enable CM16 and CM17
- Enable system control register protect
- Timer RA associated SFR initial setting processing (pulse period measurement mode)
- Enable interrupts
5.1.2 Main Function 2

1

f_edge = 1?

Yes

Check the active edge

No

undf_cnt = 0?

Yes

Check the underflow

No

measurement_value ← 0xFF − present_tra

measurement_value ← 0x0100 * undf_cnt + 0xFF − present_tra

undf_cnt ← 0

Clear the underflow counter

f_capture ← 0

Clear the edge flag

Calculate the measurement value
5.2 Timer RA Associated SFR Initial Setting Processing

- timer_ra_init()
  - pd1 ← pd1&0x7F
  - tstart_tracr ← 0
    - tcstf_tracr = 0?
      - traic ← 0x00
      - tstop_tracr ← 1
      - trapre ← 25 − 1
      - tra ← 0xFF
      - tracr ← 0x00
      - traioc ← 0x00
      - traioc ← 0x14
      - traic ← 0x07
      - tstart_tracr ← 1
        - tcstf_tracr = 1?
          - Repeat (i <= 255)
            - i++;
          - tracr ← 0x21
          - return
    - Stop timer RA operation
      - Timer RA interrupt: Interrupt level 0 (interrupt disabled)

  - Initialize registers TRAPRE and TRA, and bits TSTART and TCSTF in the TRACR register
  - Underflow period: Set to 10 μs (40 MHz ⨉ f2 ⨉ f8 ⨉ 25 = 10 μs)
  - TRA: Set to 0xFF
  - TEDGF: Set to no active edge; TUNDF: Set to no underflow
  - Count at the rising edge of the TRAIO input
  - Select the INT1/TRAIO pin (P1_7)
  - TRAIO input filter: No filter
  - Select pulse period measurement mode
  - Count source: Set to f8
  - Provide the count source
  - Timer RA interrupt: Interrupt level 7
    - Start timer RA operation
      - Wait for two or more cycles of the timer RA prescaler
      - Set 0 to tedgf_tracr

- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
- P1_7(TRAIO) pin: Set to an input port
5.3 Timer RA Interrupt Handling

TRA_int()

```
if (tedgf_tracr != 0)
    Yes
    tracr ← 0x21
    present_tra ← tra
    f_edge ← 1

if (tundf_tracr != 0)
    Yes
    tracr ← 0x11
    undf_cnt ++
```

Any active edge?
Set 0 to both tedgf_tracr and tundf_tracr
Read tra
Set the edge flag
Any underflow?
Set 1 to tedgf_tracr and 0 to tundf_tracr
Increment the underflow counter

return
6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Series page.

7. Reference Documents

Hardware Manual
R8C/25 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.
<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Sep 15, 2006</td>
<td>−</td>
<td>First Edition issued</td>
</tr>
<tr>
<td>2.00</td>
<td>June 29, 2007</td>
<td>2 to 4</td>
<td>3. Application Example Description modified</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 to 11</td>
<td>4. Setup SFR setting procedures added</td>
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<tr>
<td></td>
<td></td>
<td>12</td>
<td>5.1.1 Main Function 1 Oscillation stabilization processing added</td>
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<td></td>
<td></td>
<td>13</td>
<td>5.1.2. Main Function 2 Pulse period measurement calculation processing added</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14</td>
<td>5.2 Timer RA Associated SFR Initial Setting Processing modified</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>5.3 Timer RA Interrupt Handling added</td>
</tr>
</tbody>
</table>
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