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## R8C/25 Group

### Timer RA in Event Counter Mode

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#### 1. Abstract

This document describes how to set up and use the timer RA in event counter mode on the R8C/25 Group device.

#### 2. Introduction

The application example described in this document is applied to the following:

- MCU: R8C/25 Group

This program can be used with other R8C/Tiny Series which have the same SFR (special function register) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

### 3. Applications

#### 3.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA.

Figure 3.1 shows a Block Diagram of Timer RA.

Time RA has the following five modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses of which polarity inverted by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

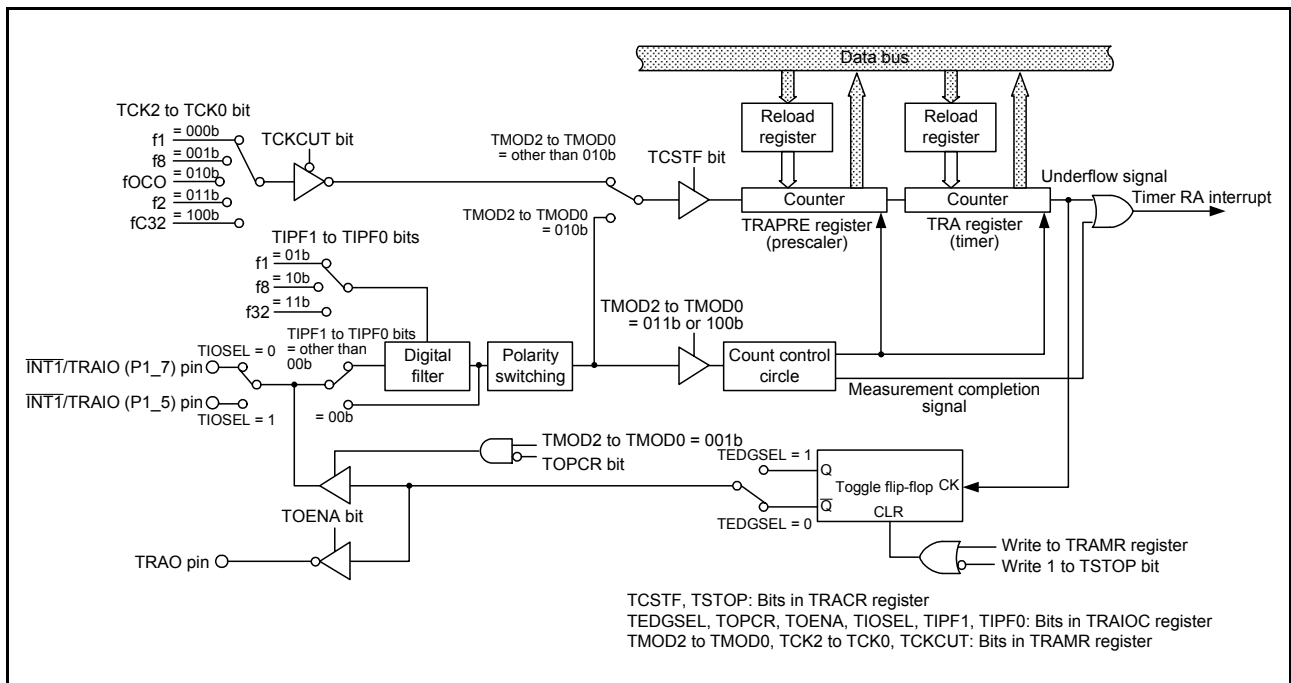


Figure 3.1 Block Diagram of Timer RA

### 3.2 Event Counter Mode

In this mode, external signal inputs to the  $\overline{\text{INT1}}$ /TRAIO pin are counted (refer to Table 3.1). Figure 3.2 shows Registers TRACR and TRAIOC in Event Counter Mode, and Figure 3.3 shows Registers TRAMR, TRAPRE, and TRA in Event Counter Mode. (Refer to the R8C/25 Group Hardware Manual for detail about each register.)

Table 3.1 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	<ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer underflows, the contents of the reload register are reloaded and the count is continued.</li> </ul>
Divide ratio	$1/(n+1)(m+1)$ n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	<ul style="list-style-type: none"> <li>0 (count stops) is written to the TSTART bit in the TRACR register.</li> <li>1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>
Interrupt request generation timing	<ul style="list-style-type: none"> <li>When timer RA underflows [timer RA interrupt].</li> </ul>
$\overline{\text{INT1}}$ /TRAIO pin function	Count source input ( $\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port or pulse output <sup>(1)</sup>
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	<ul style="list-style-type: none"> <li>When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRAPRE and TRA are written during the count, values are written to the reload register at the next count source input timing and are transferred to the counter at the second count source input timing. The count restarts at the third count source input timing.</li> </ul>
Select functions	<ul style="list-style-type: none"> <li><math>\overline{\text{INT1}}</math>/TRAIO input polarity switch function The TEDGSEL bit in the TRAIOC register selects the active edge of the count source.</li> <li>Count source input pin select function The TIOSEL bit in the TRAIOC register selects <math>\overline{\text{INT1}}</math>/TRAIO (P1_7) or <math>\overline{\text{INT1}}</math>/TRAIO (P1_5) as an <math>\overline{\text{INT1}}</math>/TRAIO pin.</li> <li>Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register).</li> <li>Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.</li> </ul>

NOTE:

- The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

Timer RA Control Register

Symbol		Address		After Reset			
TRACR		0100h		00h			
Bit Symbol	Bit Name	Function		RW			
TSTART	Timer RA count start bit <sup>(1)</sup>	1: Count starts		RW			
TCSTF	Timer RA count status flag <sup>(1)</sup>	1: During count		RO			
TSTOP	Timer RA count forcible stop bit <sup>(2)</sup>	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.		RW			
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—			
TEDGF	Active edge judgment flag	Set to 0 in event counter mode.		RW			
TUNDF	Timer RA underflow flag	Set to 0 in event counter mode.		RW			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—			

NOTES:

1. Refer to **3.3 Notes on Timer RA** for notes on bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TPAPRE and TRA are set to the values after a reset.

Timer RA I/O Control Register

Symbol		Address		After Reset			
TRAIOC		0101h		00h			
Bit Symbol	Bit Name	Function		RW			
TEDGSEL	TRAI O polarity sw itch bit	0: Starts counting at rising edge of the TRAI O input or TRAI O starts output at low		RW			
TOPCR	TRAI O output control bit	Set to 0 in event counter mode.		RW			
TOENA	TRAI O output enable bit	0: Port P3_0		RW			
TIOSEL	INT1/TRAI O select bit	0: INT1/TRAI O pin (P1_7)		RW			
TIPF0	TRAI O input filter select bits <sup>(1)</sup>	b5 b4 0 0: No filter		RW			
TIPF1							
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—			

NOTE:

1. When the same value from the TRAI O pin is sampled three times continuously, the input is determined.

Figure 3.2 Registers TRACR and TRAI OC in Event Counter Mode

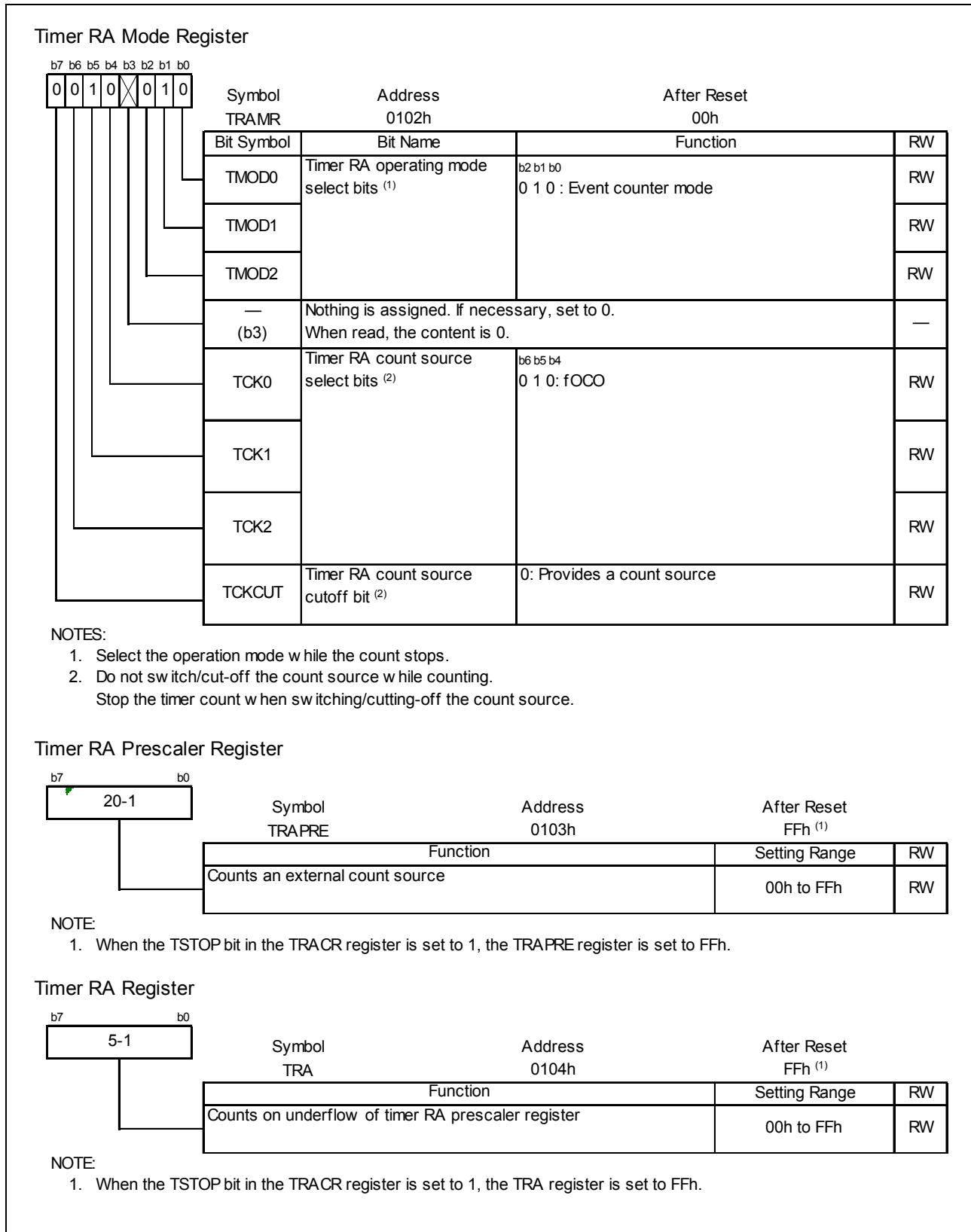


Figure 3.3 Registers TRAMR, TRAPRE, and TRA in Event Counter Mode

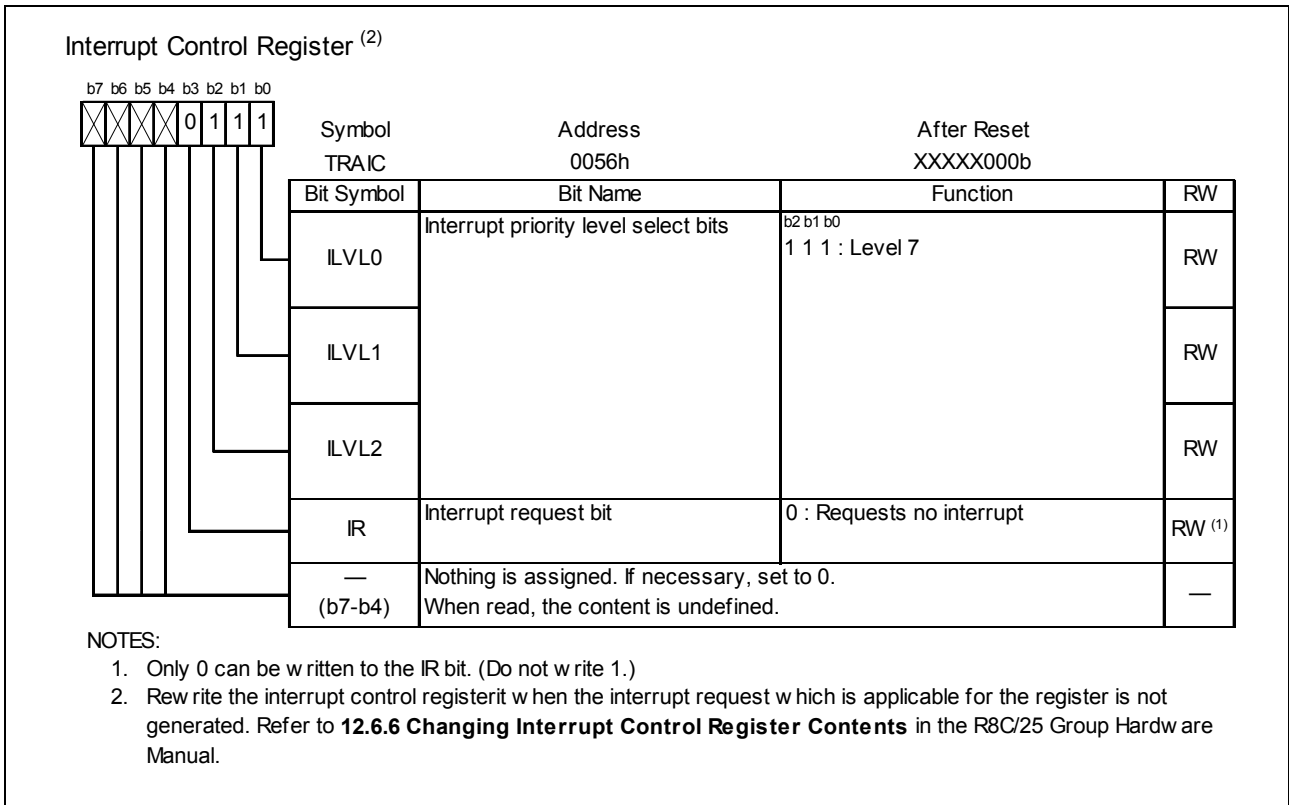


Figure 3.4 Registers TRAIC in Event Counter Mode (Using Interrupt)



### 3.3 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

During this time, do not access registers associated with timer RA<sup>(1)</sup> other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count). The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress.

During this time, do not access registers associated with timer RA<sup>(1)</sup> other than the TCSTF bit. Timer RA counting is stopped when the TCSTF bit is set to 0.

NOTE:

1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

## 4. Program Overview

When the count start bit is set to 1, external signals input to the TRAIO pin are counted.  
This program uses the following functions:

- Select the  $\overline{\text{INT1}}$ /TRAIO pin (P1\_7).
- Count at the rising edge of the TRAIO input.
- Disable the TRAIO input filter.
- After counting 100, underflow.  

$$100 = (\text{TRAPRE register setting value} + 1) \times (\text{TRA register setting value} + 1)$$

$$= (19 + 1) \times (4 + 1)$$
- TRA0 pin function: set the programmable I/O port (the TRAIO output is not invert output).

Figure 4.1 shows the Pins Used.

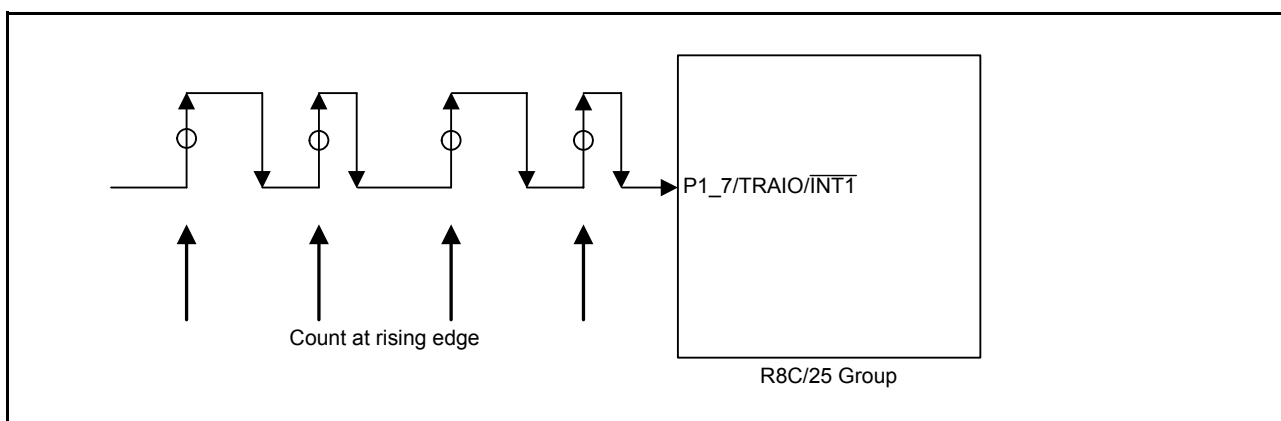


Figure 4.1 Pins Used

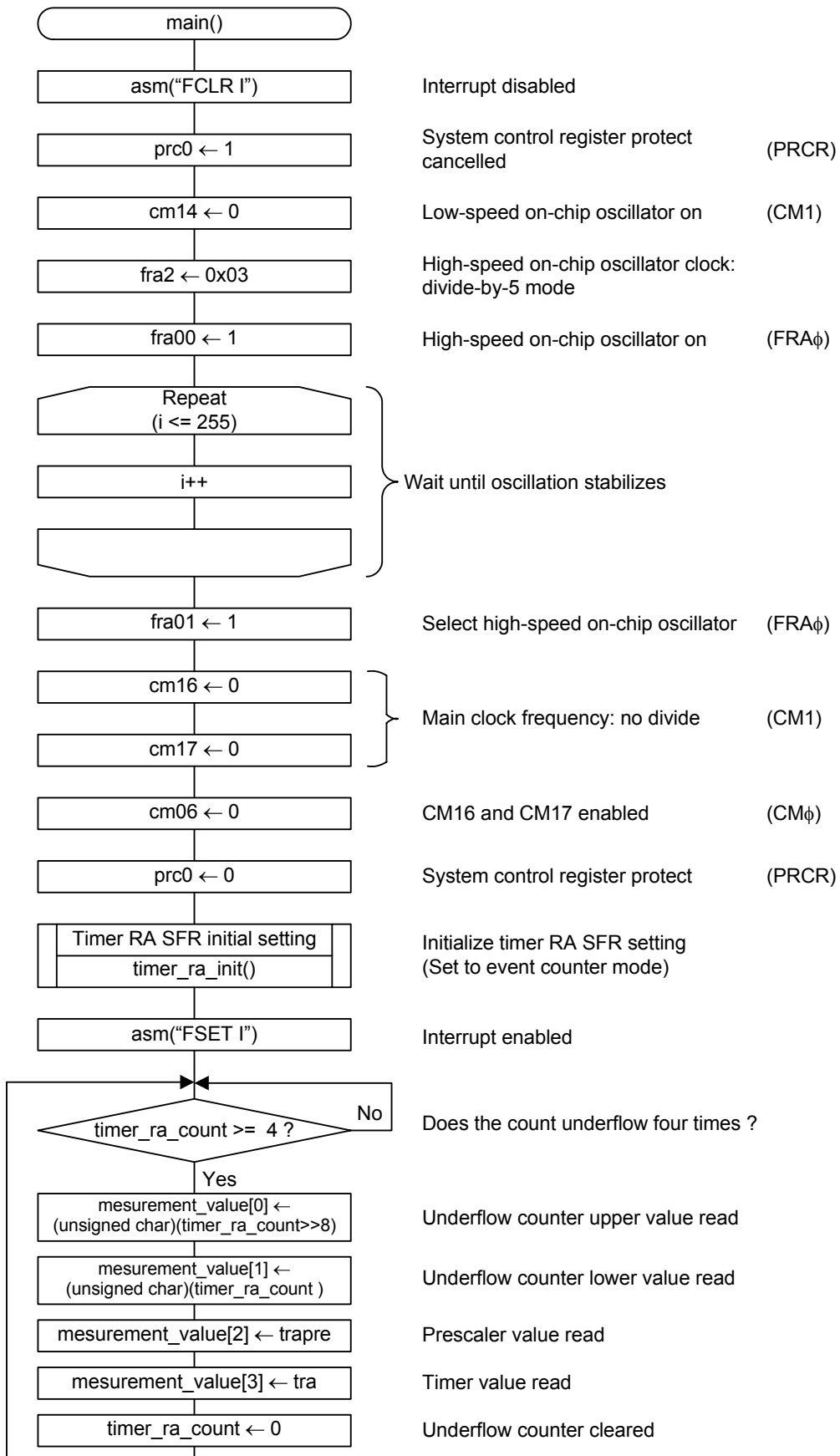
### 4.1 Function Table

Declaration	void timer_ra_init(void)		
Overview	SFR initial setting associated with timer RA		
Argument	Argument name	Meaning	
	None		
Variable used (global)	Variable name	Usage	
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with time RA		

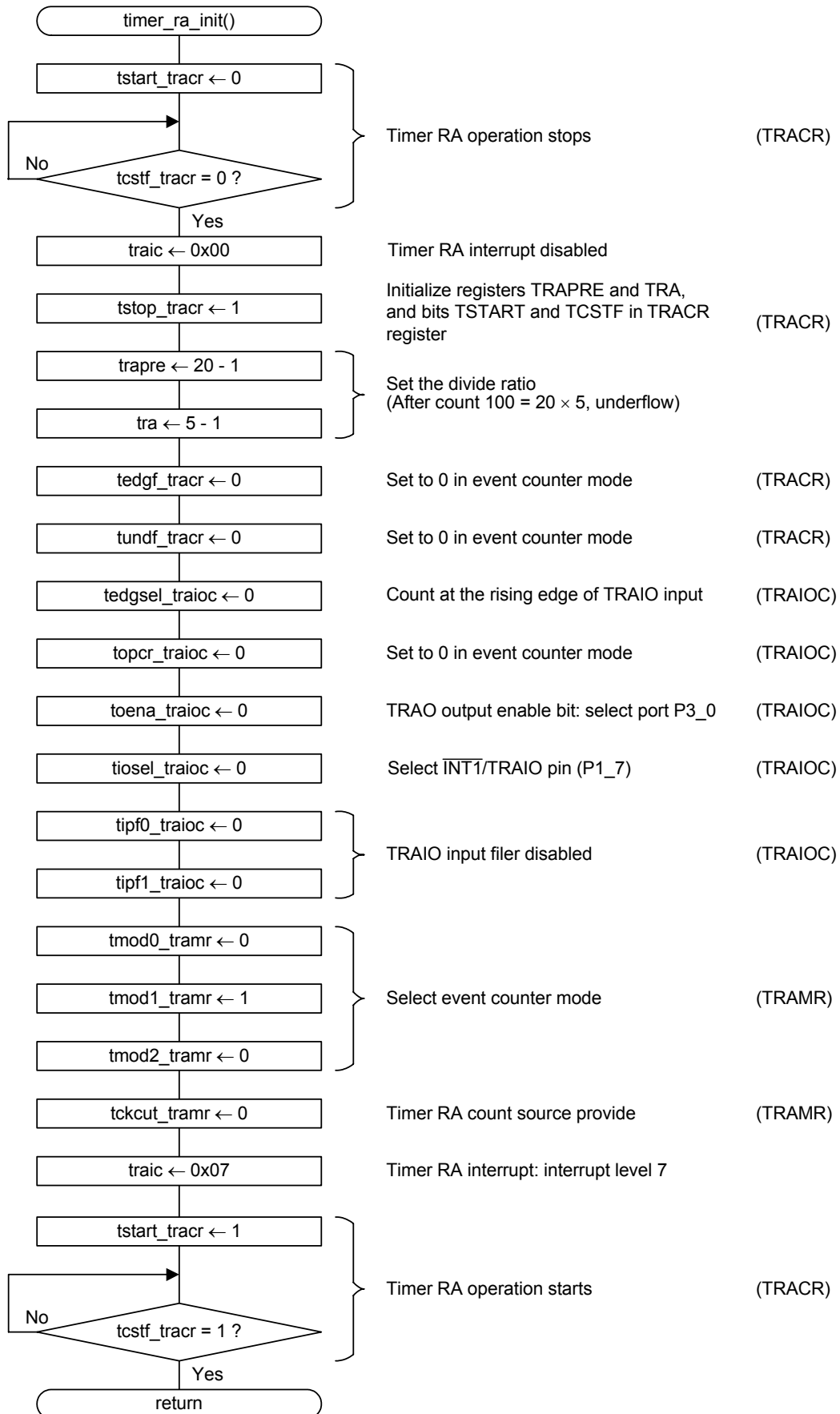
Declaration	void TRA_int(void)		
Overview	Timer RA interrupt		
Argument	Argument name	Meaning	
	None		
Variable used (global)	Variable name	Usage	
	None		
Return value	Type	Value	Meaning
	None		
Function	Perform event counter interrupt of timer RA		

4.2 Flow Chart

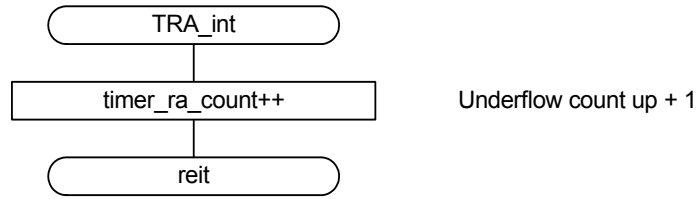
4.2.1 Main Functions



4.2.2 Timer RA SFR Initial Setting



4.2.3 Timer RA Interrupt



## 5. Sample Programming Code

Download a sample program from the Renesas Technology website.  
To download, click “Application Notes” in the left-hand side menu on the top page of the R8C/Tiny Series.

## 6. Reference Document

Hardware Manual

R8C/25 Group Hardware Manual  
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REVISION HISTORY	R8C/25 Group Timer RA in Event Counter Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	-	First Edition issued
2.00	Nov 10, 2008	2	Figure 3.1 TSTART → TCSTF
		3	Table 3.1 Event Counter Mode Specifications revised
		4	Figure 3.2 Registers TRACR and TRAI0C in Event Counter Mode revised
		5	Figure 3.3 Registers TRAMR, TRAPRE, and TRA in Event Counter Mode revised
		6	Figure 3.4 Registers TRAIC in Event Counter Mode (Using Interrupt) added
		7	3.3 Notes on Timer RA revised
		8	4.1 Function table of timer RA interrupt added
		9	4.2.1 Main Functions flowchart revised
		10	4.2.2 Timer RA SFR Initial Setting flowchart revised
		11	4.2.3 Timer RA Interrupt flowchart added
		-	3.3 Timer Write Control during Count Operation (p6 in Rev.1.00) deleted
		-	Sample program revised

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