R32C/100 Series

Timer A Operation Using a Two-phase Pulse Signal and Normal Processing in Event Counter Mode

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Abstract

This document describes timer A operation using a two-phase pulse signal and normal processing in event counter mode with the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

When using the event counter mode of timer A2, the timer counts a two-phase pulse signal applied to pins TA2IN and TA2OUT using normal processing. When an overflow or underflow occurs, a high is output from the corresponding port.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Overview of Normal Processing.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer A (timer A2)	Counts a two-phase pulse signal applied to pins TA2IN and TA2OUT

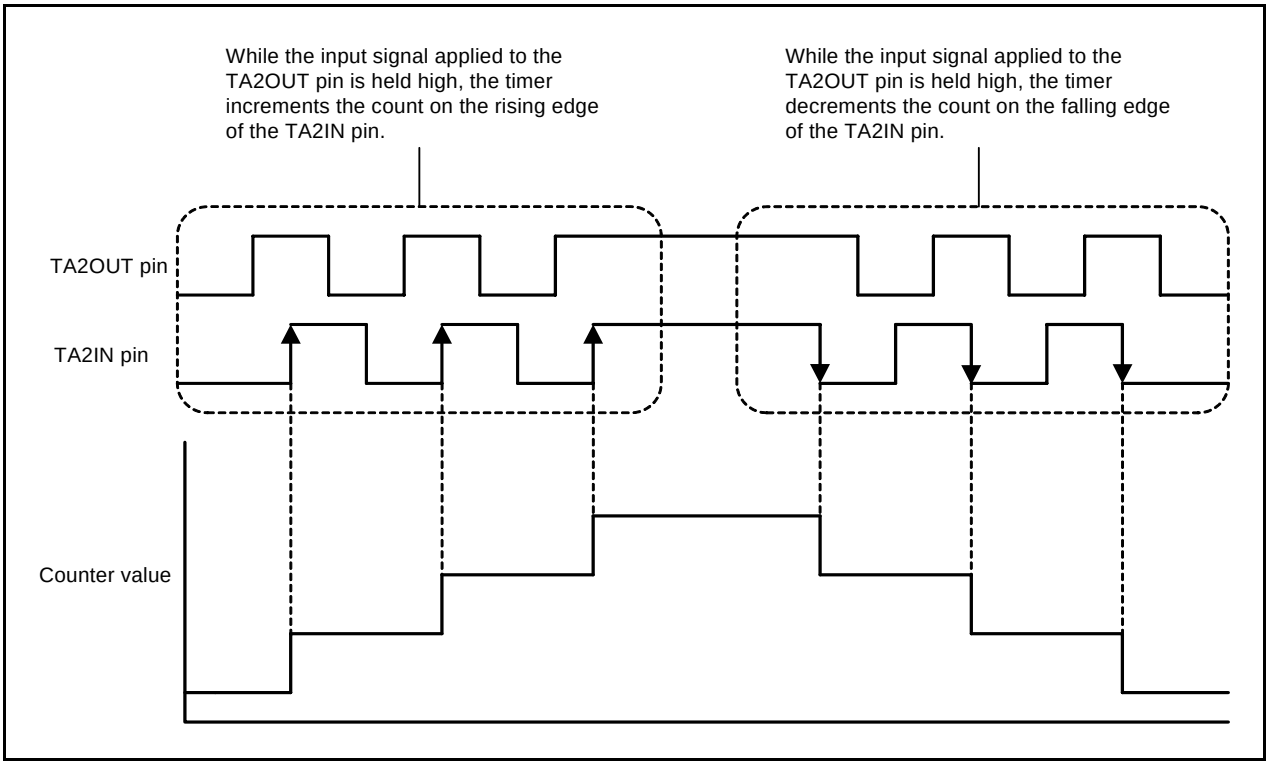

Figure 1.1 Overview of Normal Processing

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	Main clock: 16 MHz PLL clock: 100 MHz Base clock: 50 MHz CPU clock: 50 MHz Peripheral bus clock: 25 MHz Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P7_4/TA2OUT	Input	Two-phase pulse input of timer A2
P7_5/TA2IN	Input	Two-phase pulse input of timer A2
P4_0	Output	Output to confirm counter overflow
P4_1	Output	Output to confirm counter underflow

5. Software

5.1 Operation Overview

The timer counts a two-phase pulse signal applied to pins TA2IN and TA2OUT. If the counter overflows or underflows, a timer A2 interrupt is generated.

(1) Timer A2 initial settings
Table 5.1 and Table 5.2 list the Timer A2 Settings and Initial Pin Settings to Confirm Overflow or Underflow, respectively.

Table 5.1 Timer A2 Settings

Item	Contents
Operating mode	Event counter mode
Two-phase processing operation	Normal processing operation
Count operation type	Free-running type

Table 5.2 Initial Pin Settings to Confirm Overflow or Underflow

Pin	Initial Value
P4_0 (output to confirm overflow)	0
P4_1 (output to confirm underflow)	0

(2) Timer A2 count starts
Set the timer A2 count start bit in the count start register to 1 (start counter).

(3) When the counter overflows or underflows
When the counter overflows or underflows, the interrupt request flag of timer A2 becomes 1 (interrupt requested). The counter continues counting without reloading the value in the reload register.
In the timer A2 interrupt handler, set each pin as output to confirm overflow or underflow.
Table 5.3 lists the Setting Pins as Output to Confirm Overflow or Underflow.

Table 5.3 Setting Pins as Output to Confirm Overflow or Underflow

	Setting Value for Port P4_0	Setting Value for Port P4_1
When the counter overflows	0	1
When the counter underflows	1	0

Figure 5.1 shows the Operation Timing.

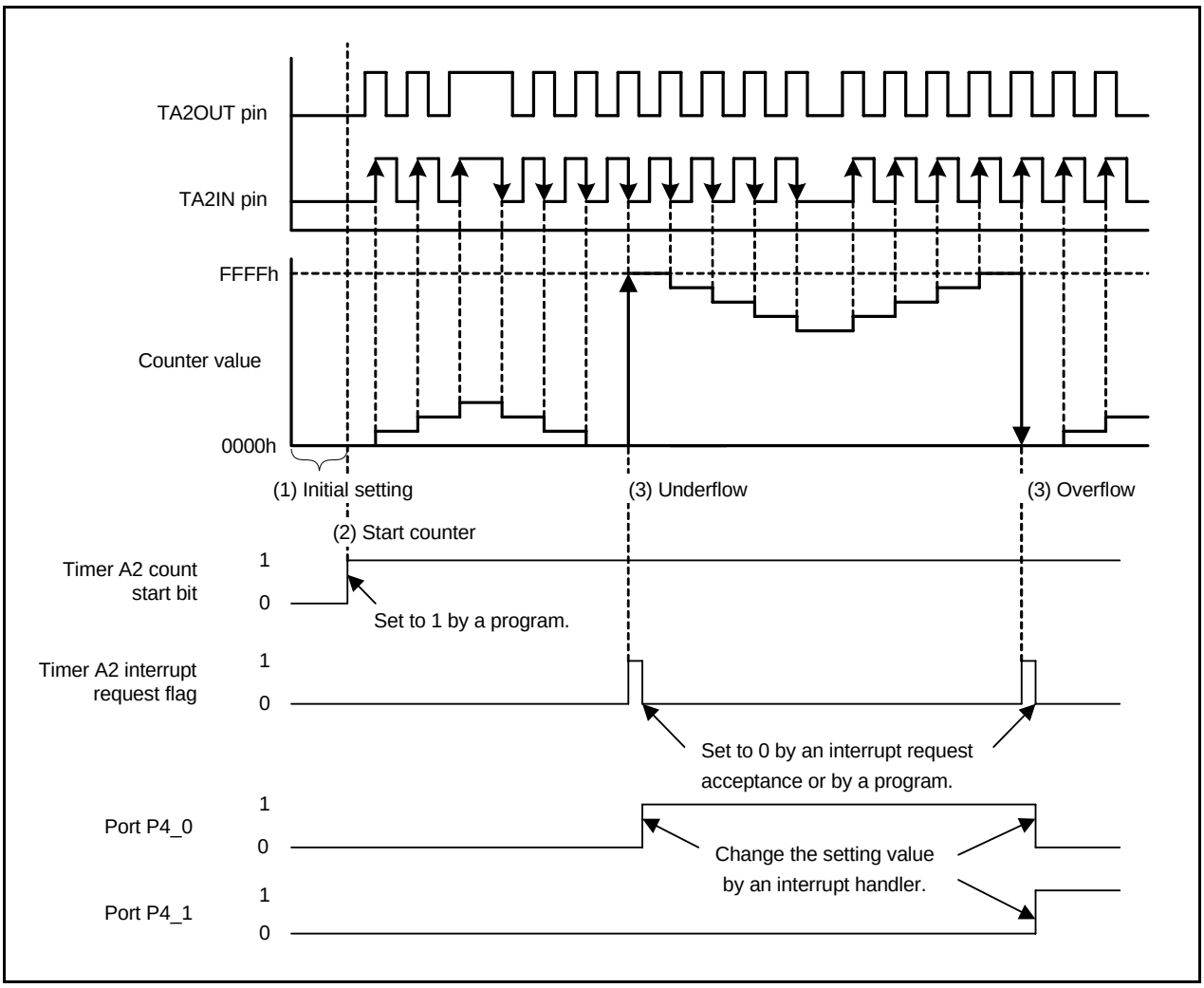

Figure 5.1 Operation Timing

5.2 Flowchart

5.2.1 Main Processing

Figure 5.2 and Figure 5.3 show Main Processing (1) and Main Processing (2), respectively.

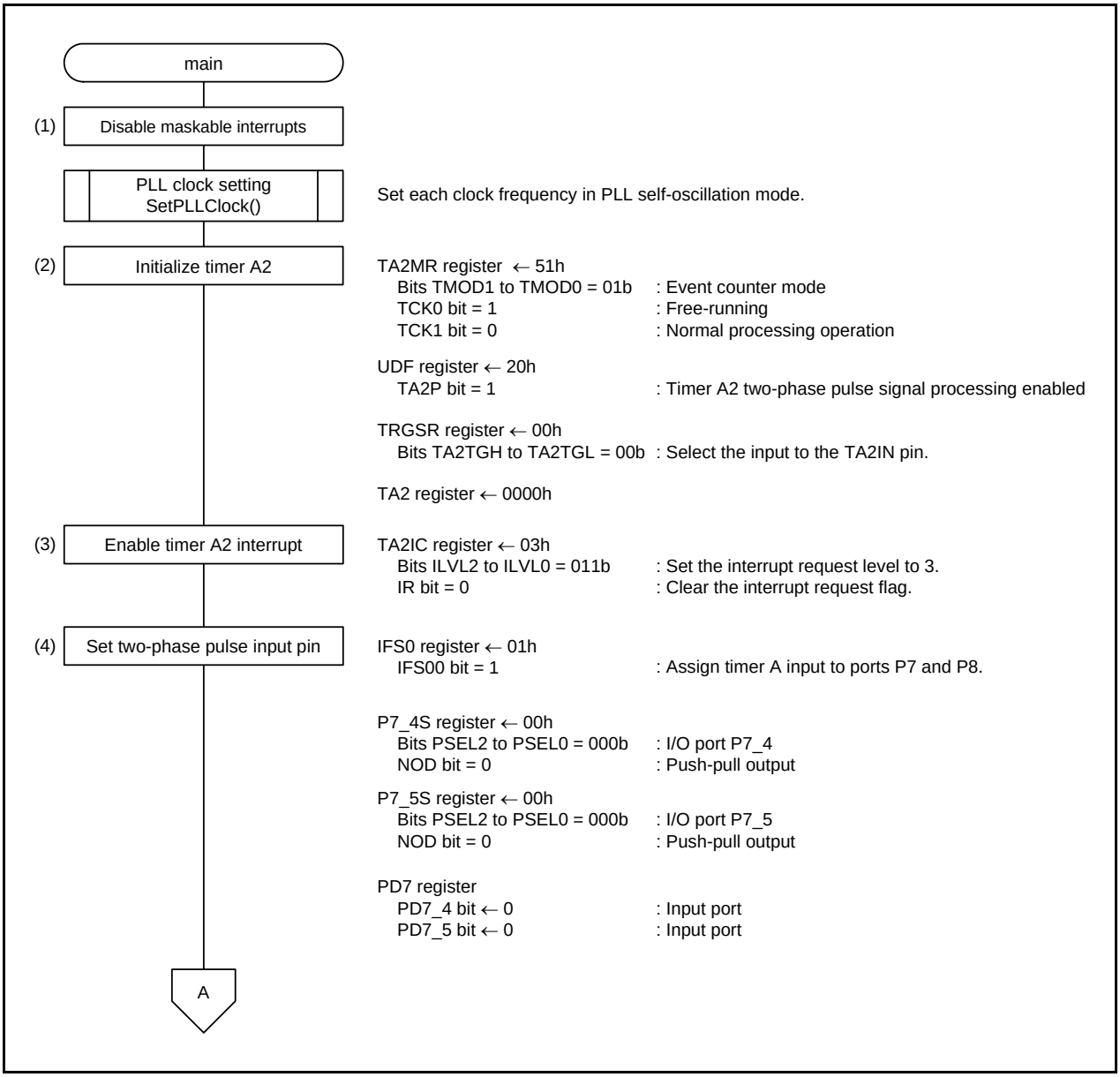

Figure 5.2 Main Processing (1)

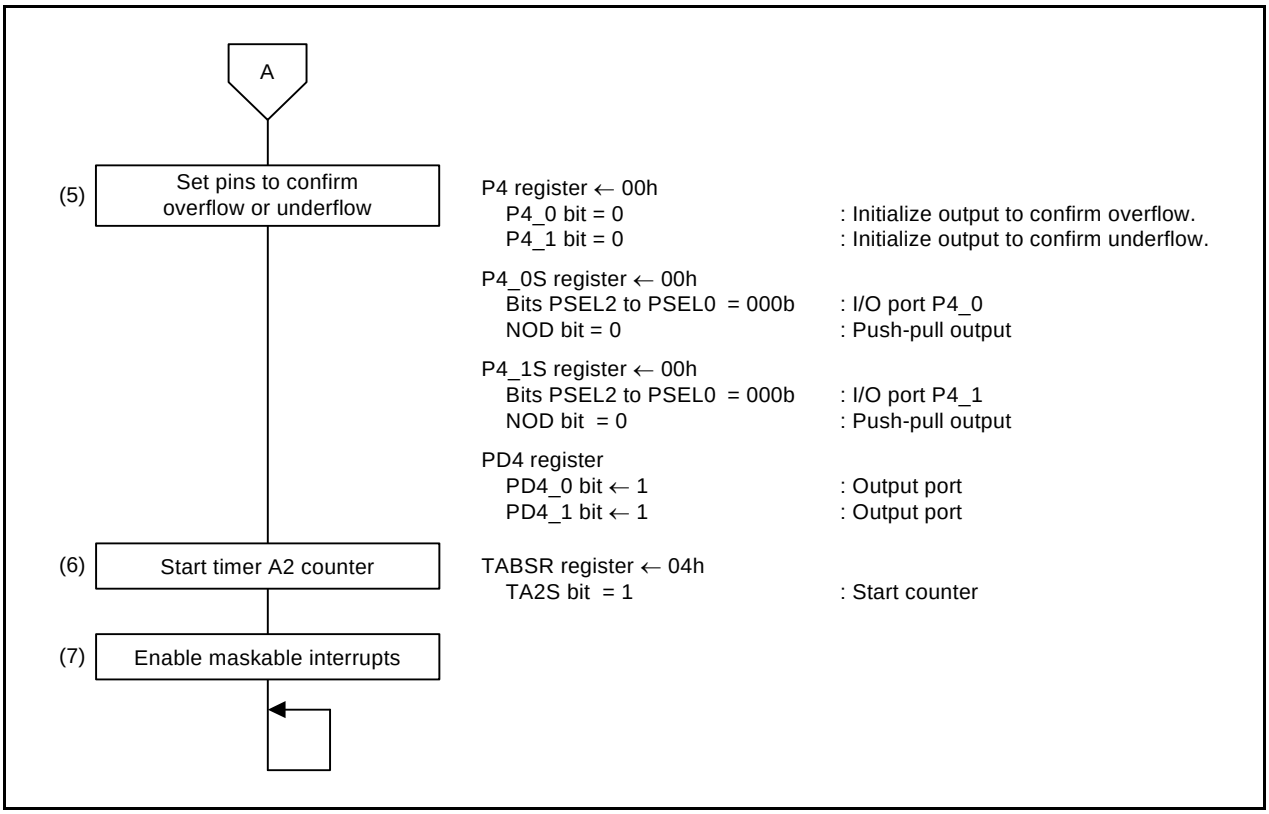

Figure 5.3 Main Processing (2)

5.2.2 Timer A2 Interrupt Handler

Figure 5.4 shows the Timer A2 Interrupt Handler.

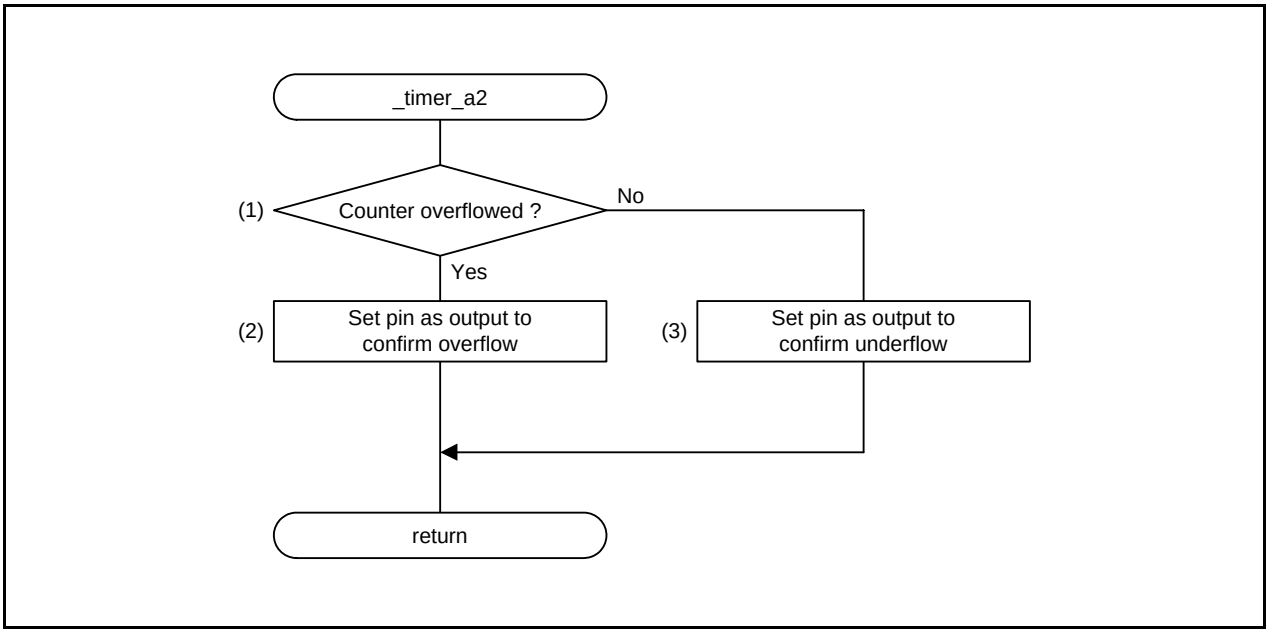

Figure 5.4 Timer A2 Interrupt Handler

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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Revision History	R32C/100 Series Timer A Operation Using a Two-phase Pulse Signal and Normal Processing in Event Counter Mode

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 14, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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