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M16C/63, 64A, 65 Group

Timer A Operation (Programmable Output Mode)

1. Abstract

This document describes timer A operation in the programmable output mode.

2. Introduction

The application example described in this document applies to the following MCUs:

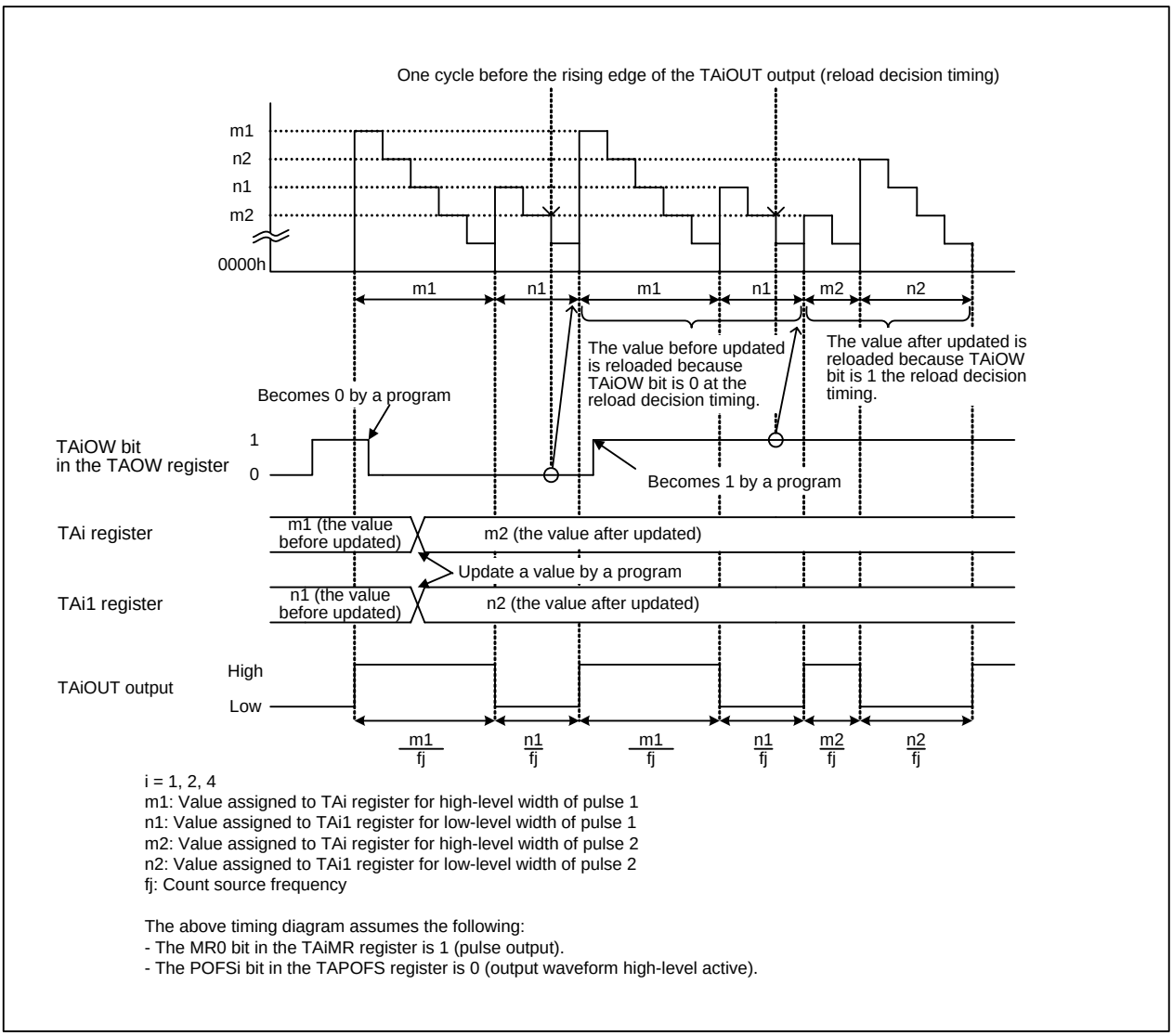
- MCUs: M16C/63 Group
  M16C/64A Group
  M16C/65 Group

Careful evaluation is recommended before using the program described in this application note.

3. Programmable Output Mode

In programmable output mode, the timer outputs arbitrary low- and high-level width of pulse successively. The mode can be used in timer A1, A2 and A4. The high-level width of pulse can be set in the TAi register (i = 1, 2 or 4), and the low-level width of pulse can be set in the TAi1 register.
To change cycles or width of the output waveform, follow the instructions below.
(1) Set the TAiOW bit to 0 (output waveform change disabled).
(2) Write to the TAi register and/or the TAi1 register.
(3) Set the TAiOW bit to 1 (output waveform change enabled).

The updated value is reloaded when the TAiOW bit is 1 (output waveform change enabled) at one cycle before the rising edge of the TAiOUT output (the falling edge when the POFSi bit is 1). The value before the update is reloaded when the TAiOW bit is 0 (output waveform change disabled). Figure 3.1 shows an example of programmable output.



i = 1, 2, 4
m1: Value assigned to TAi register for high-level width of pulse 1
n1: Value assigned to TAi1 register for low-level width of pulse 1
m2: Value assigned to TAi register for high-level width of pulse 2
n2: Value assigned to TAi1 register for low-level width of pulse 2
fj: Count source frequency

The above timing diagram assumes the following:
- The MR0 bit in the TAiMR register is 1 (pulse output).
- The POFSi bit in the TAPOFS register is 0 (output waveform high-level active).

Figure 3.1 Example of Programmable Output

4. Application Example

4.1 Explanation of the Sample Program

In the sample program, two different pulses (pulse A and B) are output alternately and successively using programmable output mode of timer A. Timer values are updated in the interrupt process of timer A. Sample output waveform is output on the following conditions.
Count source: 8 MHz
Output waveform: High-level active
High-level width of pulse A: 8 ms Low-level width of pulse A: 4 ms
High-level width of pulse B: 2 ms Low-level width of pulse B: 6 ms

Figure 4.1 shows the output waveform of the sample program.

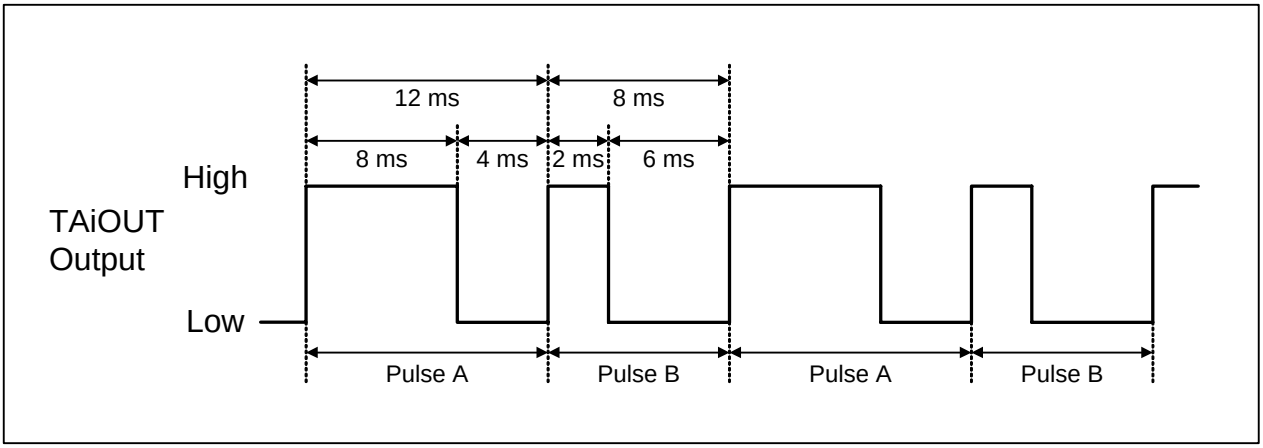


Figure 4.1 Output Waveform of the Sample Program

4.2 Configuration of the Sample Program

Table 4.1 lists the configuration of the application example.

Table 4.1 Configuration of the Application Example

Item	Specification	
Count source	√	Select from the following sources. f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fC32, fOCO-F(1), or fOCO-S
Output polarity	√	Output polarity high-level active
		Output polarity low-level active (output reversed)
Output waveform change		Change disabled
	√	Change enabled
Count trigger	√	Write 1 to the TAiS bit in the TABSR register
		Select by bits TAiTGH to TAiTGL

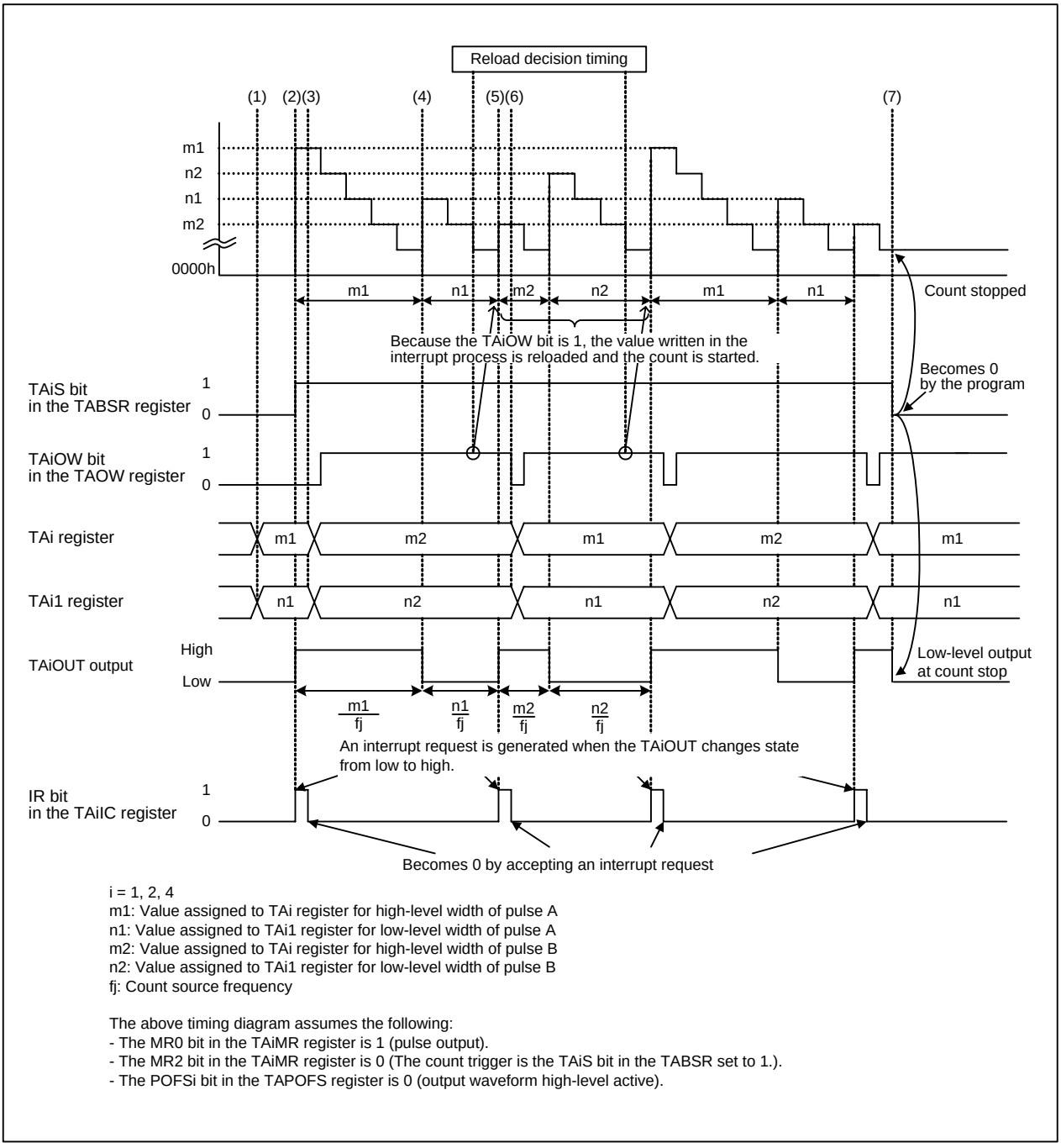
i = 1, 2, 4

Note:
1. Not available in the M16C/64A Group.

4.3 Operations of the Sample Program

(1) Timer Ai (i = 1, 2, 4) is set, a value of high-level width of pulse A (m1) is written in the TAi register and then a value of low-level width of pulse A (n1) is written in the TAi1 register.
(2) When the TAiS bit in the TABSR register is set to 1, the value of the TAi register is reloaded and the count is started. At the same time, the state of the TAiOUT pin is changed from low to high and then an interrupt request is generated.
(3) After the TAiOW bit is set to 0 in the interrupt process of timer Ai, a value of high-level width of pulse B (m2) in the TAi register and a value of low-level width of pulse B (n2) are written in the TAi1 register and then the TAiOW bit is set to 1.
(4) When the timer underflows, the value of the TAi1 register is reloaded and the count is continued. At the same time, the state of the TAiOUT pin is changed from high to low.
(5) When the timer underflows, the state of the TAiOUT pin is changed from low to high and an interrupt request is generated. Because the TAiOW bit is 1 at the reload decision timing, the values are reloaded after updated (m2, n2) and the count is started.
(When the TAiOW bit is 0, the values before updated (m1, n1) are reloaded and the count is started.)
(6) After the TAiOW bit is set to 0 in the interrupt process of timer Ai, a value of high-level width of pulse A (m1) in the TAi register and a value of low-level width of pulse A (n1) are written in the TAi1 register and then the TAiOW bit set to 1.
(7) When the TAiS bit is set to 0, the count is stopped and then low-level is output to the TAiOUT pin.

Figure 4.2 shows operation example in programmable output mode.



i = 1, 2, 4
m1: Value assigned to TAi register for high-level width of pulse A
n1: Value assigned to TAi1 register for low-level width of pulse A
m2: Value assigned to TAi register for high-level width of pulse B
n2: Value assigned to TAi1 register for low-level width of pulse B
fj: Count source frequency

The above timing diagram assumes the following:
- The MR0 bit in the TAiMR register is 1 (pulse output).
- The MR2 bit in the TAiMR register is 0 (The count trigger is the TAiS bit in the TABSR set to 1.).
- The POFSi bit in the TAPOFS register is 0 (output waveform high-level active).

Figure 4.2 Operation Example in Programmable Output Mode

5. Register Settings

Figure 5.1 and Figure 5.2 show procedure and value for setting register in programmable output mode of timer A1. Refer to a hardware manual of the MCU you use for more details on each register.

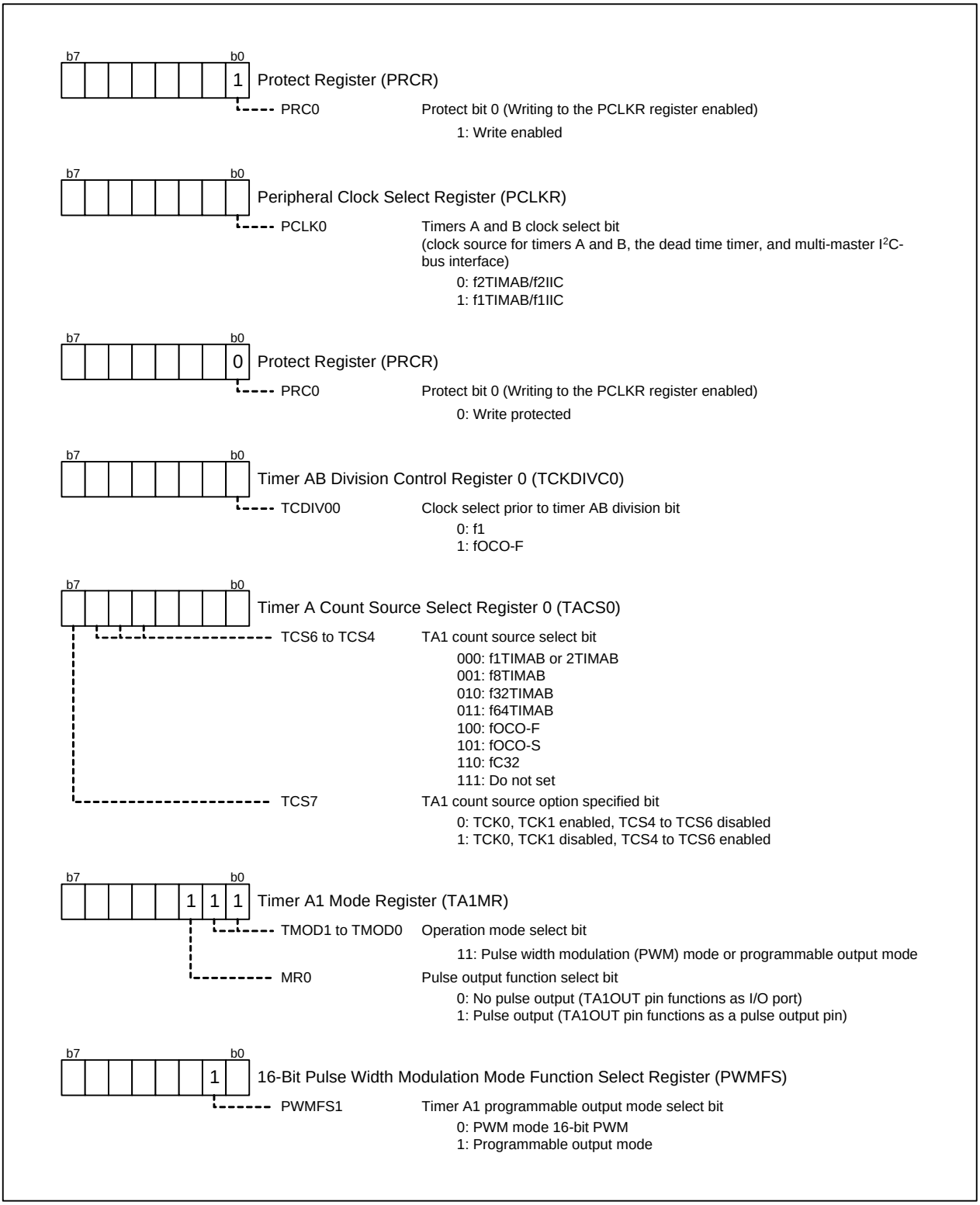


Figure 5.1 Procedure for Setting Register in Programmable Output Mode of Timer A (1/2)

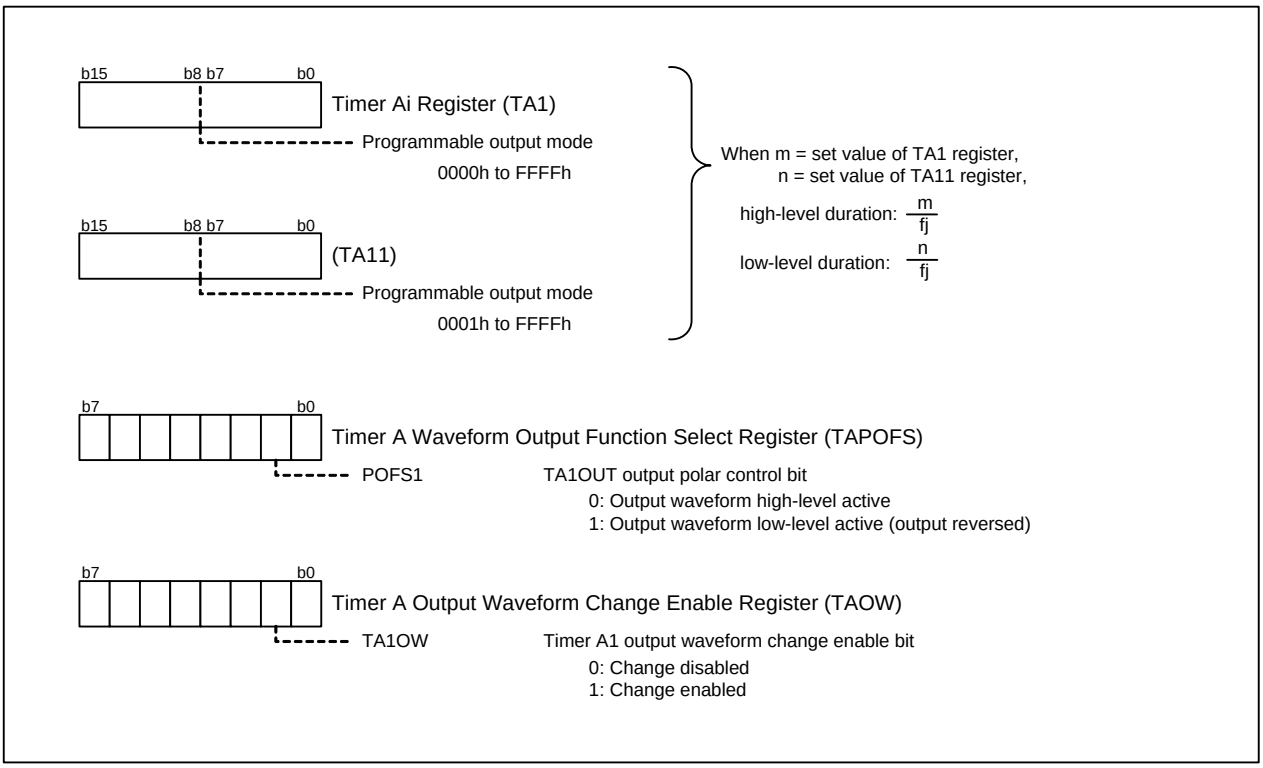


Figure 5.2 Procedure for Setting Register in Programmable Output Mode of Timer A (2/2)

6. Sample Program

A sample program can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

7. Reference Documents

Hardware Manual
M16C/63 Group Hardware Manual
M16C/64A Group Hardware Manual
M16C/65 Group Hardware Manual
The latest version of these documents can be downloaded from the Renesas Technology website.

Technical Update/Technical News
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		Page	Summary
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