1. **Abstract**

This document describes time measurement using the gate function of intelligent I/O groups 0 and 1.

2. **Introduction**

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

Intelligent I/O groups 0 and 1 each consist of one free-running 16-bit base timer and eight 16-bit registers (channels 0 to 7) for time measurement or waveform generation.

Two channels (channels 6 and 7) out of eight are equipped with the gate function for time measurement.

The gate function disables any trigger input to be accepted after time measurement by the first trigger input.

Figure 3.1 shows Time Measurement Using the Gate Function.

This section describes how to measure between the rising edge periods of an input signal to the IIO0_6 pin in the gate cleared state using time measurement channel 6.

Other conditions are as follows:

- Select the time measurement trigger: Both edges of the IIO0_6 pin
- Intelligent I/O group 0 input pin: Port P1
- Select gating: Gating enabled
- Base timer count source (fBT0): f1 (no division)
3.1 Timing

(1) When the BT0S bit in the BTSR register is set to 1, the group 0 base timer count starts.

(2) If a trigger input is applied to the IIO0_6 pin, a group 0 time measurement channel 6 (TM06) interrupt is generated. The value in the G0TM6 register is read in the interrupt handler for that interrupt. The difference from the value previously read is the time measurement. At the same time the interrupt is generated, the gating control signal is set to gating, and the trigger input applied to the IIO0_6 pin is invalid until the gating is cleared by a program.

(3) Set the GSC bit in the G0TMCR6 register to 1 (gating cleared) by a program.

Figure 3.2 shows an Operating Example of Time Measurement Function Using the Gate Function.

3.2 Notes on Intelligent I/O

If an interrupt is accepted, the IR bit in the IIOiIC register is automatically set to 0. However, even if an interrupt is accepted, each bit in the IIOiIR register is not automatically set to 0 (i = 0 to 11). They should be set to 0 by either the AND or BCLR instruction. Note that every generated interrupt request is ignored until these bits are set to 0.
3.3 Flowcharts

Figure 3.3 and Figure 3.4 show the Main Function, and Figure 3.5 shows Intelligent I/O Interrupt 6.

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main

(1) Disable maskable interrupts

(Note 1) SetPLLClock()

(2) G2BCR0 ← 7Fh
     BTSR ← 00h
     G2BCR0 ← 00h

(3) G0BCR0 ← 7Fh

(4) G0BCR1 ← 00h

(5) G0TMCR6 ← 11h

(6) G0FS ← 40h

(7) G0FE ← 40h

(8) Insert wait time

(9) IIO6IR ← 00h
     IIO6IE ← 01h (5)
     IIO6IC ← 03h (5)

1
```

**Notes:**
1. Refer to the hardware user's manual for initializing the clock.
2. The initial settings of bits and registers for the intelligent I/O are required as follows:
   - (1) Set the G2BCR0 register to provide the clock to the group 2 base timer.
   - (2) Set bits BT0S to BT2S to 0 (base timer is reset).
   - (3) Set other registers associated with the intelligent I/O.
   The BTiS bit allows the base timers of two or all groups to start counting simultaneously (i = 0 to 2).
   To start counting individually, the BTiS bit should be set to 0 and the BTS bit in the GiBCR1 register should be used.
3. Write 1 to bits 1 to 4, 6, and 7 after setting the IRLT bit in the IIO1IE register to 1.

**Figure 3.3 Main Function (1/2)**
Enable maskable interrupts

Set the group 0 base timer control register.
Count source: f1
Count source divide ratio: No division
Base timer interrupt source: Overflow of bit 15 or bit 9

Set the II00_6 pin.

Set the IIO0_6 pin.

Assign the IIO0 input to port P1.

Start the base timer count.

Wait time to periodically disable gating
Clear gating.

Figure 3.4  Main Function (2/2)

Figure 3.5  Intelligent I/O Interrupt 6
4. **Sample Program**

A sample program can be downloaded from the Renesas Electronics website.

5. **Reference Documents**

User’s Manuals
- R32C/116 Group User’s Manual: Hardware  Rev.1.00
- R32C/117 Group User’s Manual: Hardware  Rev.1.00
- R32C/118 Group User’s Manual: Hardware  Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
- R32C/100 Series C Compiler Package V.1.02 C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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## REVISION HISTORY

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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