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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M32C/82,83 Group

Time measurement function of Intelligent I/O group 0,1 with gate function

1. Abstract

This application note describes the timer measurement function of intelligent I/O group 0 with gate function.

2. Introduction

This application note is applied to the M32C/83 group microcomputer.

This program can also be used when operating other microcomputers within M16C family, provided they have the same SFR (Special Function Registers) as the M32C/83 group. However, some functions may have been modified. Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

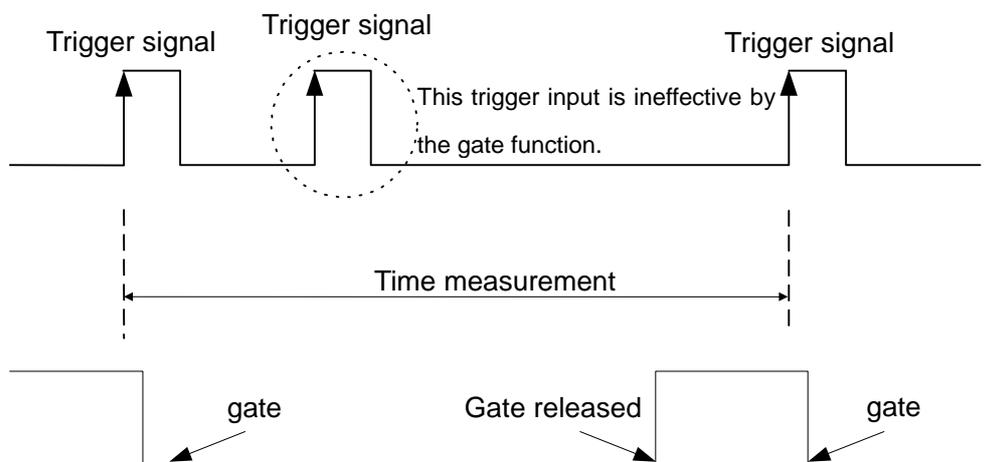
3. Detailed description

Intelligent I/O group 0 and 1 are composed of one 16-bit Base Timer for free-run operation and eight 16-bit registers for the time measurement function and waveform generation function.

Channel 6 and 7 have the gate function, which means the trigger input is ineffective until the gate is released after the time measurement starts from the first trigger input.

In this example, using the time measurement function of channel 6, the time is measured when the start edge is input to the port INPC06 at the gate released time.

Input pulse waveform



(1) Time measurement function setting

This example will use Channel 6 in Group 0 for the time measurement function. Select the rising edge mode for the trigger of the measurement.

(2) Time measurement calculation

Use the time measurement interrupt of Channel 6. Then, read the value of register G0TM6 during the interrupt routine. Then calculate the difference from the value that is measured last time. This is the measuring time.

(3) Gate releasing

Set the bit GSC in the register G0TMCR6 to "1" (release the gate).

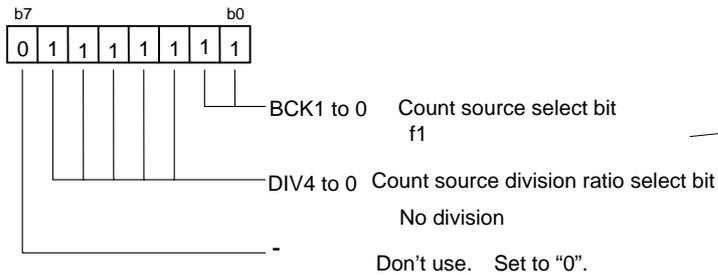
3.1 How to set up

This section shows the setting procedures and setting values to proceed section "3. Detailed Description". For detail configuration of each register, please refer to M32C/83 Group HARDWARE MANUAL.

(1) Inhibiting an Interrupt

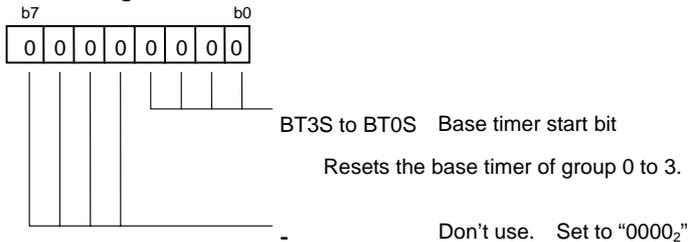
Set I flag=0. Or set bits ILV2 to 0=000₂ in register IIOkIC (k=0 to 11) where the interrupt request of the Intelligent I/O is assigned.

(2) G2BCR0 register



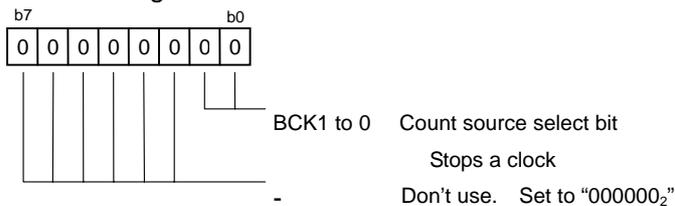
This setting supplies the BTSR register with a clock, and enables the register to be set.

(3) BTSR register



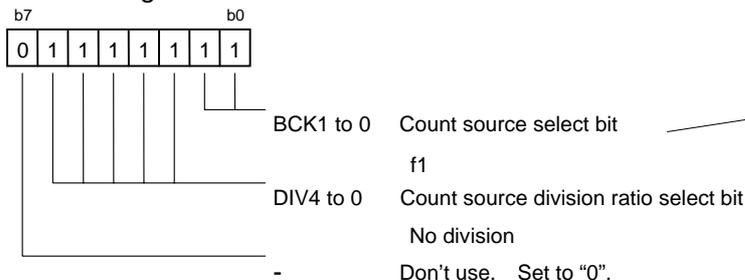
This setting resets Base Timers in Groups 0 to 3. Base Timer of Group i starts counting from 0000₁₆ by setting the BTS bit in the register GiBCR1 to "1" after the operation clock of Base Timer is set in GiBCR0 register.

(4) G2BCR0 register



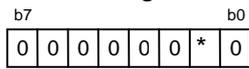
Stop a clock supplied to Group 2 when Group 2 and BTSR register are not used.

(5) GiBCR0 register



This setting supplies the registers (6) –(13) with a clock. Set each register to "01111111₂" in order to be effective after setting.

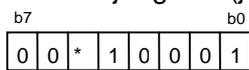
(6) GiBCR1 register



- Don't use. Set to "0".
- RST1 Base timer reset cause select bit 1
Base timer is reset by matching the GiPO0 with the Base timer.
- Don't use. Set to "00₂".
- BTS Base timer start bit
Resets the base timer
- UD1 to 0 Up down control bit
Up count mode
- Don't use. Set to "0".

Set the bit to "1" (starts base timer count) after setting Group i intelligent I/O related register.

(7) GiTMCRj register (j = 6,7)



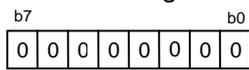
- CTS1 to 0 Timer measurement triaquer select bit
Rising edge
- DF1 to 0 Digital filter function select bit
No digital filter
- GT Gate function select bit
Use Gate function
- GOC Gate function release select bit
Release the gate by matching base timer with the register G0POp
- GSC Gate function release bit
- PR Prescaler function select bit
Don't use.

Set to use the trigger function

When J=6, P=4. When J=7, P=5

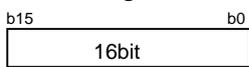
Note. Set this bit to "1" by matching Base Timer with the register G0POp when the gate release is operated.

(8) GiPOCR0 register



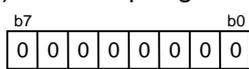
Set to "00000000₂"

(9) GiPO0 register



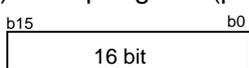
Set a period of the Base Timer reset

(10) GiPOCRp register (p=4,5)



Set to "00000000₂"

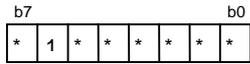
(11) GiPOp register (p=4,5)



Set a period for receiving a trigger input again after a trigger input is stopped.

When the gate is released, the setting (8) thru (11) is performed by matching the Base Timer with the register G0POp.

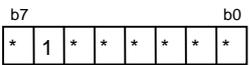
(12) GiFS register



- FSC5 to 0 Channel 5-1 time measurement, waveform generation function select bit
When Channel j is used, set the bit FSCj to "1" (select time measurement function)
- FSC6 Channel 6 time measurement, waveform generation function select bit
Channel 6 selects time measurement function
- FSC7 Channel 7 time measurement, waveform generation function select bit
When Channel 7 is used, set the bit FSC7 to "1" (select time measurement function)

The bit FSCj is a bit to select time measurement function or waveform generation function.

(13) GiFE register

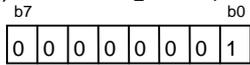


- IFE5 to 0 Channel 5 to 1 function enable bit
When Channel j is used, set the bit IFEj to "1" (operate channel j function).
- IFE6 Channel 6 function enable bit
Operate Channel 6 function
- IFE7 Channel 7 function enable bit
When Channel 7 is used, set the bit IFE7 to "1" (operate channel 7 function).

Set the FSC0,p bit and IFE0,p bit to "1" when the gate is released by matching base timer with G1POp register.

Set the bit IFEj of unused channel j to "0".

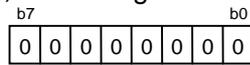
(14) IIOkIE register (k = 0 to 11)



- IRLT Interrupt Request select bit
Selects interrupt request
- bit7 to 1 Interrupt enable bit 7 to 1
Set to "000000₂"

Don't set the bit IRLT and the bit 7-1 to "1" at the same time.

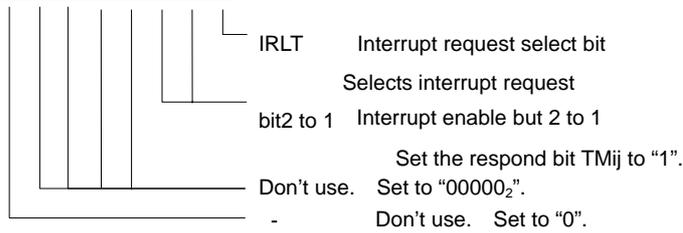
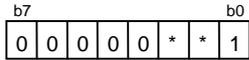
(15) IIOkIR register



- Don't use. Set to "0".
- Initializes interrupt request register.

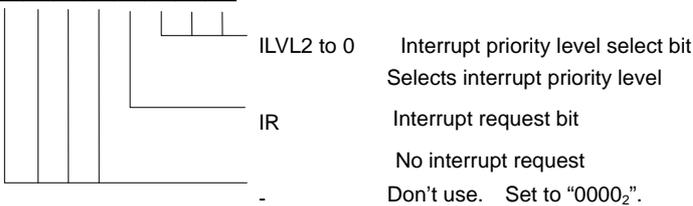
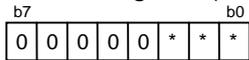
Set the register IIOkIR to "00₂".

(16) IIOkIE register (k = 0 to 11)



Set interrupt request bit not used for an interrupt to "0".

(17) IIOkIC register (k = 0 to 11)

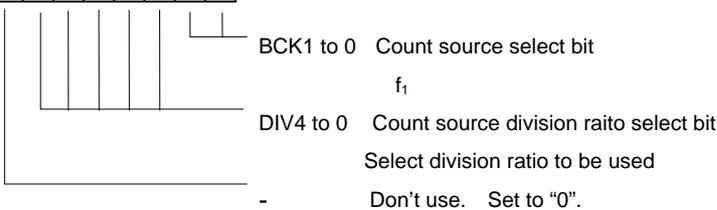
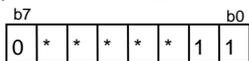


(18) PSC register, PSLa register (a=0 to 3), PSb register (b=0 to 9), IPS register

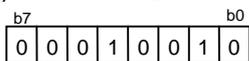
Set the port INPCij

(19) Interrupt enable flag (I flag = "1")

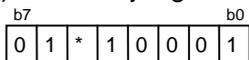
(20) GiBCR0 register



(21) GiBCR1 register



(22) G1TMCRj register (j = 6,7)



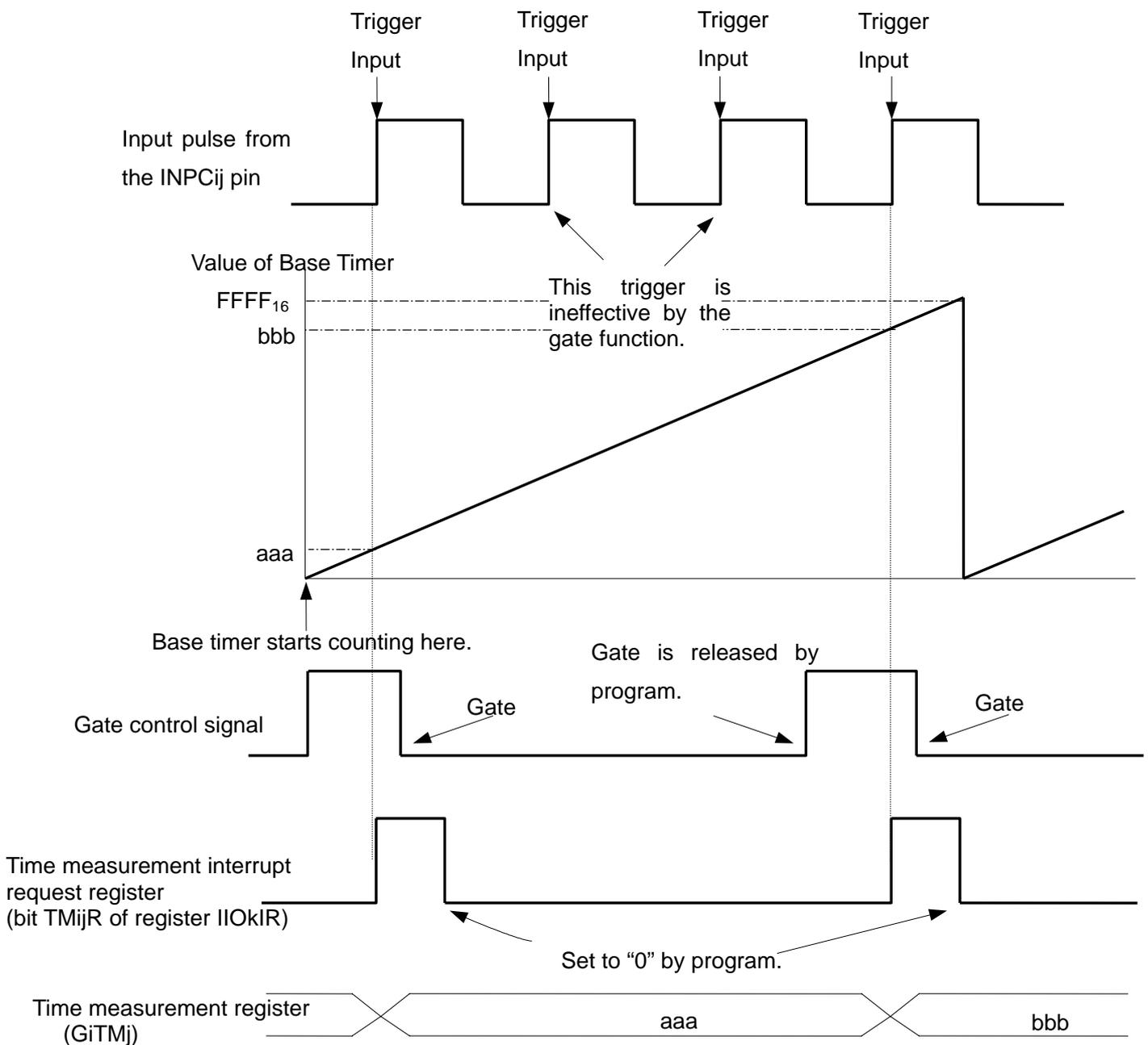
Note The gate is released in a cycle through a main loop.

3.2 Precaution on Interrupts

During the Intelligent I/O interrupt routine, the IIOkIR register corresponding to this interrupt must be set to "00₁₆" (initialize). If this setting is missing, the IR bit in the IIOkIC register is not set to "1" regardless of the Intelligent I/O interrupt request. (No interrupt occurs.)

3.3 Timing chart

The below is a timing diagram with setting according to the section 3.1 and 3.2.



4. The example of a reference program

```

/*****
/*      FILENAME: rej05b0395_src.c          *
/*      Ver      : 1.00                    *
/*      FUNCTION: Time measurement function of Intelligent I/O group 0,1 with gate function *
/*****
/*****
/*      include file                      */
/*****
#include <stdio.h>
#include "sfr32c83.h"

/*****
/*      Function Definition                */
/*****
void ch6_int();                          /* Interrupt Function */
#pragma INTERRUPT ch6_int

/*****
/*      Global variable Definition         */
/*****
static short palse;

/*****
/*      main                               */
/*****
void main()
{
    int i;
    /* main clock set */
    prc0 = 1;                          /* protect off */
    mcd   = 0x12;                       /* main clock : not divided */
    prc1 = 0;                          /* protect on */

    /* iio group0 initial set */
    g2bcr0 = 0x7f;
    btsr   = 0x00;                      /* all basetimer stop */
    g2bcr0 = 0x00;                      /* group2 clock stop */
    g0bcr0 = 0x7f;                      /*      b0,b1:  count source :f1
                                           b2 to b6: count source divided ratio :not divided */

    g0bcr1 = 0x00;
    g0tmcr6 = 0x11;                    /*      b0,b1:  staling edge
                                           b2,b3:  No digital filter
                                           b4:    Use the gate function
                                           b5:    Don't select the gate function release
                                           b6:    Gate function release bit
                                           b7:    Don't use prescaler function

g0fs   = 0x40;                        /*      ch6   : time measurement function */
g0fe   = 0x40;                        /*      ch0,6 : work the function */

    /* iio group0 interrupt initial set */
    /* ch6 */
    iio6ie = 0x01;                      /* Latch interrupt request */
    iio6ir = 0x00;                      /* Clear a flag for interrupt request */
    iio6ie = 0x03;                      /* Enables corresponding interrupt from interrupt requesting */
    iio6ic = 0x03;                      /* Sets interrupt priority level*/

    /* port set */
    pd15 = 0x00;                       /* INPC0_6 input */

```

```

ps2      = 0;
g0bcr0   = 0x7f;          /*      b0,b1:  count source:f1
                           b2 to b6: count source divided ratio : No divided*/

/* interrupt enable */
_asm("fset i");

/* iio group0 basetimer start */
bts_g0bcr1      = 1;

while(1){
    for(i=0; i<1000; i++){
        gsc_g0tmcr6 = 1;          /* Release the gate function */
    }
}

/* iio ch6 interrupt */
void ch6_int()
{
    static short p = 0;
    static signed short old_tr = 0;
    short signed now_tr;

    iio6ir = 0x00;          /* Clear interrupt request */

    now_tr = (signed short)g0tm6; /* Read time measurement register */
    palse = now_tr - old_tr;     /* Calculate the pulse width */
    old_tr = now_tr;           /* Save the latest register value */
}

/*----- program end */

```

5. Example Waveform and Result

The following example shows measuring a pulse width at pin INPC06 by using the Intelligent I/O Group 0.

Conditions: Supply voltage = 5V,

Main clock (Xin) = 30MHz

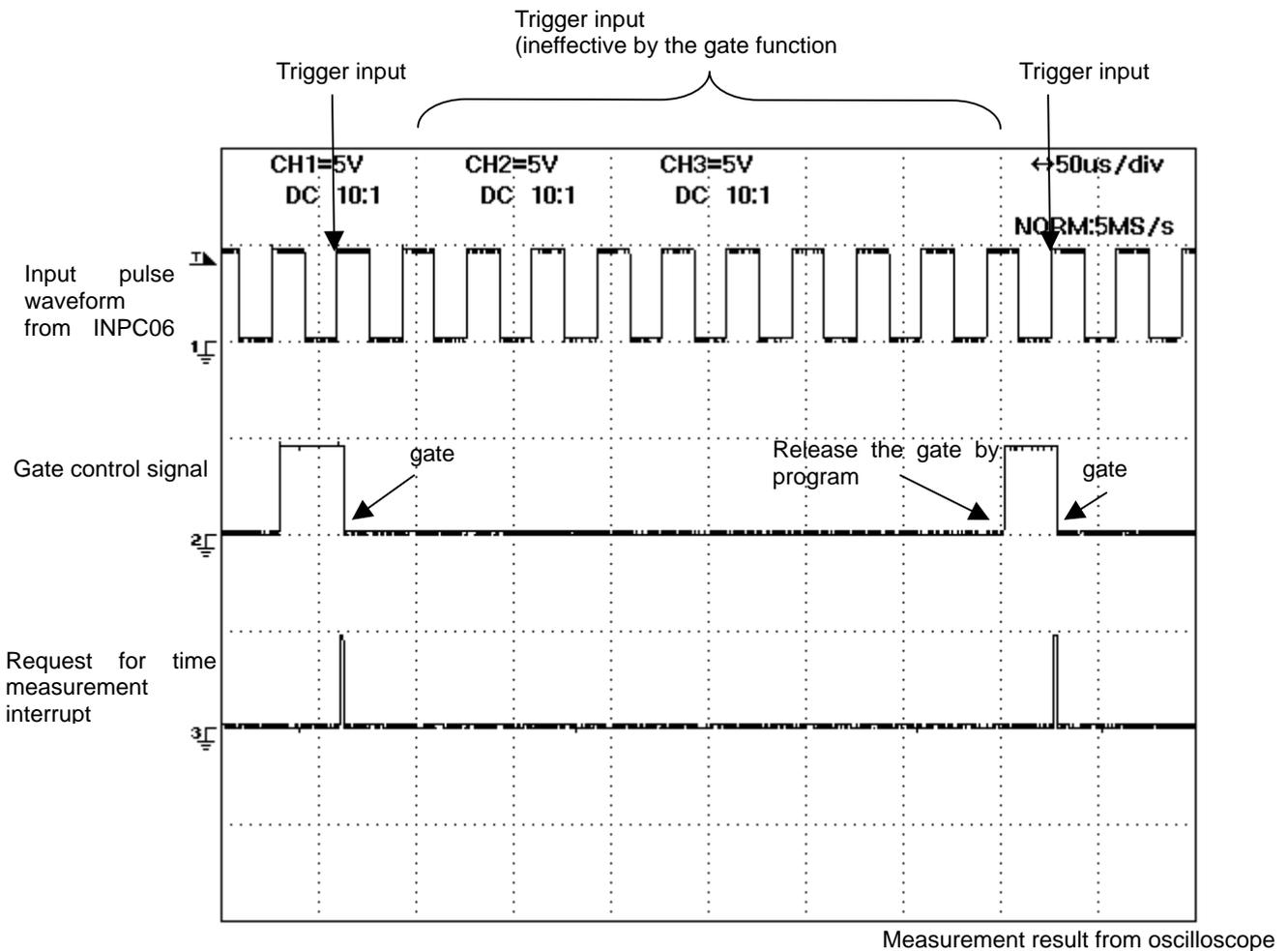
Base Timer operation clock (fBT) = 30MHz

Trigger Input = 30kHz (33 μs)

Gate release cycle = 2.7kHz

Result counts : 10984

$(33\mu s \times (n+1) n$: counts for ineffective trigger caused by the gate function)



6. Reference

HADWARE MANUAL

Refer to the M32C/ 83 group HARDWARE MANUAL.

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Rev.	Issue date		Revised
		Page	Point
1.00	Jan 30, 2004	-	First edition issued

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