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SH7080 Series

Synchronous Serial Communication Unit Master Reception (Reading from EEPROM)

Introduction

This application note describes master reception using the SSU (Synchronous Serial communication Unit) module. It is intended as reference material to help in the design of user software.

Target Device

SH7086

Contents

1. Specifications

In this application note, the synchronous serial communication unit is used to read 10-bytes of data from a 4-wire serial-transmission type EEPROM (HN58X2564I, 64K bits, 8K words × 8bit).

- The SH7086 is used as the master device in a single-master configuration.
- PE12 (general input/output port) of the SH7086 is used as the chip select pin for the EEPROM*.
- 10 bytes of data at the address of the EEPROM from H'0000 to H'0009are read.
- The data transfer clock (synchronization clock) is set to 2.5MHz.
- For reading out data from the EEPROM, the synchronous serial communication unit is set to transmission and reception operation simultaneously.

Figure 1 shows an example of connection between the SH7086 and the EEPROM. Table 1 shows the module settings of the synchronous serial communication unit. Table 2 lists the EEPROM instruction codes used in this sample application.

Note: * The synchronous serial communication unit enables the SCS pin for each frame.
When one or more frames is transmitted or received, the SCS pin is used as general output.

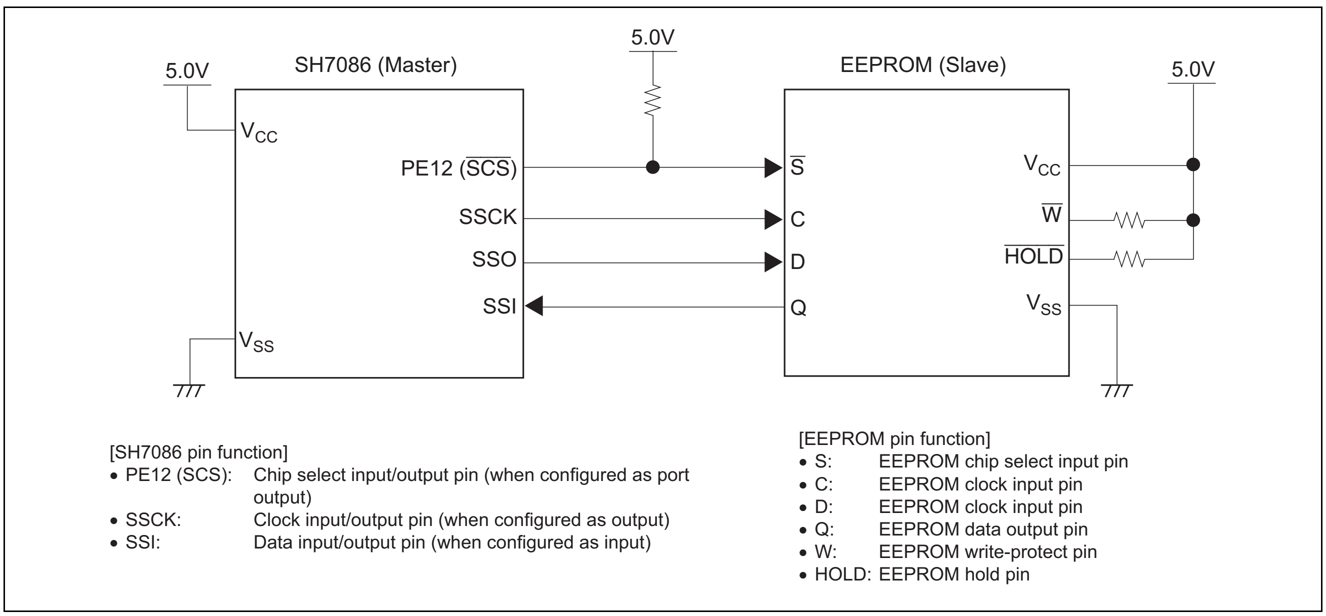


Figure 1 Example of Connection between the SH7086 and EEPROM

Table 1 Synchronous Serial Communication Unit Settings

Format	Settings
Operating mode	• Select master mode. • Select synchronous serial communication mode.
Data input/output pin	Normal (two data input/output pins used for communication)
Transfer clock	2.5 MHz (Pϕ = 40 MHz)
Number of data bits	8-bit data length
MSB/LSB first	MSB first
Timing for setting the TEND bit	The TEND bit is set after the final bit is transmitted.

Table 2 EEPROM instruction codes

Code Name	Operation	Code [B']
WREN	Sets the EEPROM as writable.	0000 0110
WRDI	Sets the EEPROM as non-writable.	0000 0100
RDSR	Reads the EEPROM Status Register.	0000 0101
WRSR	Writes the EEPROM Status Register.	0000 0001
READ	Reads stored data.	0000 0011
WRITE	Writes data.	0000 0010

2. Applicable Conditions

Table 3 shows the applicable conditions for this sample application.

Table 3 Applicable Conditions

Item	Setting
Device	SH7086 (R5F70865)
Operating frequency	Internal clock: Iϕ = 80 MHz Bus clock: Bϕ = 40 MHz Peripheral clock: Pϕ = 40 MHz MTU2 clock: MPϕ = 40 MHz MTU2S clock: MIϕ = 80 MHz
Device operating mode	Single-chip mode
Development environment	High-performance Embedded Workshop Version 4.03.00.001 SuperH RISC engine Standard Toolchain (V.9.1.1.0) SuperH RISC engine C/C++ Compiler (V.9.01.01) (Manufactured by Renesas Technology)
C compiler option	High-performance Embedded Workshop default setting -cpu=sh2 -include="$(WORKSPDIR)\inc" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo

3. Descriptions of Functions Used

An overview of the SSU (Synchronous Serial communication Unit) functions used in this sample application is given below.

3.1 Synchronous Serial Communication Unit

For synchronous serial communication, the SSU has a master mode in which this LSI outputs the clocks signal as the master device and a slave mode in which the clock signal is input from an external device. Synchronous serial communications between devices with different clock polarity and phase are possible.

Figure 2 shows a block diagram of the SSU module.

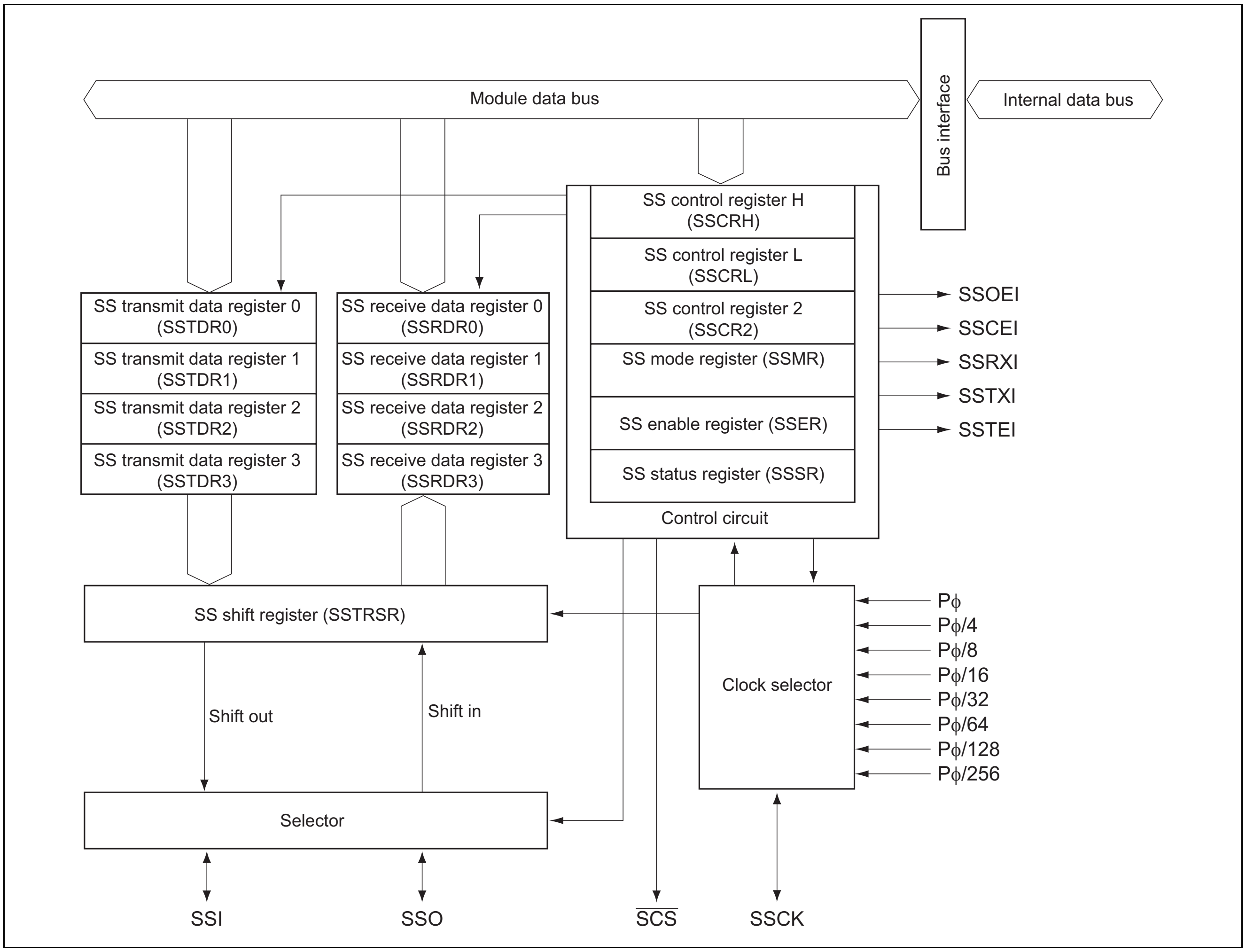


Figure 2 Block Diagram of the SSU Module

- SS Control Register H (SSCRH) selects the master or slave mode, selects the input/output pin mode, selects the SSO pin output value, and selects the $\overline{\text{SCS}}$ pin function.
- SS Control Register L (SSCRL) selects the operating mode, software reset, and the transmit/receive data length.
- The SS Mode Register (SSMR) selects MSB first or LSB first, the clock polarity, the clock phase, and the transfer clock rate.
- The SS Enable Register (SSER) enables and disables transmission, reception, and interrupts requests.
- The SS Status Register (SSSR) handles the status flags for various interrupts.
- SS Control Register 2 (SSCR2) is used to set open drain output for the SSO pin, SSI pin, SSCK pin, and SCS pin, the timing for assertion of the SCS signal, the timing for output of data from the SSO pin, and the timing for setting of the TEND bit.
- SS Transmit Data Registers 0 to 3 (SSTDR0 to 3) are 8-bit registers used to store data for transmission.
- SS Receive Data Registers 0 to 3 (SSRDR0 to 3) are 8-bit registers used to store received data.
- The SS Shift Register (SSTRSR) is used to transmit/receive serial data.

Note: For details on each register function, see the sections related to the synchronous serial communication unit in the SH7080 Group Hardware Manual.

4. Description of Operation

In this sample application, simultaneous transmission and reception operation in the SSU mode is applied to read data from the EEPROM.

4.1 Reading Data from an EEPROM

Data can be read from the EEPROM. According to the following procedure.

- Transmit the read code (READ) to the EEPROM
- Transmit the read start address to the EEPROM
- Output data from the EEPROM (receive data from the EEPROM)

Figure 3 shows the details of transfer to read data out from the EEPROM.

When data are read from the EEPROM, the EEPROM is set as the selected device (by setting PE12 low), the input clock signal then makes the EEPROM output consecutive data. After the output of each byte, the address is incremented within the EEPROM and data at the next address are output. To end the reading of data from the EEPROM device is deselected (PE12 is set high). The device can be deselected at anytime.

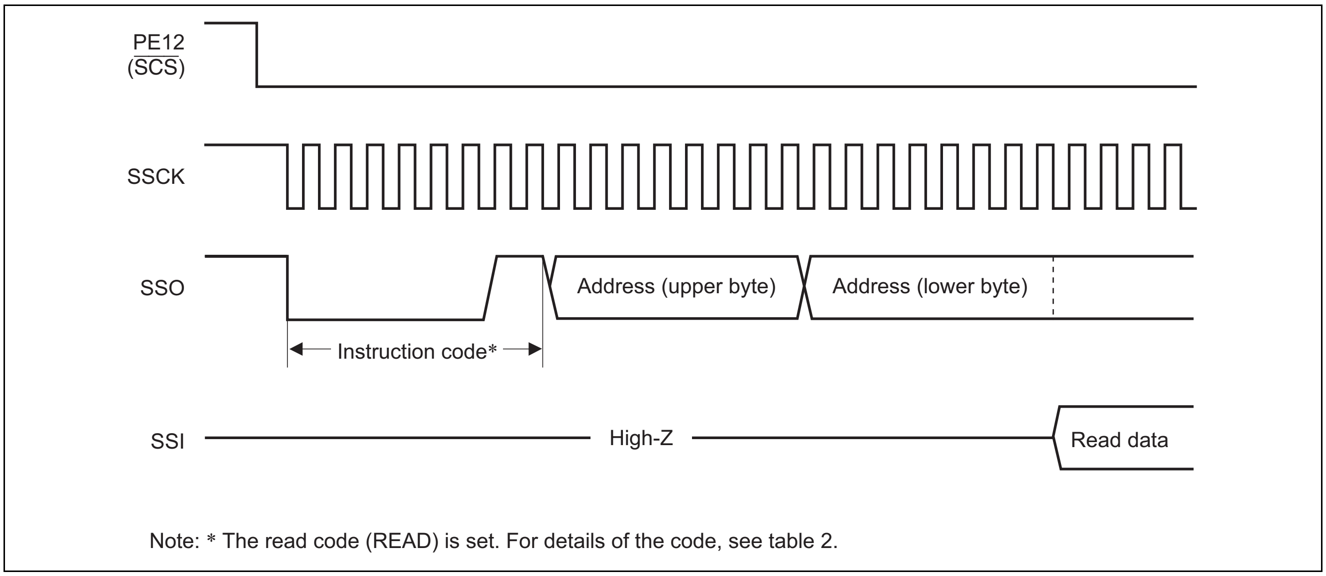
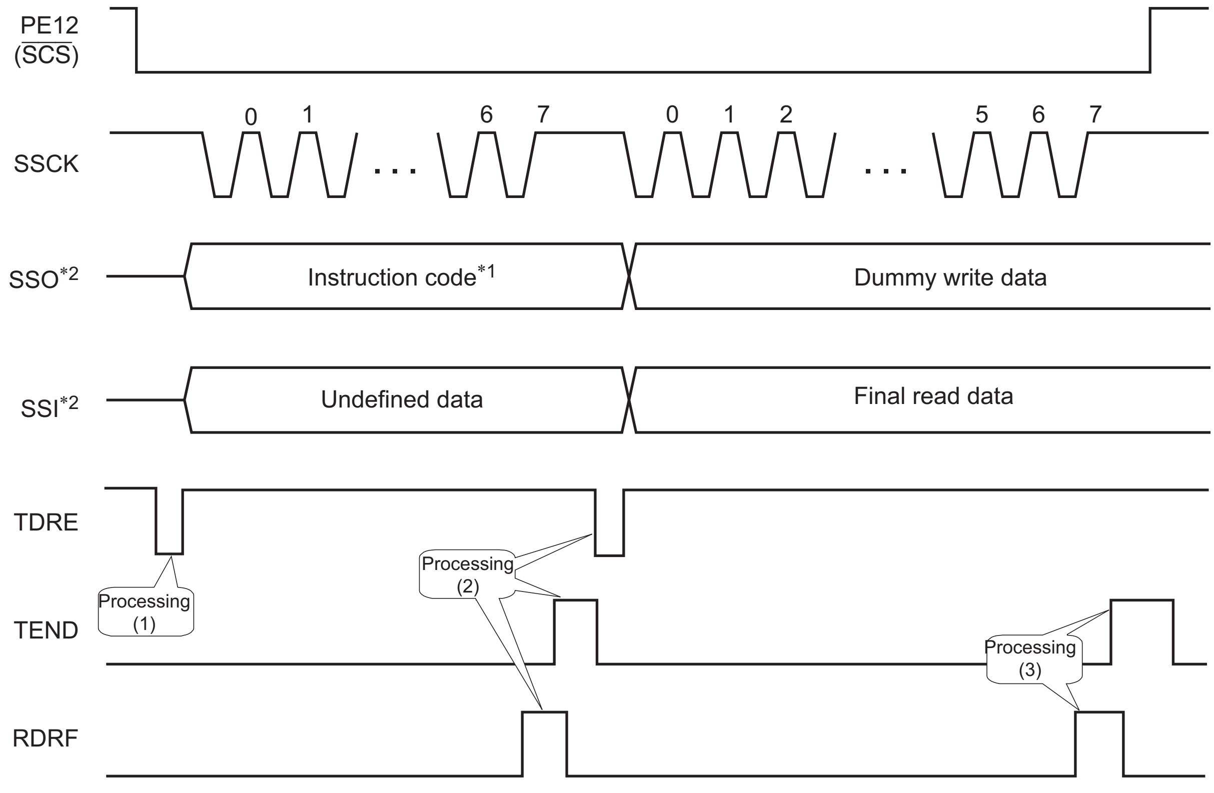


Figure 3 Details of Transfer to Read Data from the EEPROM

Figure 4 illustrates how data is read from the EEPROM. The software and hardware processing is described in table 4



Notes: 1. The read code (READ) is set. For details on the code, see table 2.
2. After the read operation, the SSO and SSI pins retain the level of the final bit.

Figure 4 Processing to Read Data

Table 4 Description of Software and Hardware Processing

	Software Processing	Hardware Processing
Process (1)	• Set PE12 low (output); (EEPROM selected). • Set data for transmission (instruction code) in SSTDR0 .	• Setting data for transmission in SSTDR0 clears the TDRE bit to 0. • Transfer the data for transmission from SSTDR0 to SSTRSR. • Set the TDRE bit to 1. • Transmit and receive the data.
Process (2)	• Confirm RDRF = 1, and read the SSRDR0 register. • Confirm TDRE = 1, and set data for transmission in the SSTDR0 register.	• Transmit and receive 1 frame (8 bits) of data. • Transfer data from the SSTRSR register to the SSRDR0 register. • Set the RDRF bit to 1. • After the last bit is transmitted with TDRE = 1, set the TEND bit to 1. • Clear the RDRF bit to 0 by reading the SSRDR0 register. • Setting data for transmission in the SSTDR0 register clears the TDRE and TEND bits to 0. • Transfer the data for transmission from the SSTDR0 register to the SSTRSR register. • Set the TDRE bit to 1. • Transmit and receive the data.
Process (3)	• Confirm RDRF = 1, and read the SSRDR0 register. • Set PE12 high (output); (EEPROM deselected) • Clear the TEND bit to 0. • Clear the TE and RE bits to 0 to disable transmit/receive operations.	• Transmit and receive 1 frame (8 bits) of data. • Transfer data from the SSTRSR register to the SSRDR0 register. • Set the RDRF bit to 1. • After transmission of the last bit with TDRE = 1, set the TEND bit to 1.

5. Description of Software

5.1 Description of Modules

The modules used in this sample applications are described in Table 5.

Table 5 Description of Modules

Module Name	Label Name	Description
Main function	main()	Sets the operating frequency, sets the address to start reading from, calls the SSU initialization function, and calls the EEPROM data-read function.
SSU initialization function	init_ssu()	Release the SSU from module standby mode, sets the pin function controller (PFC), and sets the SSU.
EEPROM-data reading function	read_EEPROM()	Reads data from the EEPROM.
Instruction code setting function	set_inst_code()	Sets an instruction code in the EEPROM Status Register.
EEPROM addressing function	set_addr_EEPROM()	Sets the start address in the EEPROM.

5.2 Variables Used

The variables used in this sample application are described in Table 6.

Table 6 Variables

Variable, Label Name	Description	Used In
read_data[0-9]	Array for storing read-out data	Main function
address	EEPROM address where reading starts	Main function
addr	Copy of the EEPROM address where reading starts	EEPROM-data reading function EEPROM addressing function
*r_data	Pointer variable to the array where the read-out data are stored	EEPROM-data reading function
num	Number of received data	EEPROM-data reading function
dmmy_w	Variable for a dummy write	EEPROM data-read function
dmmy_r	Variable for a dummy read	EEPROM-data reading function Instruction code setting function EEPROM addressing function
code	Instruction code	Instruction code setting function

5.3 Settings of Registers

This section describes the settings of registers used in this sample application. Note that the settings presented below are for this sample application and are not the initial values.

5.3.1 Register for Setting the Clock Pulse Generator (CPG)

1. Frequency Control Register (FRQCR)
   This register specifies the division ratio of the frequency.
   Setting: H'0241

Bit	Bit Name	Value	Function
15	—	0	Reserved
14 to 12	IFC[2-0]	000	Internal Clock (Iϕ) Frequency Division Ratio 000: × 1, 80 MHz when the input clock is 10 MHz
11 to 9	BFC[2-0]	001	Bus Clock (Bϕ) Frequency Division Ratio 001: × 1/2, 40 MHz when the input clock is 10 MHz
8 to 6	PFC[2-0]	001	Peripheral Clock (Pϕ) Frequency Division Ratio 001: × 1/2, 40 MHz when the input clock is 10 MHz
5 to 3	MIFC[2-0]	000	MTU2S Clock (MIϕ) Frequency Division Ratio 000: × 1, 80 MHz when the input clock is 10 MHz
2 to 0	MPFC[2-0]	001	MTU2 Clock (MPϕ) Frequency Division Ratio 001: × 1/2, 40 MHz when the input clock is 10 MHz

5.3.2 Setting the Power-Down Mode

1. Standby Control Register 3 (STBCR3)
   This register controls the operation of individual modules in the power-down mode.
   Setting: H'FB

Bit	Bit Name	Value	Function
7	MSTP15	1	1: Stops clock supply to I^2C2.
6	MSTP14	1	1: Stops clock supply to SCIF.
5	MSTP13	1	1: Stops clock supply to SCI_2.
4	MSTP12	1	1: Stops clock supply to SCI_1.
3	MSTP11	1	1: Stops clock supply to SCI_0.
2	MSTP10	0	0: SSU is operational.
1 to 0	—	11	Reserved

5.3.3 Registers for Setting the Synchronous Serial Communication Unit

1. SS Control Register H (SSCRH)
   This register selects the master or slave mode and sets the SCS pin function.
   Setting: H'8F

Bit	Bit Name	Value	Function
7	MSS	1	0: Master mode
6	BIDE	0	0: Normal mode (two input/output pins used for communication)
5	—	0	Reserved
4	SOL	0	0: Changes the serial data output to a low level.
3	SOLP	1	SOL write-protect When SOL bit is changed, the SOLP is set to 1.
2	—	1	Reserved
1 to 0	CSS[1-0]	11	11: The $\overline{\text{SCS}}$ pin is used with the automatic output function.

- SS Control Register L (SSCRL)
  This register selects the operating mode, software reset, and data length.
  Setting: H'80

Bit	Bit Name	Value	Function
7	FCLRM	1	1: Clears the interrupt flag when the register is accessed.
6	SSUMS	0	0: SSU mode
5	SRES	0	Setting 1 forcibly resets the SSU internally.
4 to 2	—	0	Reserved
1 to 0	DATS[1-0]	00	00: 8-bit data length

- SS Mode Register (SSMR)
  This register selects MSB-first and the transfer clock rate.
  Setting: H'83

Bit	Bit Name	Value	Function
7	MLS	1	1: MSB first
6	CPOS	0	0: Outputs high from the SSCK pin in the idle state and low in the active state.
5	CPHS	0	0: Changes the data at the first edge on the SSCK pin.
4 to 3	—	0	Reserved
2 to 0	CKS[2-0]	011	011: Transfer clock = Pϕ/16 (Pϕ = 40 MHz)

- SS Enable Register (SSER)
  This register enables transmit/receive operation.
  Setting: H'C0

Bit	Bit Name	Value	Function
7	TE	1	1: Enables transmission operation
6	RE	1	1: Enables reception operation.
5 to 4	—	0	Reserved
3	TEIE	0	0: Disables SSTEI interrupts.
2	TIE	0	0: Disables SSTXI interrupts.
1	RIE	0	0: Disables SSRXI and SSOEI interrupts.
0	CEIE	0	0: Disables SSCEI interrupts.

- SS Status Register (SSSR)
  SSSR is a status flag register for interrupts.
  Setting: H'04

Bit	Bit Name	Value	Function
7	—	0	Reserved
6	ORER	0	Overrun error
5 to 4	—	0	Reserved
3	TEND	0	Transmission end
2	TDRE	1	Transmit data empty
1	RDRF	0	Receive data register full
0	CE	0	Conflict error/incomplete error

Note: For clearing conditions of the individual flags, see the hardware manual.

- SS Control Register 2 (SSCR2)
  This register selects the timing for setting the TEND bit.
  Setting: H'10

Bit	Bit Name	Value	Function
7 to 5	—	000	Reserved
4	TENDSTS	1	1: Sets the TEND bit after transmission of the last bit.
3	SCSATS	0	Selects the timing for asserting the $\overline{\text{SCS}}$ signal*.
2	SSODTS	0	Selects the timing for outputting data from the SSO pin*.
1 to 0	—	00	Reserved

Note: * See the hardware manual for details.

- SS Transmit Data Register 0 (SSTDR0)*
  This register is an 8-bit register that stores data for tranmission.
  Setting: H'00 (initial value)

Note: * Since the data length is 8 bits, SSTDR1 to SSTDR3 are not used.

- SS Receive Data Register 0 (SSRDR0)*
  This is an 8-bit register that stores received data.
  Setting: H'00 (initial value)

Note: * Since the data length is 8 bits, SSRDR1 to 3 are not used.

5.3.4 Registers for Setting the Pin Function Controller (PFC)

1. Port E Control Register L4 (PECRL4)
   This register selects the functions of multiplexed pins of port E (PE15-PE12).
   Setting: H'0000

Bit	Bit Name	Value	Function
15	—	0	Reserved
14 to 12	PE15MD[2-0]	000	000: Sets the pin function to PE15 (general input/output).
11	—	0	Reserved
10 to 8	PE14MD[2-0]	000	000: Sets the pin function to PE14 (general input/output).
7 to 6	—	00	Reserved
5 to 4	PE13MD[1-0]	00	00: Sets the pin function to PE13 (general input/output).
3	—	0	Reserved
2 to 0	PE12MD[2-0]	000	000: Sets the pin function to PE12 (general input/output).

- Port E Control Register L3 (PECRL3)
  This register selects the functions of multiplexed pins of port E (PE11-PE8).
  Setting: H'0505

Bit	Bit Name	Value	Function
15	—	0	Reserved
14 to 12	PE11MD[2-0]	000	000: Sets the pin function to PE11 (general input/output).
11	—	0	Reserved
10 to 8	PE10MD[2-0]	101	101: Sets the pin function to SSO (SSU data input/output).
7	—	0	Reserved
6 to 4	PE9MD[2-0]	000	000: Sets the pin function to PE10 (general input/output).
3	—	0	Reserved
2 to 0	PE8MD[2-0]	101	101: Sets the pin function to SSCK (SSU clock input/output).

- Port E Control Register L2 (PECRL2)
  This register selects the functions of multiplexed pins of port E (PE7-PE4).
  Setting: H'5000

Bit	Bit Name	Value	Function
15	—	0	Reserved
14 to 12	PE7MD[1-0]	101	101: Sets the pin function to SSI (SSU data input/output).
11	—	0	Reserved
10 to 8	PE6MD[3-0]	000	000: Sets the pin function to PE6 (general input/output).
7	—	0	Reserved
6 to 4	PE5MD[3-0]	000	000: Sets the pin function to PE5 (general input/output).
3	—	0	Reserved
2 to 0	PE4MD[3-0]	000	000: Sets the pin function to PE4 (general input/output).

- Port E I/O Register L (PEIORL)
  This register selects the functions of multiplexed pins of port E (PE7-PE4).
  Setting: H'5000

Bit	Bit Name	Value	Function
15	PE15IOR	0	0: Input
14	PE14IOR	0	0: Input
13	PE13IOR	0	0: Input
12	PE12IOR	1	1: Output ($\overline{SCS}$ is used as a general input/output port)
11	PE11IOR	0	0: Input
10	PE10IOR	0	0: Input
9	PE9IOR	0	0: Input
8	PE8IOR	0	0: Input
7	PE7IOR	0	0: Input
6	PE6IOR	0	0: Input
5	PE5IOR	0	0: Input
4	PE4IOR	0	0: Input
3	PE3IOR	0	0: Input
2	PE2IOR	0	0: Input
1	PE1IOR	0	0: Input
0	PE0IOR	0	0: Input

5.3.5 Setting the I/O Port

1. Port E Data Register L (PEDRL)
   This register stores port E data.
   Setting: H'1000

Bit	Bit Name	Value	Function
15	PE15DR	0	0: The port state is low level.
14	PE14DR	0	0: The port state is low level.
13	PE13DR	0	0: The port state is low level.
12	PE12DR	1	0: The EEPROM is selected. 1: The EEPROM is deselected.
11	PE11DR	0	0: The port state is low level.
10	PE10DR	0	0: The port state is low level.
9	PE9DR	0	0: The port state is low level.
8	PE8DR	0	0: The port state is low level.
7	PE7DR	0	0: The port state is low level.
6	PE6DR	0	0: The port state is low level.
5	PE5DR	0	0: The port state is low level.
4	PE4DR	0	0: The port state is low level.
3	PE3DR	0	0: The port state is low level.
2	PE2DR	0	0: The port state is low level.
1	PE1DR	0	0: The port state is low level.
0	PE0DR	0	0: The port state is low level.

6. Flowcharts

Figure 5 to figure 10 show flows of processing to read data from the EEPROM.

6.1 Main Function

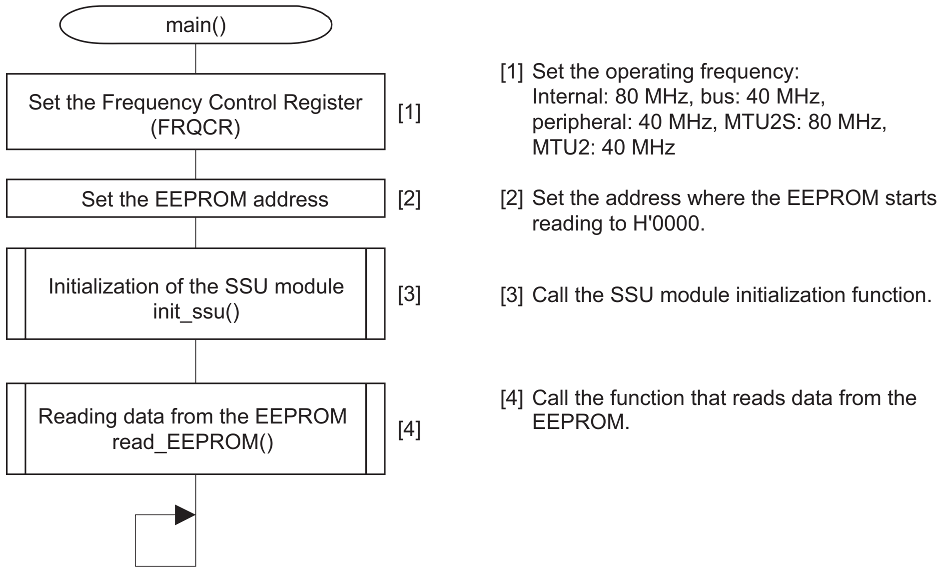
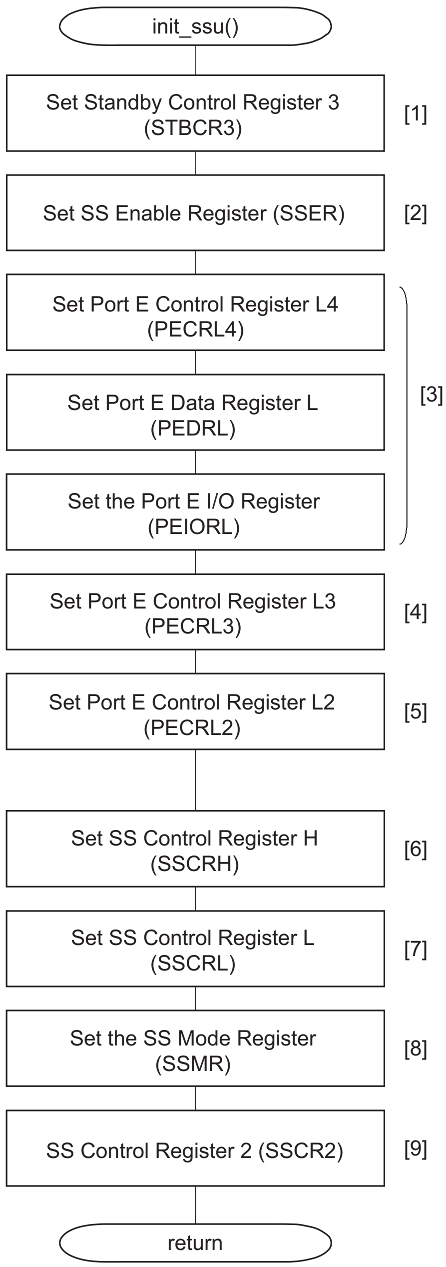


Figure 5 Main Function Processing

6.2 SSU Initialization Function



[1] Release the SSU from module standby mode.

[2] Clear the TE and RE bits to 0.
Stop SSU operation.

[3] PE12 port pin function setting:
- Set PE12 as an output pin for the port function (general input/output).
- Set the output level high to deselect the EEPROM.

The chip select pins of EEPROM are controlled by the port output (the chip select pin function ($\overline{SCS}$) of the SSU is not used).

[4] PE10 and PE8 port pin function settings
- PE10: Set to SSO (data input/output pin).
- PE8: Set to SSI (data input/output pin).

[5] PE7 pin function setting
- Set PE7 to SSCK (clock input/output).

[6] Function settings
- Master mode selected
- Normal mode (two input/output pins used for communication)
- $\overline{SCS}$ automatic output function (high before and after transfer, low during transfer)

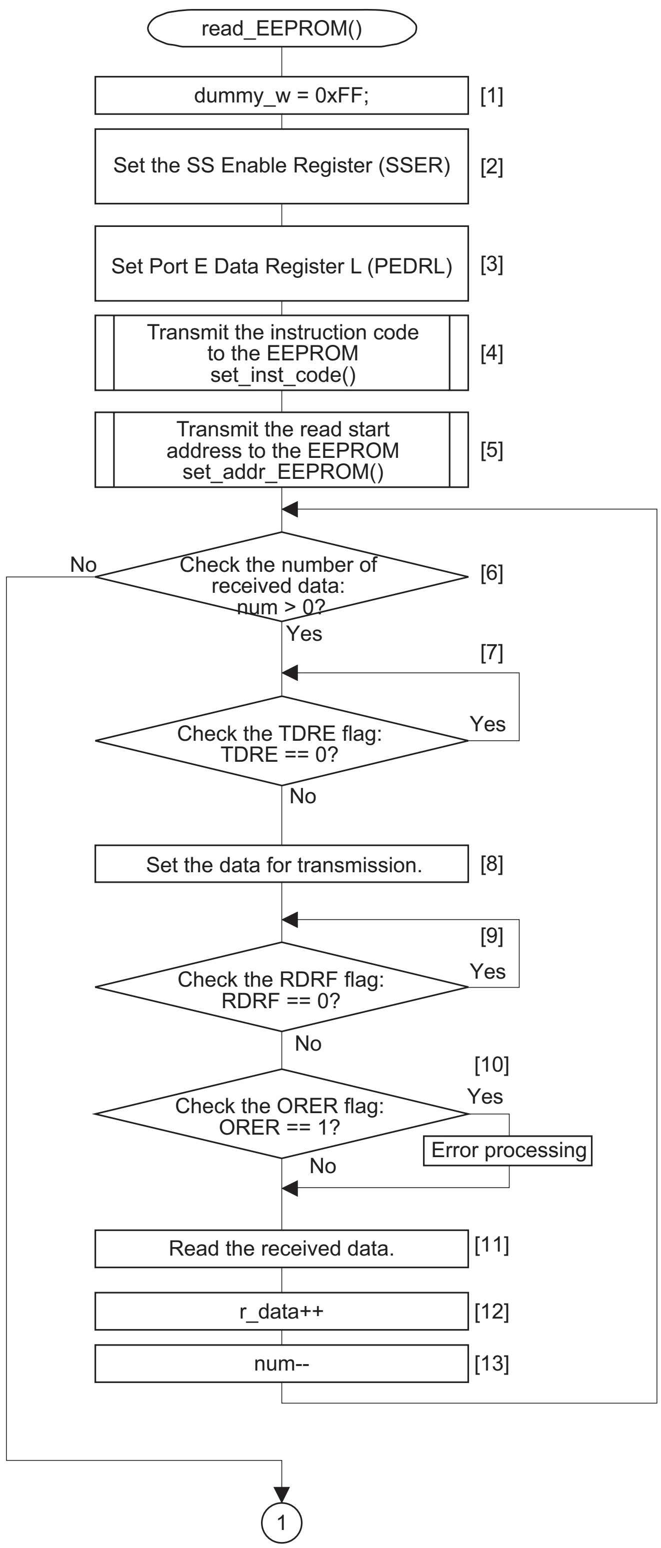
[7] Function settings
- Clear the interrupt flag when the register is accessed.
- SSU mode
- 8-bit data length

[8] Function settings:
- MSB-first selected
- Clock polarity (idle to high, active to low)
- Clock phase select: Data change on the first edge
- Transfer clock rate: Pf/16 (prescaler division ratio)

[9] Function settings:
- Set the TEND flag to 1 after the final data bit is output.

Figure 6 SSU Initialization Processing

6.3 EEPROM-Data Reading Function



read_EEPROM(argument 1, argument 2, argument3) function

- Argument 1: Addressing
- Argument 2: Pointer to the storage variable for read data
- Argument 3: Number of received data

[1] Set dummy data for transmission.

[2] Enable simultaneous transmission and reception by the SSU (TE = 1, RE = 1).

[3] Set the PE12 (SCS) output to low to change the EEPROM to selected.

[4] Transmit the READ code (instruction code) to the EEPROM.
Start an EEPROM-data read operation.

[5] Transmit the read start address to the EEPROM.

[6] Perform successive data reception operations (dummy transmission) until the specified number of data is reached.

[7] Wait until the TDRE bit in the SS Status Register (SSSR) is set to 1 and the SS Transmit Register (SSTDR) is writable.

[8] Set dummy data for transmission in SSTDR. This is the dummy transmission operation for the reception operation.

[9] Wait until the RDRF bit in SSSR is set to 1 and 1 byte has been received.

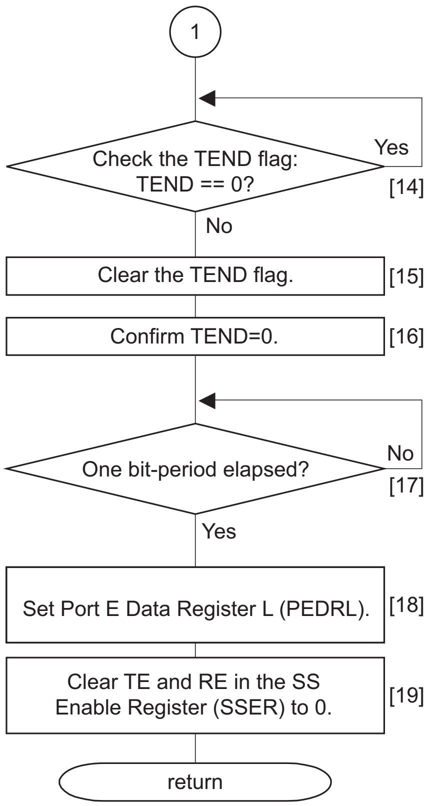
[10] Checking for an overrun error
If the ORER bit in SSSR is 1, an overrun error has occurred. In the case, perform error processing. Errors are not processed in this sample application.

[11] Store the data received from the EEPROM in SS Receive Data Register 0 (SSRDR0).

[12] Increment the received data storage pointer variable.

[13] Decrement the number of received data.

Figure 7 Processing for EEPROM-Data Reading (1)



[14] Wait until 1 frame of data has been transmitted and the TEND bit in the SS Status Register (SSSR) is set to 1.

[15] Clear the TEND bit in SSSR to 0.

[16] Confirm that the TEND bit in SSSR is 0.

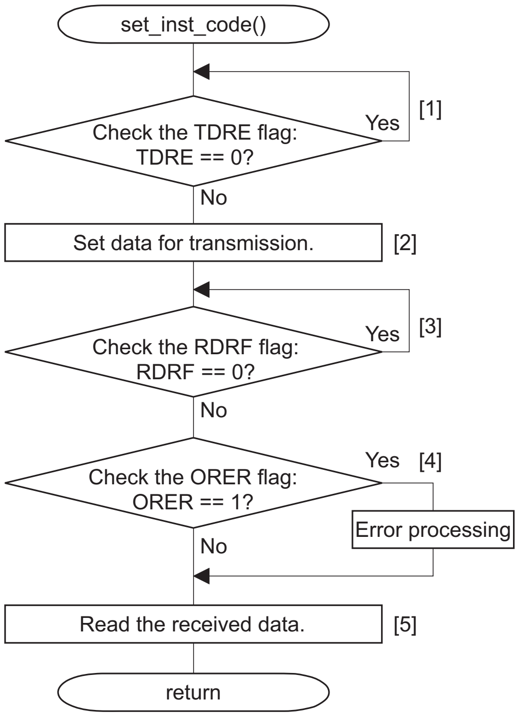
[17] Wait at least one bit-period until the last bit has been transmitted.

[18] Set the PE12 (SCS) output to low to deselect the EEPROM.

[19] Disable transmission/reception operations of the SSU ((TE = 0, RE = 0)).
Complete the operation of reading data from the EEPROM.

Figure 8 Processing for EEPROM-Data Reading (2)

6.4 EEPROM Instruction Code Setting Function



set_inst_code(argument 1) function
• Argument 1: EEPROM instruction code

[1] Wait until the TDRE bit in the SS Status Register (SSSR) is set to 1 and the SS Transmit Register (SSTDR) is writable.

[2] Set data (instruction code) for transmission in SSTDR.

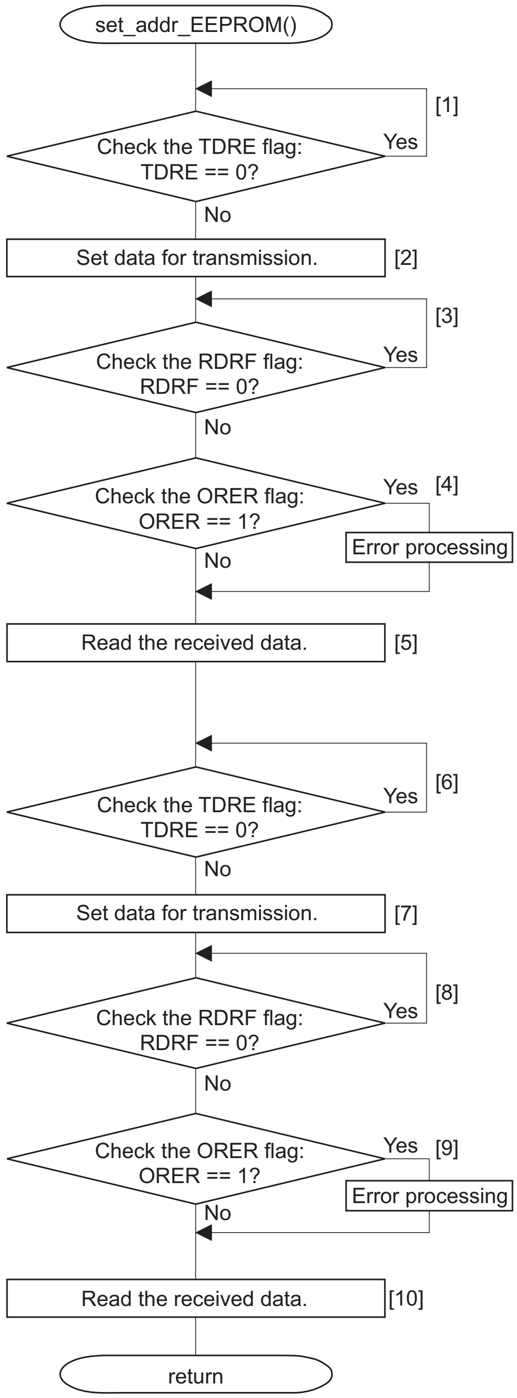
[3] Wait until the RDRF bit in SSSR is set to 1 and 1 byte has been received.

[4] Checking for an overrun error
If the ORER bit in SSSR is 1, an overrun error has occurred. In that case, perform error processing. Errors are not processed in this sample application.

[5] Dummy-read the received data held in SS Receive Data Register 0 (SSRDR0).

Figure 9 Processing for EEPROM Instruction Code Setting

6.5 EEPROM Addressing Function



set_inst_code(argument 1) function

- Argument 1: Read start address (2-byte data)

[1] Wait until the TDRE bit in the SS Status Register (SSSR) is set to 1 and the SS Transmit Register (SSTDR) is writable.

[2] Set the higher-order byte of the (2-byte) start address in SSTFR.

[3] Wait until the RDRF bit in SSSR is set to 1 and 1 byte has been received.

[4] Checking for an overrun error
If the ORER bit in SSSR is 1, an overrun error has occurred. In that case, perform error processing. Errors are not processed in this sample application.

[5] Dummy-read the received data held by the SS Receive Data Register 0 (SSRDR0).

[6] Wait until the TDRE bit in the SS Status Register (SSSR) is set to 1 and the SS Transmit Register (SSTDR) is writable.

[7] Set the lower-order byte of the (2-byte) start address in SSTDR.

[8] Wait until the RDRF bit in SSSR is set to 1 and 1 byte has been received.

[9] Checking for an overrun error
If the ORER bit in SSSR is 1, an overrun error has occurred. In that case, perform error processing. Errors are not processed in this sample application.

[10] Dummy read the received data held by the SS Receive Data Register 0 (SSRDR0).

Figure 10 Processing for EEPROM Addressing

7. Documents for Reference

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7080 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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