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April 1\textsuperscript{st}, 2010
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SH7263/SH7203 Group
SSI Master Transmitter

Introduction
This application note presents an example of data transfer by the serial sound interface (SSI).

Target Device
SH7263/SH7203

Contents

1. Preface........................................................................................................................................... 2
2. Description of the Sample Application ...................................................................................... 3
3. Documents for Reference .............................................................................................................. 19
1. Preface

1.1 Specifications
The serial sound interface (SSI) is set to master transmitter mode for PCM data transmission.
The direct memory access controller (DMAC) is used for data transfer to the SSI.

1.2 Module Used
- Serial sound interface (SSI)
- Direct memory access controller (DMAC)

1.3 Applicable Conditions
- MCU: SH7263/SH7203
- Operating frequency: Internal clock 200 MHz
  Bus clock 66.67 MHz
  Peripheral clock 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options: 
  -cpu = sh2afpu -fpu = single -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo

1.4 Related Application Note
The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of Initialization" for the SH7263/SH7203 Group (REJ06B0740). Please refer to that document when setting up this sample task.
2. Description of the Sample Application

In this sample application, the SSI operates as a master transmitter with the sampling rate set to 44.1 kHz.

2.1 Operational Overview of Module Used

The following are the features of the serial sound interface (SSI):

- Number of channels: Four channels
- Operating mode: Non-compressed mode
  - The non-compressed mode supports serial audio streams divided by channels.
- Serves as both a transmitter and a receiver
- Capable of using serial bus format
- Handles asynchronous transfer between the data buffer and the shift register.
- It is possible to select a dividing ratio for the clock used by the serial bus interface.
- It is possible to control data transmission and reception with DMAC or interrupt requests.
- Selects the oversampling clock input from among the following pins:
  - EXTAL, XTAL (Clock operation modes 0)
  - CKIO (Clock operation mode 2)
  - AUDIO_CLK
  - AUDIO_X1, AUDIO_X2

To change the oversampling clock, change the value in the SSI oversampling clock selection register (SCSR) of the pin function controller (PFC).

Table 1 shows the oversampling clock source selection made by setting the SSInCKS bits in the SCSR. Figure 1 shows the block diagram of the SSI.

<table>
<thead>
<tr>
<th>Settings of SSInCKS[2:0] *1</th>
<th>Clock Operation Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 or 1</td>
</tr>
<tr>
<td>000</td>
<td>AUDIO_X1 input</td>
</tr>
<tr>
<td>001</td>
<td>AUDIO_X1 input / 4</td>
</tr>
<tr>
<td>010</td>
<td>AUDIO_CLK input</td>
</tr>
<tr>
<td>011</td>
<td>AUDIO_CLK input / 4</td>
</tr>
<tr>
<td>100</td>
<td>EXTAL input</td>
</tr>
<tr>
<td>101</td>
<td>EXTAL input / 4</td>
</tr>
<tr>
<td>110</td>
<td>EXTAL input / 2</td>
</tr>
<tr>
<td>111</td>
<td>EXTAL input / 8</td>
</tr>
</tbody>
</table>

Notes:
1. n = 0 to 3
2. When using the AUDIO_CLK input clock, set the PF30MD0 bit to 1 in the port F control register H4 (PFCRH4).
Figure 1 Block Diagram of SSI
2.2 Procedure for Setting the Module Used

Figures 2 and 3 show the examples of the SSI and DMAC setting procedures, respectively.

For details on the settings of individual registers, see the SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).

![Figure 2 Example of SSI Setting Procedure](image-url)
START

Set standby control register 2 (STBCR2)

Set DMA channel control register (CHCRn)

Set DMA source address register (SARn)

Set DMA reload source address register (RSARn)

Set DMA destination address register (DARn)

Set DMA reload destination address register (RDARn)

Set DMA transfer count register (DMATCRn)

Set DMA reload transfer count register (RDMATCRn)

Set DMA channel control register (CHCRn)

Set DMA extension resource selector (DMARS0 to DMARS3)

Set DMA operation register (DMAORn)

Set interrupt priority register (IPR05)

Set DMA channel control register (CHCRn)

END

- Enabling clock supply to the DMAC (STBCR2)
  MSTP8 (module stop 8) bit is cleared to 0.
  [Function] Supplies clock to DMAC.

- Disabling the DMA transfer (CHCRn)
  DE (DMA enable) bit is cleared to 0.
  [Function] DMA transfer is disabled.

- DMA source address settings (SARn)
  [Function] Specifies a DMA transfer source address.

- DMA reload source address settings (RSARn)
  [Function] Specifies a DMA transfer source reload address.

- DMA destination address settings (DARn)
  [Function] Specifies a DMA transfer destination address.

- DMA reload destination address settings (RDARn)
  [Function] Specifies a DMA transfer destination reload address.

- DMA transfer count settings (DMATCRn)
  [Function] Specifies the DMA transfer count.

- DMA reload transfer count settings (RDMACTRn)
  [Function] Specifies the DMA reload transfer count.

- DMA transfer mode setting (CHCRn)
  TC (transfer count mode) bit is set.
  [Function] "0": Transmits data once by one transfer request
  (when the transfer request source is set to SSI)
  RLDSAR (SAR reload function ON/OFF) bit is set.
  [Function] Enables or disables the function to reload SAR and DMATCR.
  RLDDAR (DAR reload function ON/OFF) bit is set.
  [Function] Enables or disables the function to reload DAR and DMATCR.
  TEMASK (TE set mask) bit is set to 1.
  [Function] DMA transfer does not stop even if the TE bit is set
  DM (destination address mode) bit is set.
  [Function] Selects whether to increase or decrease a DMA transfer destination address.
  Fixes a DMA transfer destination address.
  SM (source address mode) bit is set.
  [Function] Selects whether to increase or decrease a DMA transfer source address.
  Increases a DMA transfer source address.
  RS (resource select) bits are set to B’1000.
  [Function] Selects DMA extension resource selector (DMA transfer request source)
  TB (transfer bus mode) bit is set.
  [Function] Selects DMA transfer bus mode.
  Cycle steal mode
  [Note] When TC is set to 0, cycle steal mode should be set.
  TS (transfer size) bit is set.
  [Function] Selects the DMA transfer size.
  IE (interrupt enable) bit is set.
  [Function] Enables or disables an interrupt request.

- DMA transfer request from on-chip peripheral module settings (DMARS0 to DMARS3)
  [Function] Selects a DMA transfer request from SSI.

- DMA operation setting (DMAOR)
  AE (address error flag) bit is read, and then cleared to 0.
  [Function] Clears the address error flag.
  NMIF (NMI flag) bit is read, and then cleared to 0.
  [Function] Clears the NMI flag.
  DME (DMA master enable) bit is set to 1.
  [Function] Enables DMA transfer on all channels.

- Enabling DMA transfer (CHCRn)
  DE (DMA enable) bit is set to 1.
  [Function] Starts DMA transfer.

Figure 3 Example of DMAC Setting Procedure
2.3 Operation of the Sample Program

In the sample program, the DMAC channel 1 is activated by the DMA transfer request from the SSI, and data is transferred from the external memory to the transmit data register (SSITDR) in the SSI channel 0. The data written to SSITDR is transferred to the shift register upon transmission request, and is then output from the SSIDATA pin.

In the sample program, 10 samples (40 bytes) of PCM data are transferred four times. When the transfer has been completed, the SSI output is muted.

The SSI settings for the sample program are as follows:

- Channel used: channel 0
- Operation mode: master transmitter mode
- Data transmission control method: DMAC
- Oversampling clock: AUDIO_X1 input (16.9344 MHz)
- Serial oversampling clock frequency: Oversampling clock frequency/6 (2.8224 MHz)
- Data word length: 16 bits
- System word length: 32 bits
- Padding bit: "L" level
- No delay between SSIWS and SSIDATA
- SSIWS and SSIDATA change on the falling edge of SSISCK.
- Sampling frequency: 44.1 kHz \[354 \text{ ns} (2.8224 \text{ MHz}) \times 32 \text{ bits} \times 2\]
- "HFFFF" and "H'0000" are set in data word 1 (L channel) of the 1st channel and data word 2 (R channel) of the 2nd channel, respectively.
Figure 4 shows the output waveform of the sample program and figure 5 shows the block diagram of the configuration used for the sample program.

**Figure 4  Output Waveform of Sample Program**

**Figure 5  Block Diagram of Configuration Used for Sample Program**
### 2.4 Sequence of Processing by the Sample Program

Tables 2 and 3 show the settings of the SSI and DMAC registers used in the sample program, respectively.

Figure 6 shows the processing flow of the sample program.

#### Table 2 SSI Register Settings Used in Sample Program

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control register</td>
<td>H'FFFF C000</td>
<td>H'1C0B D553</td>
<td>DMEN = &quot;1&quot;: DMA request is enabled.</td>
</tr>
<tr>
<td>(SSICR_0)</td>
<td></td>
<td></td>
<td>UIEN = &quot;1&quot;: Underflow Interrupt is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OIEN = &quot;1&quot;: Overflow interrupt is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IIEN = &quot;0&quot;: Idle mode interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CHNL = &quot;B'00&quot;: One channel per system word</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DWL = &quot;B'001&quot;: Data Word Length 16 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SWL = &quot;B'011&quot;: System Word Length 32 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCKD = &quot;1&quot;: Serial bit clock is output. Master mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SWSD = &quot;1&quot;: Serial word is set as input. Master mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SCKP = &quot;0&quot;: Serial Bit Clock Polarity. SSIWS and SSI DATA change on SSISCK falling edge.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SWSP = &quot;1&quot;: Serial WS Polarity, high for 1st channel, low for 2nd channel.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SPDP = &quot;0&quot;: Padding bits are low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDTA = &quot;1&quot;: Transmitting and receiving in the order of padding bits and serial data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PDTA = &quot;0&quot;: When a data word length is 16 bits, the PDTA setting is ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DEL = &quot;1&quot;: No delay between SSIWS and SSIDATA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKDV = &quot;B'101&quot;: Oversampling clock frequency / 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MUEN = &quot;0&quot;: Module is not muted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TRMD = &quot;1&quot;: SSI module is in transmit mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>EN = &quot;1&quot;: SSI module is enabled.</td>
</tr>
</tbody>
</table>
### Table 3  DMAC Register Settings Used in Sample Program

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 2 (STBCR2)</td>
<td>H'FFFE 0018</td>
<td>H'00</td>
<td>MSTP8 = &quot;0&quot;: DMAC is operational.</td>
</tr>
<tr>
<td>DMA channel control register_1 (CHCR1)</td>
<td>H'FFFE 101C</td>
<td>H'0000 0000</td>
<td>DE = &quot;0&quot;: DMA transfer disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H'2010 1814</td>
<td>TC = &quot;0&quot;: Transmits data once. RLDSAR = &quot;1&quot;: Enables the function to reload SAR.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RLDDAR = &quot;0&quot;: Disables the function to reload DAR. TEMASK = &quot;1&quot;: * DMA transfer does not stop even if the TE bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DM = &quot;B'00&quot;: Fixed destination address SM = &quot;B'01&quot;: Source address is incremented.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RS = &quot;B'1000&quot;: DMA extension resource selector TB = &quot;0&quot;: Cycle steal mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TS = &quot;B'10&quot;: Longword transfer IE = &quot;1&quot;: Enables an interrupt request.</td>
</tr>
<tr>
<td>DMA source address register_1 (SAR1)</td>
<td>H'FFFE 1010</td>
<td>On-chip RAM</td>
<td>Transfer source start address: Sets an area in the on-chip RAM.</td>
</tr>
<tr>
<td>DMA reload source address register_1 (RSAR1)</td>
<td>H'FFFE 1110</td>
<td>On-chip RAM</td>
<td>Transfer source start address: Sets an area in the on-chip RAM.</td>
</tr>
<tr>
<td>DMA destination address register_1 (DAR1)</td>
<td>H'FFFE 1014</td>
<td>H'FFFF C008</td>
<td>Transfer destination start address: SSI transmit data register (SSITDR_0)</td>
</tr>
<tr>
<td>DMA transfer count register_1 (DMATCR1)</td>
<td>H'FFFE 1018</td>
<td>H'0000 0000A</td>
<td>Transfer count: 10 (H'0A)</td>
</tr>
<tr>
<td>DMA operation register (DMAOR)</td>
<td>H'FFFE 1200</td>
<td>H'0001</td>
<td>DME = &quot;1&quot;: DMA transfer is enabled on all channels.</td>
</tr>
<tr>
<td>DMA extension resource selector 0 (DMARS0)</td>
<td>H'FFFE 1300</td>
<td>H'0023</td>
<td>SSI channel 0</td>
</tr>
</tbody>
</table>

Note: 1. PCM data must be output from the SSI at a constant timing.

When TEMASK is set to "0", the DMA is disabled upon the completion of DMA transfer. Thus, the SSI might have an underflow if interrupt processing on completion of DMA transfer is delayed due to the period over which interrupts are disabled in the main routine and so on. To prevent this, we recommend the setting TEMASK = 1 so that DMA transfer can continue immediately after a previous round of DMA transfer is completed.
Is the SSI module enabled?

- Disable a DMA request.
- Disable an error interrupt.

Is the transmit buffer empty?

- Set mute.

Yes

No

DMA transfer end interrupt

io_int_dma1 function

START

Count -

Count == 0?

- Disable DMA transfer.
- Set SSI mute.
- Clear the transfer end flag.
- Dummy read of the transfer end flag

END

SSI mute setting

io_ssi0_set_mute function

START

No

Is the SSI module enabled?

- Yes

Disdisable a DMA request.
- Disable an error interrupt.

No

Is the transmit buffer empty?

- Yes

Set mute.

END

Figure 6 Flow of Processing by the Sample Program
### 2.5 Listing of the Sample Program

```c
/*FILE COMMENT************************************************************
* System Name  : SH7203 Sample Program
* File Name  : main.c
* Contents    : SSI data transfer
* Version     : 1.00.00
* Model       : M3A-HS30
* CPU         : SH7203
* Compiler    : SHC9.1.1.0
* note        : A data transfer sample program using SSI0
*/

# define DMA_SIZE_BYTE   0x0000u
# define DMA_SIZE_WORD   0x0001u
# define DMA_SIZE_LONG   0x0002u
# define DMA_SIZE_LONGx4 0x0003u
# define DMA_INT_DISABLE 0x0000u
# define DMA_INT_ENABLE  0x0010u
# define DMA_INT (DMA_INT_ENABLE >> 4u)

#include <string.h>
#include "iodefine.h"      /* iodefine.h is a file automatically created by HEW*/

void main(void);
void io_init_ssi0(void);
void io_ssi0_set_mute(void);
void io_init_dma1(void *src, void *dst, size_t size, unsigned int mode);

unsigned long Data[10] = {
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful
};

#include "string.h"

#define DMA_SIZE_BYTE   0x0000u
#define DMA_SIZE_WORD   0x0001u
#define DMA_SIZE_LONG   0x0002u
#define DMA_SIZE_LONGx4 0x0003u
#define DMA_INT_DISABLE 0x0000u
#define DMA_INT_ENABLE  0x0010u
#define DMA_INT (DMA_INT_ENABLE >> 4u)

#include <string.h>

#include "iodefine.h"      /* iodefine.h is a file automatically created by HEW*/

void main(void);
void io_init_ssi0(void);
void io_ssi0_set_mute(void);
void io_init_dma1(void *src, void *dst, size_t size, unsigned int mode);

unsigned long Data[10] = {
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful,
  0x0000fffful, 0x0000fffful
};

#include <string.h>
```

Figure 7 Sample Program Listing: main.c (1)
```c
/* **FUNC COMMENT*********************************************************
* Outline   : Sample program main
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : void main(void);
*-----------------------------------------------------------------------
* Function   : Initializes the SSI module, and then transfers data.
*-----------------------------------------------------------------------
* Argument   : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice     :
**FUNC COMMENT END*****************************************************/

void main(void)
{
    Count = 4;        /* DMA transfer count */

    /* ==== Initialize DMAC and enable transfer ==== */
    io_init_dma1(Data,    /* Source address */
                  (void *)&SSI0.SSITDR,    /* Destination address */
                  sizeof(Data),            /* Number of bytes */
                  DMA_SIZE_LONG | DMA_INT_ENABLE);   /* 32 bits; interrupts enabled */

    /* ==== Initialize SSI0 ==== */
    io_init_ssi0();

    while(1){
        /* Program end */
    }
}
```

**Figure 8** Sample Program Listing: main.c (2)
void io_init_ssi0(void)
{
    /* === Supply clock to SSI module === */
    CPG.STBCR6.BIT.MSTP67 = 0u; /* SSI0 */

    /* === Select an oversampling clock supply source === */
    PORT.SCSR.BIT.SSI0CKS = 0u; /* AUDIO_X1 input 16.9344 MHz */

    /* === SSI module pin enabled === */
    PORT.PFCRH1.BIT.PF18MD = 1u; /* SSISCK0 */
    PORT.PFCRH1.BIT.PF19MD = 1u; /* SSIWS0 */
    PORT.PFCRH2.BIT.PF20MD = 1u; /* SSIDATA0 */

    /* === Control register (SSICR) === */
    SSI0.SSICR.LONG = 0x1c0bd553ul;

    /*
     * bit31-29 : reserve 0
     * bit28 : DMEN : 1------------- DMA request is enabled
     * bit27 : UIEN : 1-------------- Underflow interrupt is enabled
     * bit26 : OIEN : 1-------------- Overflow interrupt is enabled
     * bit25 : IIEN : 0-------------- Idle mode interrupt is disabled
     * bit24 : DIEN : 0-------------- Data interrupt is disabled
     * bit23-22 : CHNL : 0---------- Having one channel per system word
     * bit21-19 : DWL : B'001-------- Data word length 16 bits
     * bit18-16 : SWL : B'011-------- System word length 32 bits
     * bit15 : SCKD : 1-------------- Serial bit clock is output; master mode
     * bit14 : SWSD : 1-------------- Serial word select is output; master mode
     * bit13 : SCKP : 0-------------- SSIS and SSIData change at the SSISCK rising edge
     * bit12 : SWSP : 1-------------- SSIMS is high for first channel, and low for second channel
     * bit11 : SPDP : 0-------------- Padding bits are low
     * bit10 : SDTA : 1-------------- Transmitting and receiving padding bits and serial data in this order
     * bit9 : PDTA : 0-------------- Not used
     * bit8 : DEL : 1-------------- No delay between SS1WS and SSIDATA
     * bit7 : reserve 0
     * bit6-4 : CKDV : B'101-------- Oversampling clock frequency (16.9344 MHz) / 6 [44.1 kHz]
     * bit3 : MUEN : 0-------------- SSI module is not muted
     * bit2 : reserve 0
     * bit1 : TRMD : 1-------------- SSI module is in transmit mode
     * bit0 : EN : 1-------------- SSI module is enabled
     */
}
void io_ssi0_set_mute(void)
{
    if(S80.SSICR.BIT.EN == 1ul) {
        /* ---- disable SSI interrupt ---- */
        S80.SSICR.BIT.UIEN = 0ul;
    
        /* ---- disable dreq ---- */
        S80.SSICR.BIT.DMEN = 0ul;
        while(S80.SSISR.BIT.DIRQ == 0ul) {
            /* ---- wait data req ---- */

            S80.SSICR.BIT.MUEN = 1ul; /* mute start */
        }
    }

    if(S80.SSISR.BIT.UIRQ == 1ul) {
        S80.SSISR.BIT.UIRQ = 0ul;
        while(1) {
            /* dead loop */
        }
    }

    if(S80.SSISR.BIT.OIRQ == 1ul) {
        S80.SSISR.BIT.OIRQ = 0ul;
        while(1) {
            /* dead loop */
        }
    }

    if(S80.SSISR.BIT.IIRQ == 1ul) {
        S80.SSISR.BIT.IIRQ = 0ul;
    }
}

Figure 10 Sample Program Listing: main.c (4)
/*"FUNC COMMENT"*******************************************************
* Outline   : DMA transfer initial setting
*---------------------------------------------------------------------
* Include   : #include "iodefine.h"
*---------------------------------------------------------------------
* Function   : Transfers data for the number of bytes specified by "size" from source
*---------------------------------------------------------------------
* Argument   : void *src : Source address
*              : void *dst : Destination address
*              : size_t size : Transfer size (byte)
*              : unsigned int mode : Transfer mode: The following modes are specified with logical OR.
*              :        DMA_SIZE_BYTE(0x0000) Byte transfer
*              :        DMA_SIZE_WORD(0x0001) Word transfer
*              :        DMA_SIZE_LONG(0x0002) Longword transfer
*              :        DMA_SIZE_LONGx4(0x0003) 16-byte transfer
*              :        DMA_INT_DISABLE(0x0000) DMA transfer end interrupt is not used
*              :        DMA_INT_ENABLE(0x0010) DMA transfer end interrupt is used
*---------------------------------------------------------------------
* Return Value : void
*---------------------------------------------------------------------
* Notice   : If the transfer size and source/destination address alignment
*              : do not match, correct operation is not guaranteed.
*              : To use an interrupt, the interrupt routine should be registered.
"FUNC COMMENT END"***************************************************/

void io_init_dma1(void *src, void *dst, size_t size, unsigned int mode)
{
    unsigned int ts;
    unsigned long ie;
    ts = mode & 3u;
    ie = (mode & 0x00f0u) >> 4u;
    /* ====
    Set standby control register 2 (STBCR2) ====
    */
    CPG.STBCR2.BIT.MSTP8 = 0u;       /* Cancel DMAC module stop */
    /* ---- Set DMA channel control registers ----
    */
    DMAC.CHCR1.BIT.DE = 0ul;       /* Disable DMA transfer */
    /* ---- Set DMA source address register ----
    */
    DMAC.SAR1.LONG = (unsigned long)src;
    /* ---- Set DMA reload address register ----
    */
    DMAC.RSAR1.LONG = (unsigned long)src;
    /* ---- Set DMA destination address register ----
    */
    DMAC.DAR1.LONG = (unsigned long)dst;
    /* ---- Set DMA reload destination address register ----
    */
    DMAC.RDAR1.LONG = (unsigned long)dst;
    /* ---- Set DMA transfer count register ----
    */
    switch(ts){
        case DMA_SIZE_BYTE:
            DMAC.DMATCR1.LONG = size;     /* Set transfer count (1/1) */
            DMAC.RDMATCR1.LONG = size;
            break;
        case DMA_SIZE_WORD:
            DMAC.DMATCR1.LONG = size >> 1u; /* Set transfer count (1/2) */
            DMAC.RDMATCR1.LONG = size >> 1u;
            break;
        case DMA_SIZE_LONG:
            DMAC.DMATCR1.LONG = size >> 2u; /* Set transfer count (1/4) */
            DMAC.RDMATCR1.LONG = size >> 2u;
            break;
        case DMA_SIZE_LONGx4:
            DMAC.DMATCR1.LONG = size >> 4u; /* Set transfer count (1/16) */
            DMAC.RDMATCR1.LONG = size >> 4u;
            break;
        default:
            break;
    }
}

Figure 11  Sample Program Listing: main.c (5)
/* ---- Set DMA channel control registers ---- */
DMAC.CHCR1.LONG = 0x20101800ul | (ts << 3u) | (ie << 2u) ;
/*
bit31 : TC DMACTR transfer 0--------- 1 Transfers data once
bit30 : reserve 0
bit29 : RLDSAR OFF : 1---------- Enables the function to reload SAR
bit28 : RLDSAR OFF : 0---------- Disables the function to reload DAR
bit27-24 : reserve 0
bit23 : DO over run0 : 0--------- Not used
bit22 : TL TEND low active : 0---- Not used
bit21 : reserve 0
bit20 : TEMASK :TE set mask : 1---- DMA transfer does not stop even if the TE bit is set
bit19 : HE :0------------------- Not used
bit18 : HIE :0------------------- Not used
bit17 : AM :0------------------- Not used
bit16 : AL :0------------------- Not used
bit15-14 : SM1:0 DM0:0---------- Fixed destination address
bit13-12 : SM1:0 SM0:1--------- Source address is incremented
bit11-8 : RS : auto request : B'1000- DMA extension resource selector
bit7 : DL : DREQ level : 0 ------ Not used
bit6 : DS : DREQ select :0 Low level Not used
bit5 : TB : cycle :0------------- Cycle steal mode
bit4-3 : TS : transfer size: B'10--- Longword unit
bit2 : IE : interrupt enable: 1--- DMA transfer does not stop even if the TE bit is set
bit1 : TE : transfer end----------
bit0 : DE : DMA enable bit: 0----- DMA transfer is disabled
*/
/* ---- Set DMA extension resource selector 0 ---- */
DMAC.DMARS0.BIT.CH1MID = 0x08u; /* MID = SSI0 */
DMAC.DMARS0.BIT.CH1RID = 0x03u; /* RID */
/* ---- Set DMA operation register ---- */
DMAC.DMAOR.WORD &= 0xfff9u; /* Clear the AE and NMIF bits */
if(DMAC.DMAOR.BIT.DME == 0ul){ /* Enable DMA transfer on all channels */
DMAC.DMAOR.BIT.DME = 1ul;
}
if(ie == 1ul){
INTC.IPR06.BIT._DMAC1 = 1u; /* Set the interrupt priority */
}
/* ---- Perform DMA transfer ---- */
DMAC.CHCR1.BIT.DE = 1ul; /* Enable DMA transfer */
}*/

/**FUNC COMMENT******************************************
* Outline   : DMA transfer end interrupt
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : void io_int_dma1(void);
*-----------------------------------------------------------------------
* Function   : Shifts the SSI to the mute state when the DMA transfers are executed for the specified count.
*-----------------------------------------------------------------------
* Argument   : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice   :
/**FUNC COMMENT END**************************************************/
void io_int_dma1(void)
{
volatile unsigned long dummy;
Count--;
if(Count == 0){ /* Transfers are executed for the specified count */
/* ---- Stop DMA transfer---- */
DMAC.CHCR1.BIT.DE = 0ul; /* Disable DMA1 transfer */
io_ssi0_set_mute(); /* Set mute */
}
DMAC.CHCR1.BIT.TE = 0ul; /* Clear the transfer end flag */
dummy = DMAC.CHCR1.BIT.TE;
}*/
/* End of File */
```c
#include <machine.h>
#include "vect.h"
#pragma section IntPRG

(Snip)

// 112 DMAC1 TEI1
void INT_DMAC1_TEI1(void)
{
    extern void io_int_dma1(void);
    io_int_dma1();
}

(Snip)

// 214 SSI0
void INT_SSI0(void)
{
    extern void io_int_ssi0(void);
    io_int_ssi0();
}

(Snip)

/* End of File */

Figure 13  Sample Program Listing: intprg.c (1)"
3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7203 Group Hardware Manual (REJ09B0313)
  The most up-to-date version of this document is available on the Renesas Technology Website.
  SH7263 Group Hardware Manual (REJ09B0290)
  The most up-to-date version of this document is available on the Renesas Technology Website.
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<tbody>
<tr>
<td>1.00</td>
<td>Jan.19.09</td>
<td>First edition issued</td>
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