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Renesas Electronics Corporation

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M16C/80 Group

The Software Reset Judging Method

1.0 Abstract

The following article introduces the software reset / power-on-reset judging method and its application.

2.0 Introduction

The explanation of this issue is applied in the following condition.
Applicable MCU: M16C/ 80 Group

This program can be also operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/80 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3.0 Description of the application example

This chapter describes how to judge which reset, software or hardware, is operated.

< Specification for software reset judgment>

The contents of internal RAM are preserved. Write the data proved to be for the software reset operation (data for software reset judgment) to the internal RAM just before software reset is operated. After the reset, the initial setting processor judges which reset, hardware or software, is operated from this data for the software reset judgment. Initialize the data after the reset is operated.

When you use this procedure, be aware of the following timing in which it cannot judge which reset, hardware or software, is operated.

- Hardware reset is operated before the completion of the data initialization in the internal RAM.
- Hardware reset is operated just before the software reset is operated.

A section on 3.1 describes an example of the reset judgment of which reset is operated after software reset is executed while the watchdog timer interrupt is processed.

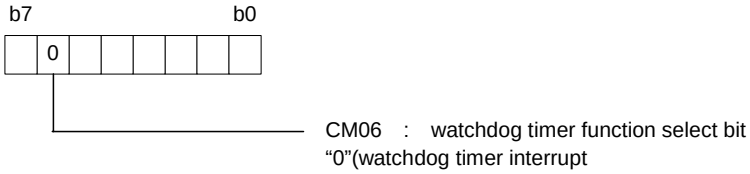
3.1 Judgment Procedures

The setup procedures for “3.0 Description of the application example” will be shown.

Refer to M16C/80 group datasheet for the details of each register.

(1) Set system clock control register 0 (CM0).

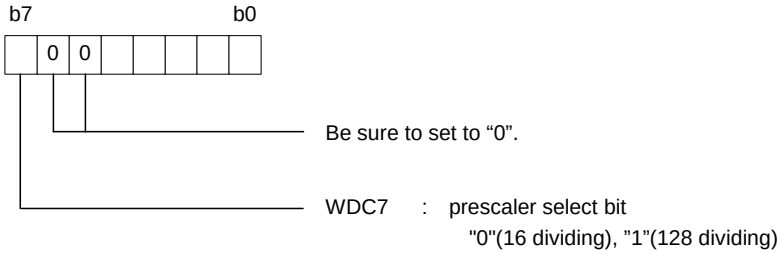
- Set the watchdog timer function select bit to “watchdog timer interrupt”.



(Note) : When writing this register, set bit 0 in the protect register (000A16 address) to “1”.

(2) Set the watchdog timer control register (WDC).

- Set prescaler.



(3) Set the watchdog timer start register (WDTS).

- The watchdog timer is initialized by writing to this register to be started.

(4) Occurrence of the watchdog timer interrupt

- The watchdog timer interrupt occurs by underflow.

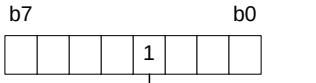
(5) Set the data for the software reset judgment.

- The contents of the internal RAM are preserved. Set the data for the software reset judgment in the internal RAM.

(Note) When power-on of hardware reset is operated, the internal RAM becomes indeterminate. Use at least 20 to 30 bytes of data space for the data for the software reset judgment to avoid the accidental coincidence of the internal RAM. The more data space to be used in the internal RAM is, the more reliable the judgment is. Also, each address should have a different value in the internal RAM to improve a reliability of the judgment.

(6) Set processor mode register 0 (PM0).

- Execute the software reset.



PM03 : software select bit
Setting this bit to "1" resets the microcomputer.

(Note) : When writing this register, set bit 0 in the protect register ($000A_{16}$ address) to "1".

(7) The reset of the microcomputer is executed.

(8) Judging whether the software reset or hardware reset is executed.

- Does the data for the software reset judgment in the internal RAM correspond with the data set in the process of (5) on the above?

Yes → the software reset

No → the hardware reset

(9) Clear the data for the software reset judgment.

- Clear the data for the next judgment.

(10) Start each processing for the hardware reset / the software reset.

Cautions

The judgment cannot be performed when the hardware reset is executed before the data for the software reset judgment is completely cleared and before the software reset is executed.

(The judgment cannot be performed when the hardware reset is executed during (5) to (9) on the above procedures.)

4.0 Program sample

```
/***********************************************************************/
/*      FILE NAME : rjj05b0289_src.c                                   */
/*      Ver       : 1.00                                               */
/*      CPU       : M16C/80                                            */
/*      FUNCTION  : The software reset judging method sample           */
/*---------------------------------------------------------------------*/
/*      Copyright(C)2003, Renesas Technology Corp.                     */
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/*                                                                     */
/***********************************************************************/
/****************************************/
/*      include file                    */
/****************************************/
#include "sfr80144.h"                   // SFR definition header

/****************************************/
/*      Section name change             */
/****************************************/
#pragma SECTION bss aaa                 // change the data section name(bss -> aaa)
#pragma SECTION program aaa_prog        // change the program section name


/****************************************/
/*      Global variable declaration     */
/****************************************/
unsigned char   wdt_flg[256];           // S/W-RESET decision table
unsigned char   reset_flg;              // S/W-RESET,H/W-RESET decision result
                                        //   0:S/W-RESET, 1:H/W-RESET

/****************************************/
/*      Function declaration            */
/****************************************/
void wdt_exe(void);
void ta0_init(void);
void ta0_int(void);
void wdt_int(void);
```

```
/************************************************************/
/*       main function                                      */
/*          The software reset judging method sample program      */
/************************************************************/
void main(void)
{
      pd10 = 0xff;                          // P10 is an outout port.
      pd8 = 0x1f;                           // P8_0-P8_4 are an outout port.
      pd6 = 0xff;                           // P6 is an outout port.
      p10 = 0;                              // port initialization.
      p8    = 0;                            //
      p6    = 1;                            //

      ta0_init();                           // TA0 initialization
      ta0s = 1;                             // TA0 start
      while(ir_ta0ic == 0)
      {
            ;                               // Timing adjustment
      }
      ta0s = 0;                             // TA0 stop

      wdt_exe();                            // S/W-RESET decision & WDT execution

      while(1)
      {
            p8_0    = !p8_0;                // monitor
      }
}

/***************************************/
/*       Timer-A0 initialization               */
/***************************************/
void ta0_init(void)
{
      ta0mr = 0x80;                         // Timer-mode(f32)
      ta0     = 0x8fff;                     // Timer-value set
```

```
    ta0ic = 0;                          // Interruption priority level = 0
}

/****************************************/
/*      S/W-RESET decision              */
/*      & WDT execution                 */
/****************************************/
void wdt_exe(void)
{
    int       i;
    p10 = wdt_flg[255];                 //

    reset_flg = 0;                      // S/W-RESET
    for (i=0;i<256;i++)
    {
        if(wdt_flg[i] != i)             // S/W-RESET decision table miss-match
        {
            reset_flg = 1;              // H/W-RESET
            break;
        }
    }
    memset(wdt_flg, 0x0, 5);            // S/W-RESET decision table "0" clear

    prcr = 7;                           // protect OFF
    cm06 = 0;                           // WDT chooses interruption.
    prcr = 0;                           // protect ON
    wdc  = 0x80;                        // Prescaler division ratio (128)
    wdts = 1;                           // WDT start
}

/****************************************/
/*      Timer-A0 interrupt routine      */
/****************************************/
#pragma INTERRUPT/B   ta0_int
void ta0_int(void)
{
    p6_3 = !p6_3;                       //
}
```

```
/****************************************/
/*      Watch-Dog-Timer interrupt routine */
/****************************************/
#pragma INTERRUPT/B    wdt_int
void wdt_int(void)
{
      int        i;

      for (i=0;i<256;i++)
      {
            wdt_flg[i] = i;                    // S/W-RESET decision table set
      }

      p8_4       = 1;

      ta0_init();
      ta0s = 1;                                // TA0 start
      while(ir_ta0ic == 0)
      {
            ;                                  // Timing adjustment
      }

      prcr = 7;                                // protect OFF
      pm03 = 1;                                // S/W-RESET execution
      prcr = 0;                                // protect ON
      while(1)
      {
            ;                                  //
      }
}
```

5.0 Reference

Datasheet

- Refer to M16C/80 Group datasheet.

(Acquire the most current version from Renesas Technology website)

6.0 Web-site and contact for support

Renesas Web-site

http://www.renesas.com

Contact for Renesas technical support

Mail to : support_apl@renesas.com

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
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