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H8S Family

Single-Master Mode Communications Using the I^{2}C Bus Interface (IIC)

Introduction

This application note describes the usage of the IIC module in single-master mode.

Target Device

H8S/2638

Contents

1. Specifications

- Figure 1 shows the connections for communications using I²C bus interface in single master mode. The slave addresses and settings for the SAR_0 registers of the individual devices are listed in table 1.
- The single master system in this sample task consists of one master device and one slave device.
- The I²C bus transfer clock rate is 100 k bit/s (kHz).

The following describes the procedures for the operation of this sample task.

1. The I²C bus interface single master transfer starts on the input of the low trigger to the $\overline{\text{IRQ0}}$ pin of the master.
2. The master transmits four bytes of data, which have been prepared in the on-chip ROM in advance, to the on-chip RAM on the slave side.
3. The slave device returns the four bytes of data received in step 2 from its on-chip RAM to the on-chip RAM on the master side.
4. The master device performs processing for random reading of the EEPROM. This includes the generation of a new start condition and reception of the single byte of data read out from the slave.
5. The master compares the received data in its on-chip RAM with the data transmitted from its on-chip ROM, and confirms whether the two match.
6. Based on the results of this comparison, the master outputs levels on the PE1 and PE0 pins that indicate the result of operations.

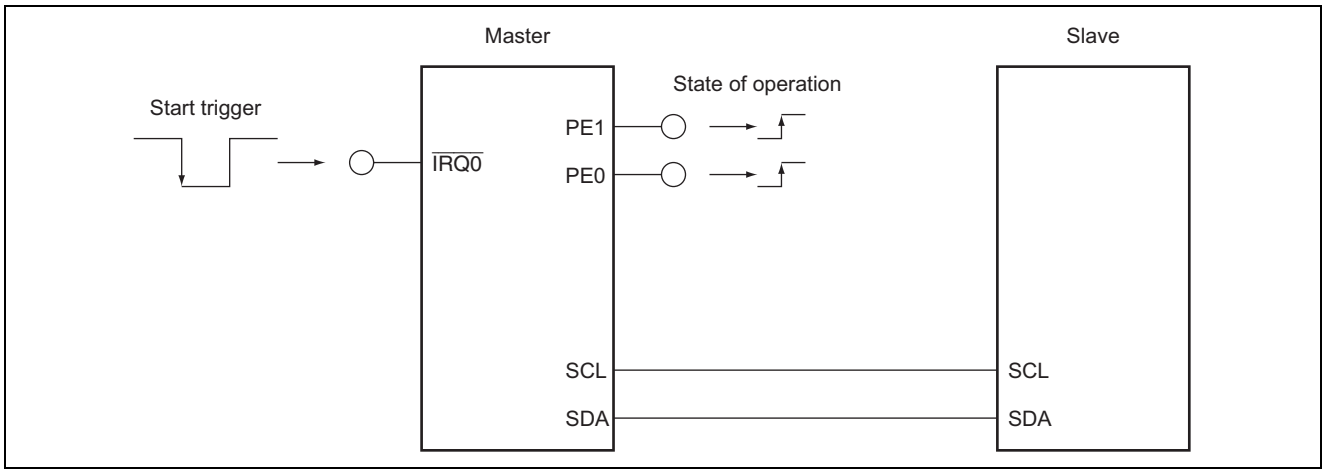


Figure 1 Connections for I²C Bus Interface Single Master Mode Communication

Table 1 Slave Addresses

Device	Slave Address	SAR_0 Setting
Master	1	H'02
Slave	3	H'06

2. Applicable Conditions

Table 2 Applicable Conditions

Items	Description	
Operating frequency	Input clock	20 MHz
	System clock (ϕ)	20 MHz
	Peripheral module clock	20 MHz
Mode of operation	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tools	High-performance Embedded Workshop, ver. 4.01.01	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler ver. 6.01.02, manufactured by Renesas Technology Corp.	
Compiler options	-cpu = 2000a:24, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 3 Section Settings

Address	Section	Description
H'001000	P	Program area
	C	Data table
H'FF6000	B	Non-initialized data area (RAM area)

3. Description of Functions

3.1 Description of I²C Bus Interface (IIC)

An I²C bus interface (IIC) is used in single master operation to demonstrate bidirectional communications in master mode.

3.2 Master Side $\overline{\text{IRQ0}}$ Pin

The trigger to start master transmission and master reception is input to the $\overline{\text{IRQ0}}$ pin on the master side. IRQ0 starts the processing of I²C bus interface communications on the input of a rising edge on the $\overline{\text{IRQ0}}$ pin.

The master judges whether or not the $\overline{\text{IRQ0}}$ pin has received the start trigger by polling the IRQ status flag. The IRQ interrupt is not used.

3.3 Master Side PE1 and PE0 Pins

As indicated in table 4, the pins PE1 and PE0 on the master side indicate the state of I²C bus interface communications (reset state or result of operations).

Table 4 Output Values of Master Side Pins and State of Operations

PE1	PE0	State of Operations
0	0	Reset
0	1	Data match
1	0	Data mismatch

4. Description of Operations

4.1 Timing of Operations in Master Transmit Mode

Figure 2 shows the timing of operations of the I²C bus interface in master transmit mode. Table 5 describes processing by hardware and software at the numbered points in figure 2.

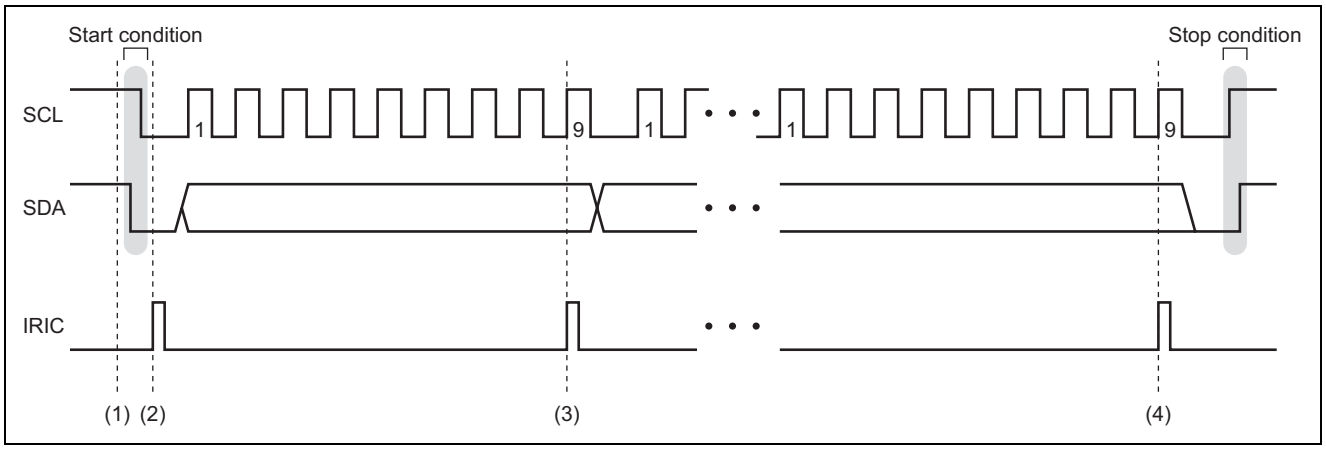


Figure 2 Timing of Operations in Master Transmit Mode

Table 5 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the IEIC bit to 1, enabling I²C bus interface interrupts. b. Issue the start condition.
(2)	a. I²C bus interface interrupt generation Start condition is detected and the IRIC bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDR, then transmit this data. b. Clear the IRIC flag.
(3)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1.	a. Write the data for transmission to ICDR and transmit the data. b. Clear the IRIC flag.
(4)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1.	a. Set the IEIC bit to 0, disabling I²C bus interface interrupts. b. Clear the IRIC flag. c. Issue the stop condition.

4.2 Master Receive Mode Operation Timing

Figures 3 and 4 show the timing of operations of the I²C bus interface in master receive mode. Tables 6 and 7 describe processing by hardware and software at the numbered points in figures 3 and 4.

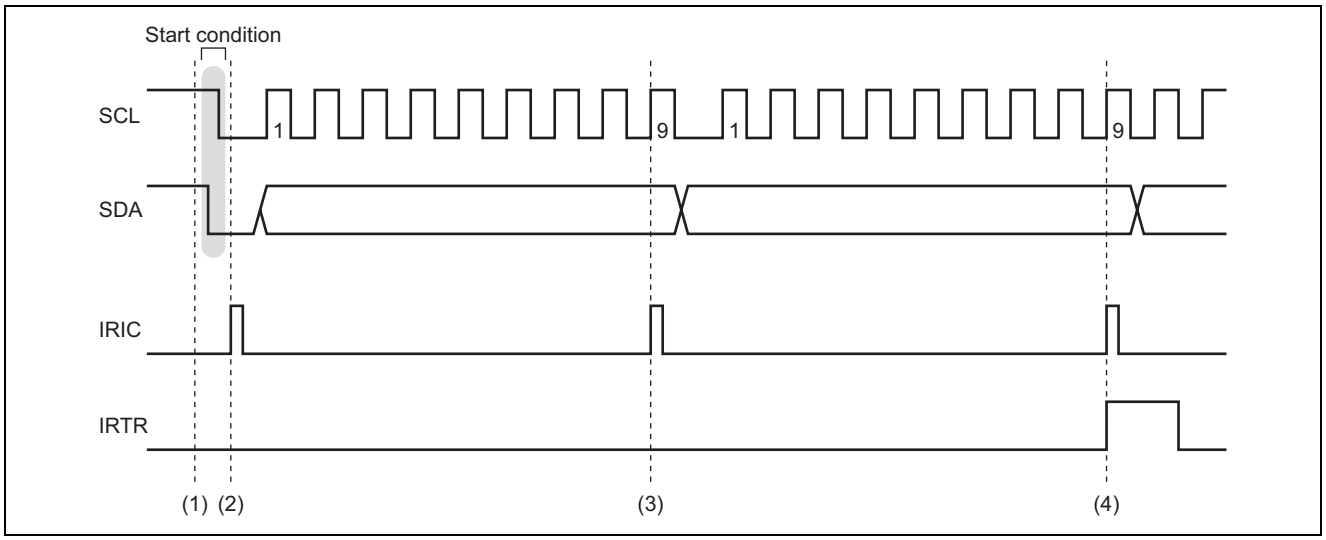


Figure 3 Master Receive Mode Operation Timing 1

Table 6 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the IEIC bit to 1, enabling I²C bus interface interrupts. b. Issue the start condition.
(2)	a. I²C bus interface interrupt generation Start condition is detected and the IRIC bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDR, then transmit this data. b. Clear the IRIC flag.
(3)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1.	a. Set the TRS bit to 0, selecting receive mode. b. Set the ACKB bit to 0 so that 0 is output at the time of acknowledge output. c. Clear the IRIC flag. d. Set the WAIT bit to 1; this inserts a wait between the data bits and the acknowledge bit. e. Execute a dummy read of ICDRR.
(4)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1. b. IRTR is set to 1. When the received data are transferred from ICDRS to ICDRR, both the RDRF and IRTR bits are set to 1.	a. Set the IRTR bit to 1 to read one byte of data from ICDR and store the data in RAM. b. Clear the IRIC flag (this also clears IRTR).

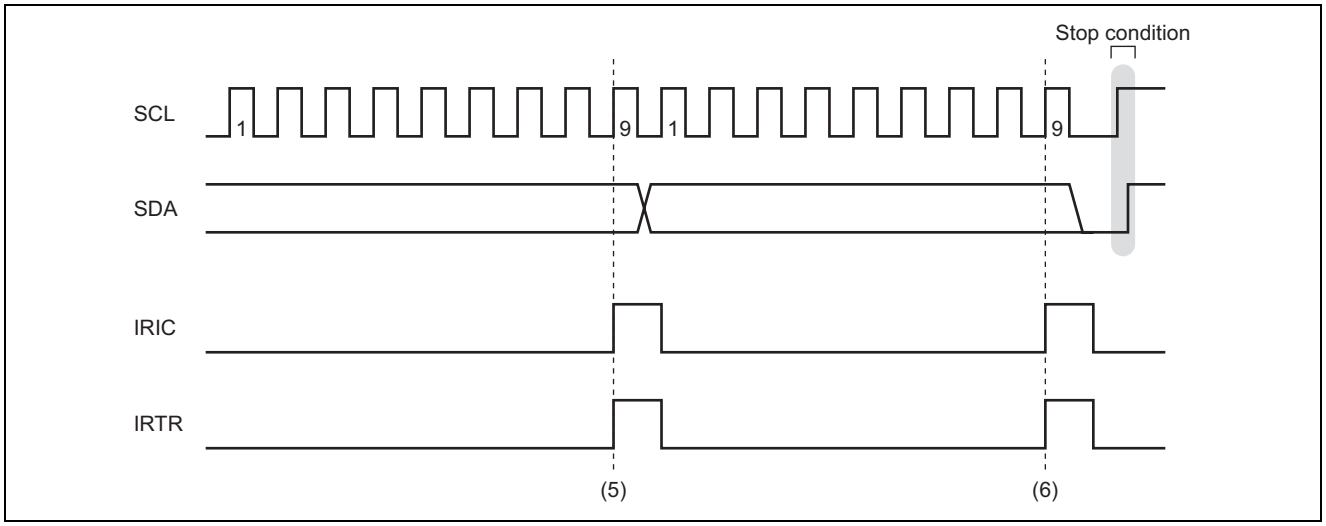


Figure 4 Master Receive Mode Operation Timing 2

Table 7 Description of Processing

	Hardware Processing	Software Processing
(5)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1. b. IRTR is set to 1. When the received data are transferred from ICDRS to ICDRR, both the RDRF and IRTR bits are set to 1.	a. Set the ACKB bit to 1, so that 1 is output at the timing of acknowledge output. b. Set the TRS bit to 1, selecting transmit mode so that the stop condition is output. c. Set the IRTR bit to 1 to read one byte of data from ICDR and store the data in RAM. d. Clear the IRIC flag (this also clears IRTR).
(6)	a. I²C bus interface interrupt generation On the rising edge of the ninth cycle of SCL, the IRIC bit is set to 1. b. IRTR is set to 1. When the received data are transferred from ICDRS to ICDRR, both the RDRF and IRTR bits are set to 1.	a. Set the WAIT bit to 0 to transfer the data and acknowledge bits consecutively. b. Clear the IRIC flag (this also clears IRTR). c. Set the IRTR bit to 1 to read the final data from ICDR and store the data in RAM. d. Issue the stop condition.

4.3 Random Read Waveform and Interrupt Timing

Figure 5 shows the timing of operations for the I²C bus interface in master transmit mode. Table 8 describes processing by hardware and software at the numbered points in figure 5.

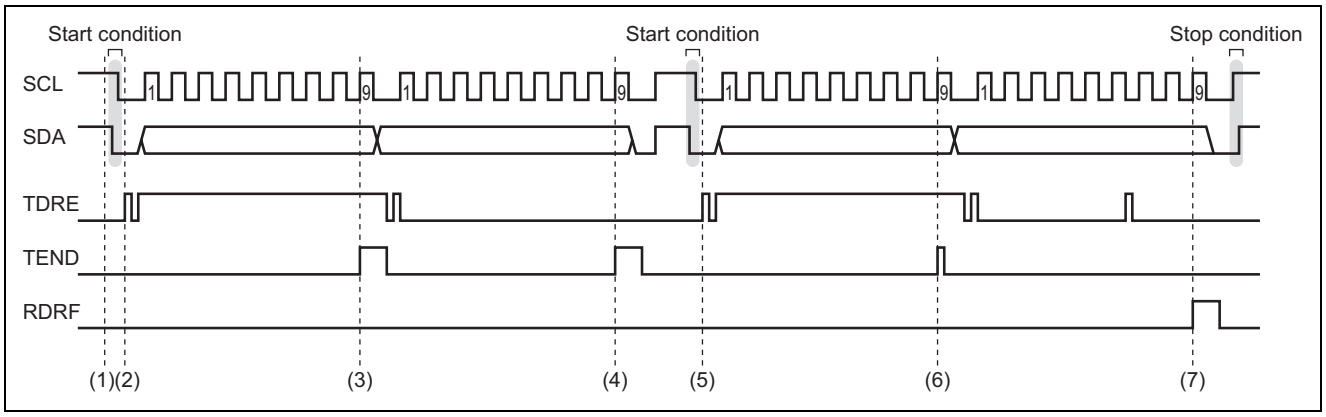


Figure 5 Timing of Operations in Master Transmit Mode

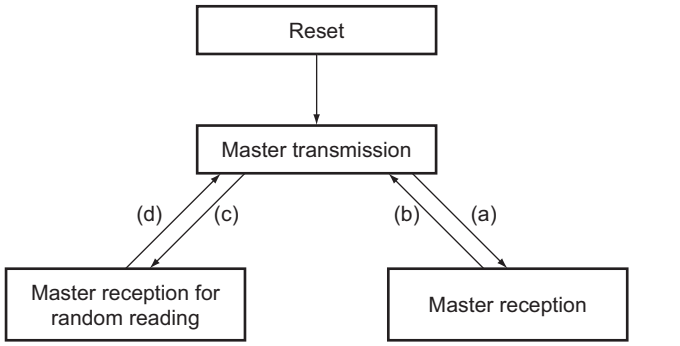
Table 8 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the TIE bit to 1, enabling the data-empty interrupt. Set the TDRE bit to 1 for interrupt generation. b. Issue the start condition.
(2)	a. Generation of transmit-data empty interrupt Start condition is detected and the TDRE bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. The interrupt will be generated when the TEND bit is 1.
(3)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Write the memory address to ICDRT and transmit the data. Writing to ICDRT clears the TDRE and TEND flags.
(4)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Set the TIE bit to 1, enabling the data-empty interrupt. Set the TDRE bit to 1 to generate the interrupt. b. Set the TEIE bit to 0, disabling the transmit-end interrupt. c. Clear the TEND flag. d. Confirm that the SCL signal is at the low level and then issue the start condition.
(5)	a. Generation of transmit-data empty interrupt Start condition is detected and the TDRE bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. The interrupt will be generated when the TEND bit is 1.

	Hardware Processing	Software Processing
(6)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Set the TIE bit to 0, disabling the transmit-end interrupt. b. Set the RIE bit to 1, enabling the receive-data full interrupt. c. Clear the TEND flag. d. Set the TRS bit to 0: Selects receive mode. e. Set the ACKBT bit to 1: Outputs 1 at the timing of acknowledge output in receive mode. f. Execute a dummy read of ICDRR; this clears RDRF.
(7)	a. Generation of receive-data interrupt Since the data have been transferred from ICDRS to ICDRR, the RDRF bit is set to 1.	a. Read the final byte of received data from ICDRR and store the data in RAM. Reading ICDRR clears RDRF. b. Set the RIE bit to 0, disabling the receive-data full interrupt. c. Clear the TEND flag. d. Confirm that the SCL signal is at the low level and then issue the start condition.

4.4 State Transition Diagram

Figure 6 is a state-transition diagram for this sample task. In this sample task, the master transmit mode is selected as the default. After a reset and when I²C bus interface transfer is in the idle state, the state transition is to the master transmit mode.



(a) Transition initiated by software instruction
(b) Transition on completion of reception or an error in communications
(c) Transition initiated by software instructions
(d) Transition on completion of reception or an error in communications

Figure 6 State Transition Diagram

5. Description of Software

5.1 List of Functions

Table 9 List of Functions: main.c

Function	Description
init	Initialization routine Sets the CCR and clock, releases IIC module 0 from module stop mode, and calls function "main".
main	Main routine Selects master mode operation, judges the state of the $\overline{\text{IRQ0}}$ pin, and handles master-transmission/reception processing.

Table 10 List of Functions: iic.c

Function	Description
iic_init	I²C bus interface initialization routine
mtrs_start	Sets I²C bus interface master transmission. Issues the start condition.
mrcv_start	Sets I²C bus interface master reception. Issues the start condition.
mrandrd_start	Sets random reading. Issues the start condition.
iici0_int	Handler for I²C bus interface interrupts. According to the state of operations, the functions for receiving the stop condition, master transmission, master reception, and random-reading are called from this function.
receive_stop_condition	Detects the stop condition.
master_transfer	When the state of operation of this sample task is master transmission, this function for master transmission processing is called from the I²C bus interface interrupt handler. One byte of data is transferred per call of this function.
master_receive	When the state of operation of this sample task is master reception, this function for master-reception processing is called from the I²C bus interface interrupt handler. One byte of data is received per call of this function.
master_randomread	When the state of operation of this sample task is random-reading, this function for random-reading is called from the I²C bus interface interrupt. The function transmits the specified address and receives the byte of data from that address.

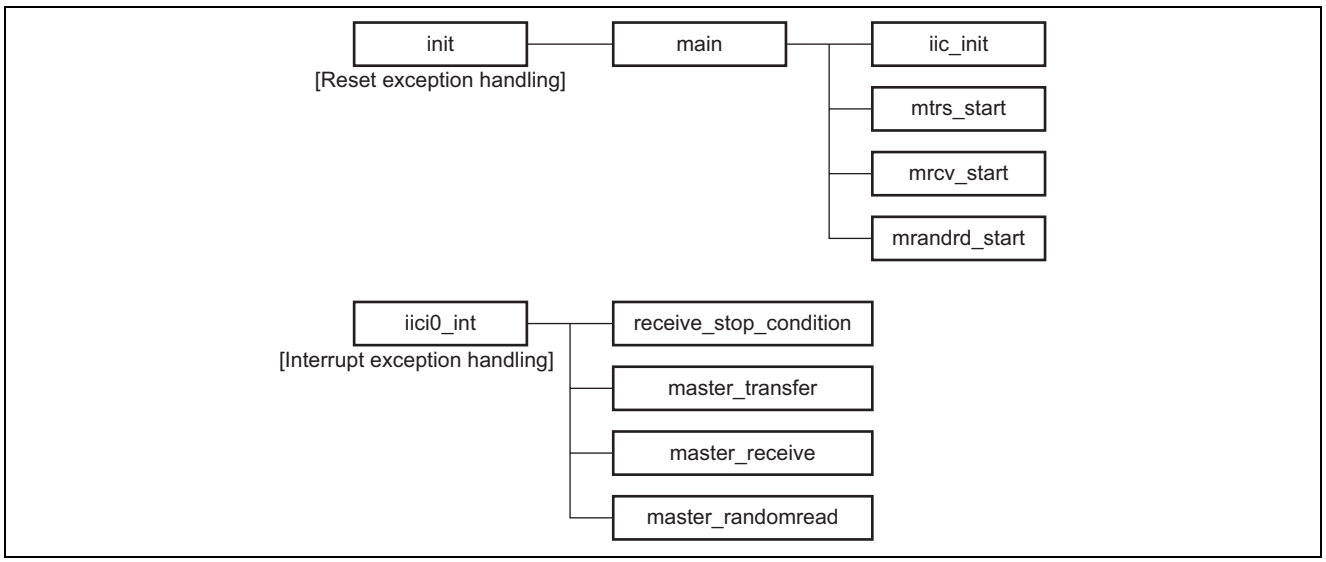


Figure 7 Hierarchy of Calls in the User Program

5.2 Vector Table

Table 11 Exception-Handling Vector Table

Origin of Exception	Vector Number	Vector Table Address	Target Function of the Vector
Task "Reset"	0	H'000000	main
IICI0 interrupt	116	H'0001D0	iici0_int

5.3 RAM Usage

Table 12 Description of RAM Usage

Type	Name of Variable	Description	Usage in Functions
unsigned char	iic_mode	Sets state of processing by this sample task.	iic_init mtrs_start mrcv_start mrandrd_start iici0_int receive_stop_condition
unsigned short	mt_cnt	Counter used for master transmission	main iic_init mtcv_start master_transfer
unsigned short	mr_cnt	Counter used for master reception	main iic_init mrcv_start master_receive
unsigned char	randrd_cnt	Counter used for random reading	main iic_init mrandrd_start master_randomread
unsigned short	mt_num	Number of bytes for master transmission	mtrs_start master_transfer
unsigned short	mr_num	Number of bytes for master reception	mrcv_start master_receive
unsigned char	*mt_data	Pointer to data for transmission	mtrs_start mrandrd_start master_transfer master_randomread
unsigned char	*mr_data	Pointer to received data	mrcv_start mrandrd_start master_receive master_randomread
unsigned char	MemAddress	Memory area used to set the address of the data for random reading from the EEPROM area	mrandrd_start
unsigned char	MRcv_dt[4]	Master-side reception area	main

5.4 Constants

Table 13 Constants

Type	Name of Variable	Setting	Description	Usage in Function
unsigned char	MTrs_dt[4]	H'81, H'01, H'02, H'03	Data for master transmission	main

5.5 Macro Constants

Table 14 Macro Constants

Name of Variable	Setting	Description	Function Used
DTNUM	4	Number of data for transmission/reception	main
SLAVE_ADDR	H'02	Slave address	iic_init
MT_ID	H'06	Slave address + R/$\overline{W}$ bit for master transmission Slave-side slave address + 0 (transmission to the slave)	master_transfer master_randomread
MR_ID	H'07	Slave address + R/$\overline{W}$ bit for master reception Slave-side slave address + 1 (reception from the slave)	master_receive master_randomread
MODE_MR_RAND	4	State of processing of this sample task: Random-read mode	mrandrd_start iici0_int
MODE_MT	3	State of processing of this sample task: Master transmission	iic_init mtrs_start iici0_int receive_stop_condition
MODE_MR	2	State of processing of this sample task: Master reception	mrcv_start iici0_int

5.6 Functions of File main.c

5.6.1 Function init

1. Overview
   This initialization routine releases I²C bus interface 0 from module stop mode, sets the clock, and calls function "main".
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- System Clock Control Register (SCKCR) Address: H'FFFDE6

Bit	Bit Name	Setting	R/W	Function
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select the bus timer clock.
0	SCK0	0	R/W	000: Bus master in high-speed mode

- Low-Power Control Register (LPWRCR) Address: H'FFFDEC

Bit	Bit Name	Setting	R/W	Function
1	STC1	0	R/W	System Clock Select 2 to 0
0	STC0	0	R/W	Specify the frequency multiplier for the PLL circuit. 00: x1

- Mode Control Register (MDCR) Address: H'FFFDE7

Bit	Bit Name	Setting	R/W	Function
2	MDS2	—*	R	Mode Select 2 to 0
1	MDS1	—*	R	Indicate the input levels at pins MD2 to MD0 (the current operating mode). Bits MDS2 to MDS0 correspond to pins MD2 to MD0. MDS2 to MDS0 are read-only bits, and cannot be modified. The levels being input on the mode pins (MD2 to MD0) are latched into these bits when MDCR is read. The latching is released by a power-on reset.
0	MDS0	—*	R	

Note: * Determined by the levels on pins MD2 to MD0.

MSTPCRA, MSTPCRB, MSTPCRC, and MSTPCRD control the module stop mode. Setting a bit in these registers places the corresponding module in the module stop mode. Clearing a bit takes the module out of module stop mode.

- Module Stop Control Register A (MSTPCRA) Address: H'FFFDE8

Bit	Bit Name	Setting	R/W	Function
6	MSTPA6	1	R/W	Data transfer controller (DTC)
5	MSTPA5	1	R/W	16-bit timer pulse unit (TPU)
3	MSTPA3	1	R/W	Programmable pulse generator (PPG)
2	MSTPA2	1	R/W	D/A converter (channels 0, 1)
1	MSTPA1	1	R/W	A/D converter

- Module Stop Control Register B (MSTPCRB) Address: H'FFFDE9

Bit	Bit Name	Setting	R/W	Function
7	MSTPB7	1	R/W	Serial communication interface_0 (SCI_0)
6	MSTPB6	1	R/W	Serial communication interface_1 (SCI_1)
5	MSTPB5	1	R/W	Serial communication interface_2 (SCI_2)
4	MSTPB4	0	R/W	I²C bus interface_0 (IIC_0)
3	MSTPB3	1	R/W	I²C bus interface_1 (IIC_1)

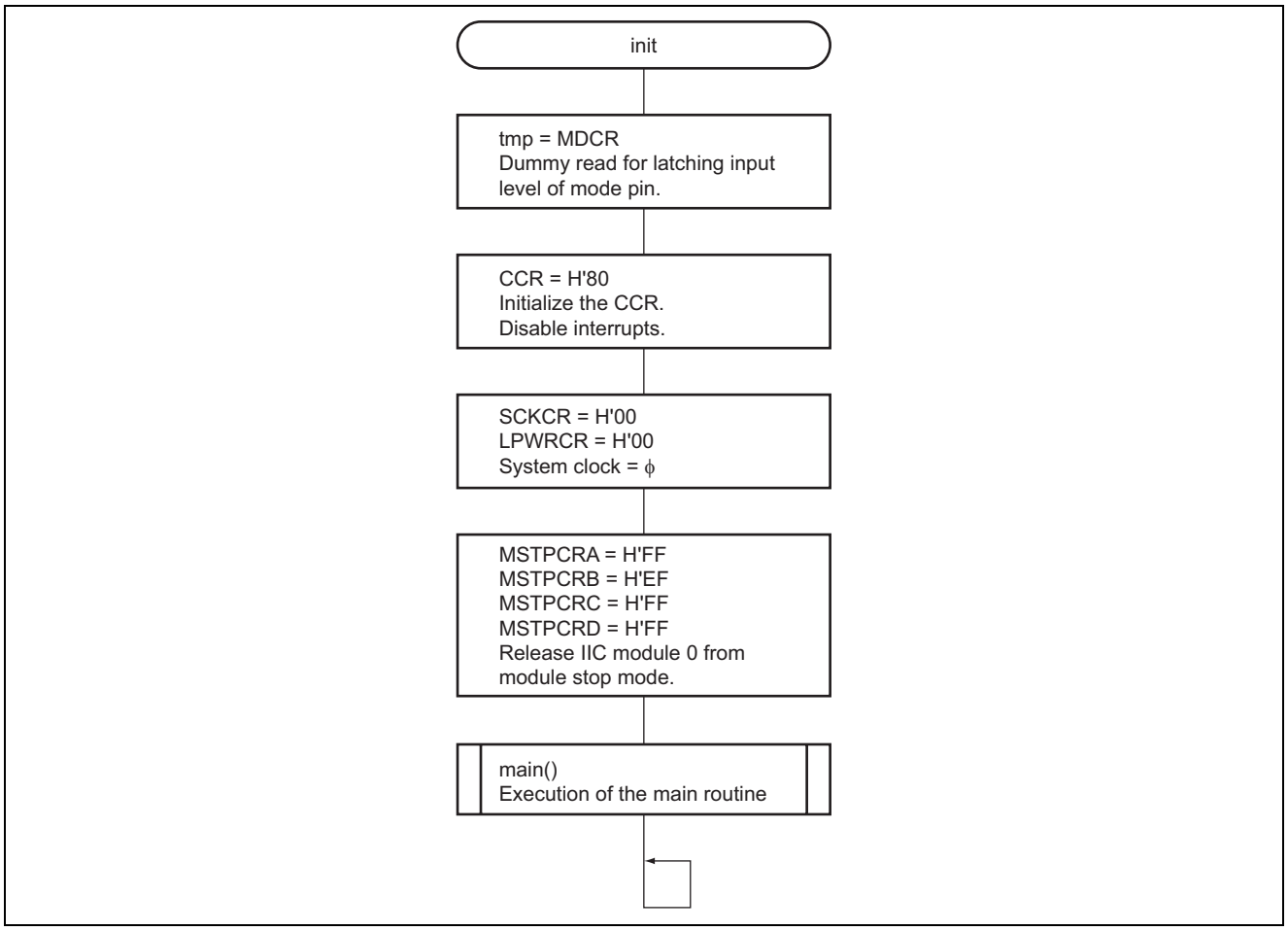
- Module Stop Control Register C (MSTPCRC) Address: H'FFFDEA

Bit	Bit Name	Setting	R/W	Function
4	MSTPC4	1	R/W	PC break controller (PBC)
3	MSTPC3	1	R/W	HCAN0
2	MSTPC2	1	R/W	HCAN1

- Module Stop Control Register D (MSTPCRD) Address: H'FFFC60

Bit	Bit Name	Setting	R/W	Function
7	MSTPD7	1	R/W	Motor control PWM (PWM)

5. Flow Chart


init
tmp = MDCR
Dummy read for latching input level of mode pin.
CCR = H'80
Initialize the CCR.
Disable interrupts.
SCKCR = H'00
LPWRCR = H'00
System clock = ϕ
MSTPCRA = H'FF
MSTPCRB = H'EF
MSTPCRC = H'FF
MSTPCRD = H'FF
Release IIC module 0 from module stop mode.
main()
Execution of the main routine

5.6.2 Function main

1. Overview
   — On falling edges of the $\overline{\text{IRQ0}}$ signal, this function performs 4-byte master transmission, 4-byte master reception, and 1-byte random reading.
   — Compares the master-transmission data with the master-reception data, and outputs an indicator of the results of comparison to pins PE1 and PE0.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used for this sample task, and are not initial settings.

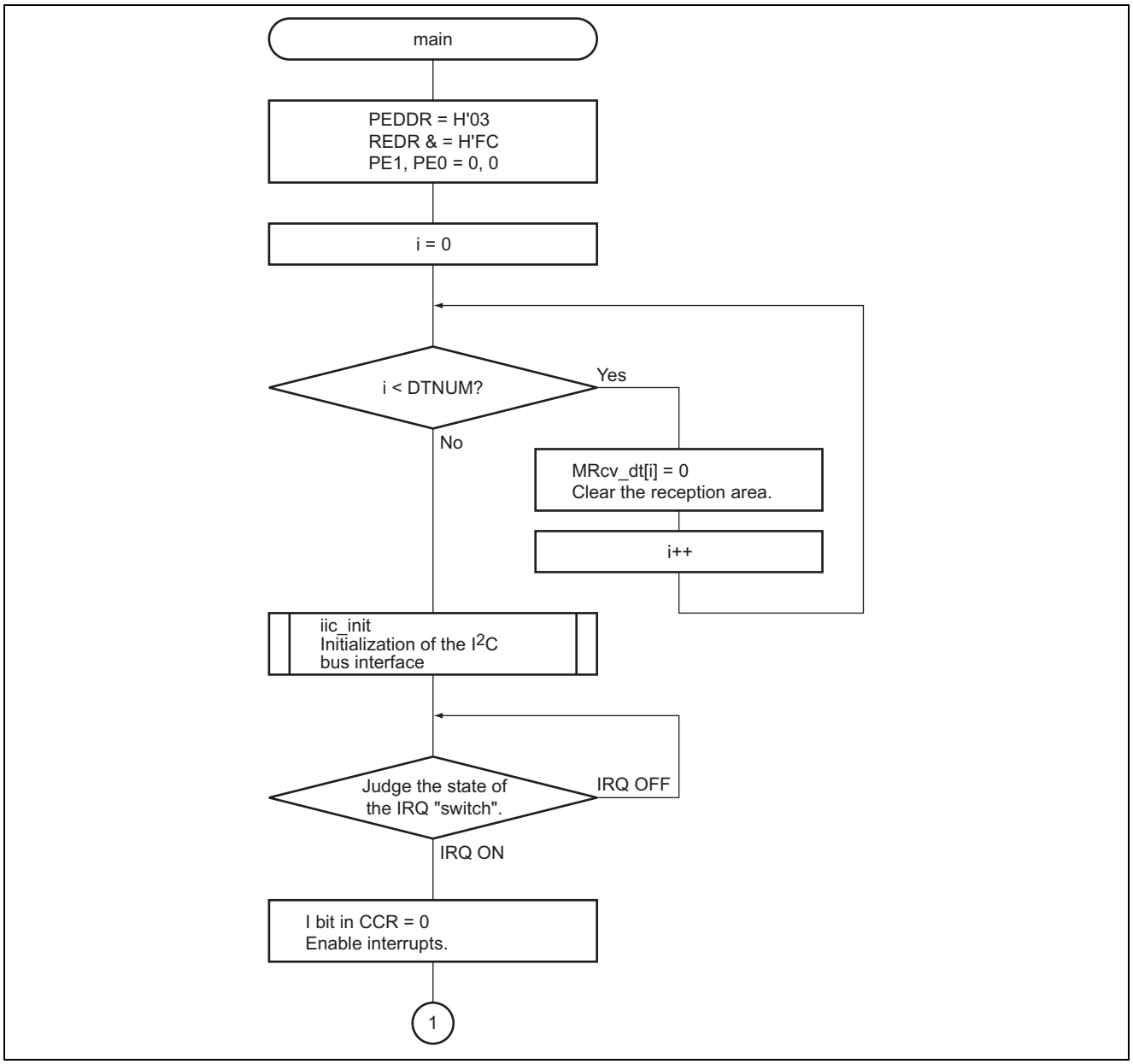
- Port E Data Direction Register (PEDDR) Address: H'FFFE3D

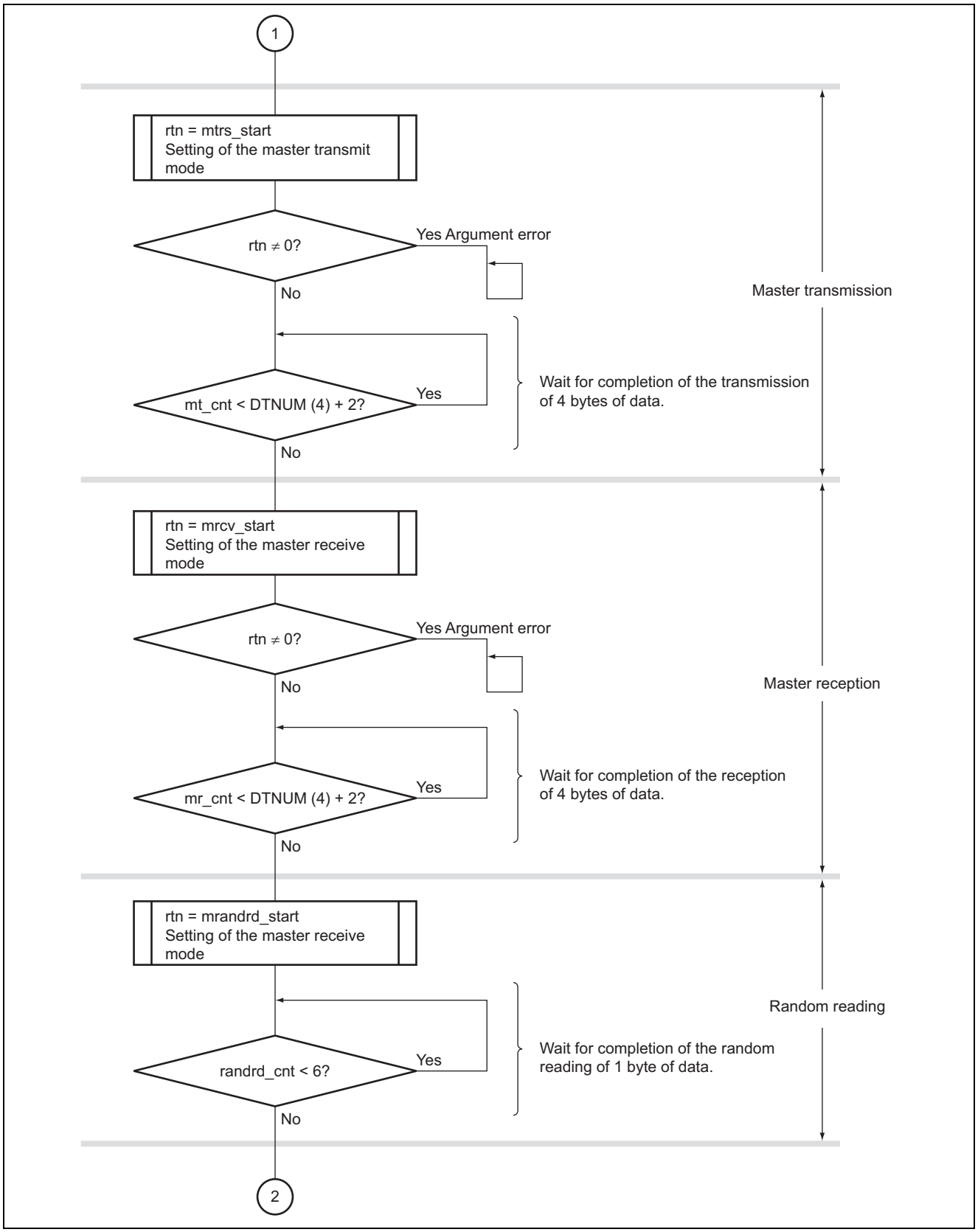
Bit	Bit Name	Setting	R/W	Function
1	PE1DDR	1	R/W	0: Sets the PE1 pin as an input pin. 1: Sets the PE1 pin as an output pin.
0	PE0DDR	1	R/W	0: Sets the PE0 pin as an input pin. 1: Sets the PE0 pin as an output pin.

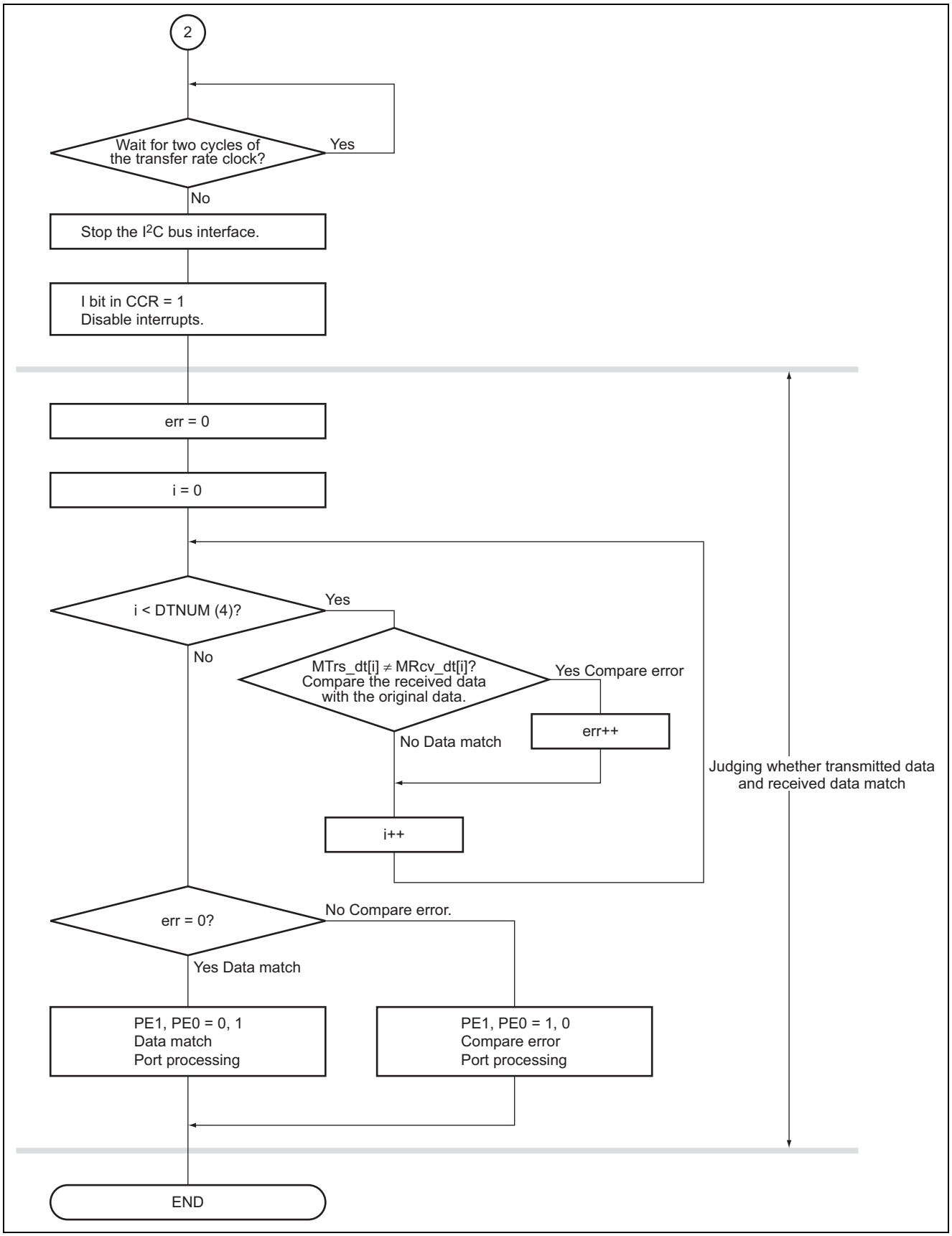
- Port E Data Register (PEDR) Address: H'FFFF0D

Bit	Bit Name	Setting	R/W	Function
1	PE1DR	0/1	R/W	0: Sets PE1 pin to the low level. 1: Sets PE1 pin to the high level.
0	PE0DR	0/1	R/W	0: Sets PE0 pin to the low level. 1: Sets PE0 pin to the high level.

5. Flow Chart


main
PEDDR = H'03
REDR & = H'FC
PE1, PE0 = 0, 0
i = 0
i < DTNUM?
Yes
No
MRcv_dt[i] = 0
Clear the reception area.
i++
iic_init
Initialization of the I2C
bus interface
Judge the state of
the IRQ "switch".
IRQ OFF
IRQ ON
I bit in CCR = 0
Enable interrupts.
1


1
rtn = mtrs_start
Setting of the master transmit mode
rtn ≠ 0?
Yes Argument error
No
mt_cnt < DTNUM (4) + 2?
Yes
No
Wait for completion of the transmission of 4 bytes of data.
Master transmission
rtn = mrcv_start
Setting of the master receive mode
rtn ≠ 0?
Yes Argument error
No
mr_cnt < DTNUM (4) + 2?
Yes
No
Wait for completion of the reception of 4 bytes of data.
Master reception
rtn = mrandrd_start
Setting of the master receive mode
randrd_cnt < 6?
Yes
No
Wait for completion of the random reading of 1 byte of data.
Random reading
2


2
Wait for two cycles of the transfer rate clock?
Yes
No
Stop the I²C bus interface.
I bit in CCR = 1
Disable interrupts.
err = 0
i = 0
i < DTNUM (4)?
Yes
No
MTrs_dt[i] ≠ MRcv_dt[i]?
Compare the received data with the original data.
Yes Compare error
err++
No Data match
i++
Judging whether transmitted data and received data match
err = 0?
No Compare error.
Yes Data match
PE1, PE0 = 0, 1
Data match
Port processing
PE1, PE0 = 1, 0
Compare error
Port processing
END

5.7 Functions of File iic.c

5.7.1 Function iic_init

1. Overview
   I²C bus interface initialization routine
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- Serial Control Register X (SCRX) Address: H'FFFDB4

Bit	Bit Name	Setting	R/W	Function
5	IICX0	1	R/W	I²C Bus Transfer Select 1, 0 In combination with bits CKS2 to CKS0 in ICMR, this bit selects the transfer rate in master mode.
4	IICE	1	R/W	I²C Bus Master Enable 0: Disables CPU access to the I²C bus interface data and control registers. 1: Enables CPU access to the I²C bus interface data and control registers.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78[*1]

Bit	Bit Name	Setting	R/W	Function
7	ICE	0/1	R/W	I²C Bus Interface Enable 0: Disables the IIC module and initializes its internal state. SAR and SARX can be accessed. 1: Enables transfer via the IIC module (pins SCL and SDA are driving the bus). ICMR and ICDR can be accessed.
6	IEIC	1	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	Transmit/Receive Select 00: Slave receive mode
3	ACKE	0/1	R/W	Acknowledge Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)[*2]	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	1	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. 1: The SCP bit is always read as 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79[*1]

Bit	Bit Name	Setting	R/W	Function
2	AAS	0	R/(W)[*2]	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 when the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or when the general call address (H'00) is detected. [Setting condition] • Detection of the slave address in slave receive mode when FS = 0 • Detection of the general address in slave receive mode when FS = 0 [Clearing condition] • Writing of data to ICDR (transmit mode) or reading of data from ICDR (receive mode) • Writing of 0 to this bit after reading it as 1 • Transition to master mode
0	ACKB	0	R/W	Acknowledge Bit In receive mode, sets the value of the bit to be returned at acknowledge timing here. 0: Returns 0 as acknowledge data. 1: Returns 1 as acknowledge data.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Mode Register_0 (ICMR_0) Address: H'FFFF7F[*1]

Bit	Bit Name	Setting	R/W	Function
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first
6	WAIT	0	R/W	Wait Insertion Bit 0: Transfers data and acknowledge bits consecutively 1: Inserts a wait between the data bits and acknowledge bit.
5	CKS2	1	R/W	Serial Clock Select Transfer rate is 100 kbps with ϕ = 20 MHz when IICX0 = 1 in the SCRX register, CKS2 = 1, CKS1 = 0, and CKS0 = 1.
4	CKS1	0	R/W	
3	CKS0	1	R/W	
2	BC2	0	R/W	Bit Counter Specify the number of bits to be transferred next. 000: 9 bits
1	BC1	0	R/W	
0	BC0	0	R/W	

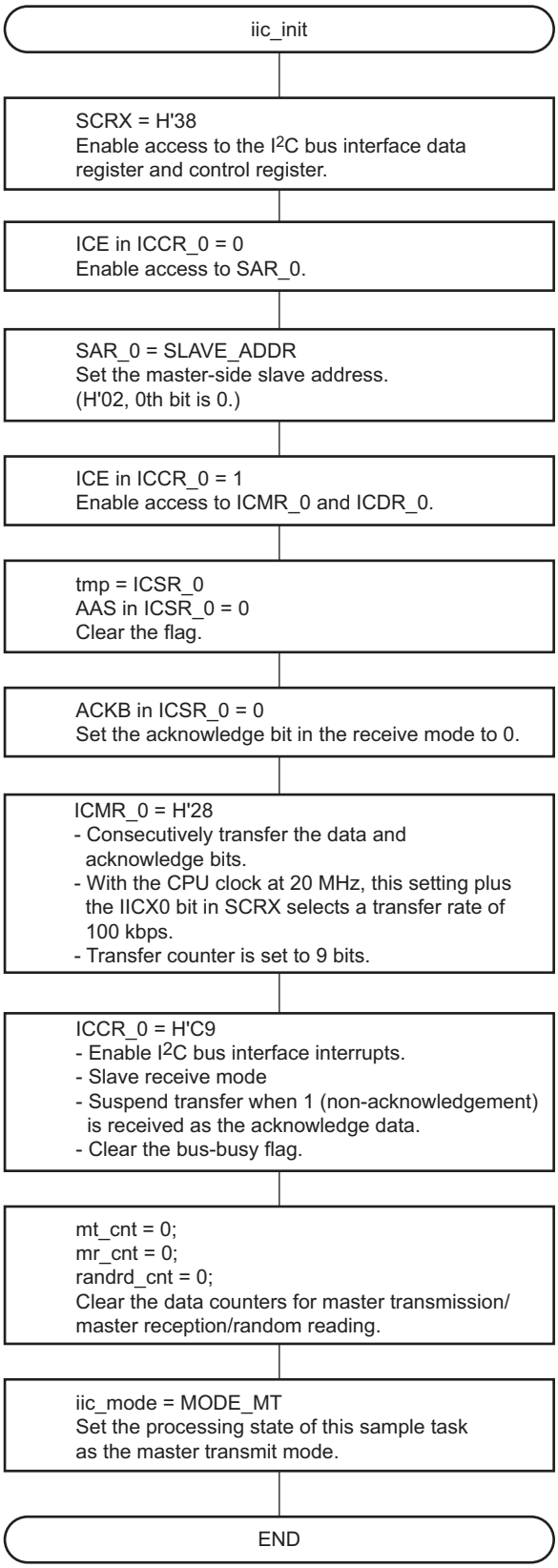
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

- Slave Address Register_0 (SAR_0) Address: H'FFFF7F[*1]
  The slave address is set in the SAR bits. An interface in slave mode responds as the slave device when the 7 higher-order bits of SAR match the 7 higher-order bits of the first frame received after a start condition. SAR is assigned to the same address as ICMR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

Bit	Bit Name	Setting	R/W	Function
7 to 1	SVA6 to SVA0	SLAVE_ADDR	R/W	Slave Address 6 to 0 Unique address setting (address differing from the addresses of other slave devices connected to the I²C bus) for the device
0	FS		R/W	Format Select Selects recognition of the slave address in the higher-order bits of SAR.

Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

5. Flow Chart


iic_init
SCRX = H'38
Enable access to the I²C bus interface data register and control register.
ICE in ICCR_0 = 0
Enable access to SAR_0.
SAR_0 = SLAVE_ADDR
Set the master-side slave address.
(H'02, 0th bit is 0.)
ICE in ICCR_0 = 1
Enable access to ICMR_0 and ICDR_0.
tmp = ICSR_0
AAS in ICSR_0 = 0
Clear the flag.
ACKB in ICSR_0 = 0
Set the acknowledge bit in the receive mode to 0.
ICMR_0 = H'28
- Consecutively transfer the data and acknowledge bits.
- With the CPU clock at 20 MHz, this setting plus the IICX0 bit in SCRX selects a transfer rate of 100 kbps.
- Transfer counter is set to 9 bits.
ICCR_0 = H'C9
- Enable I²C bus interface interrupts.
- Slave receive mode
- Suspend transfer when 1 (non-acknowledgement) is received as the acknowledge data.
- Clear the bus-busy flag.
mt_cnt = 0;
mr_cnt = 0;
randrd_cnt = 0;
Clear the data counters for master transmission/ master reception/random reading.
iic_mode = MODE_MT
Set the processing state of this sample task as the master transmit mode.
END

5.7.2 Function mtrs_start

1. Overview

   This function sets up the task for I²C bus interface master transmission and issues the start condition.

2. Arguments

Type	Name of Variable	Description
const unsigned char	*dtadd	First address of data for transmission
unsigned short	dtnum	Number of data (bytes) to be transmitted

3. Return value

Type	Description
unsigned char	0: Arguments were normal. 1: Arguments were abnormal.

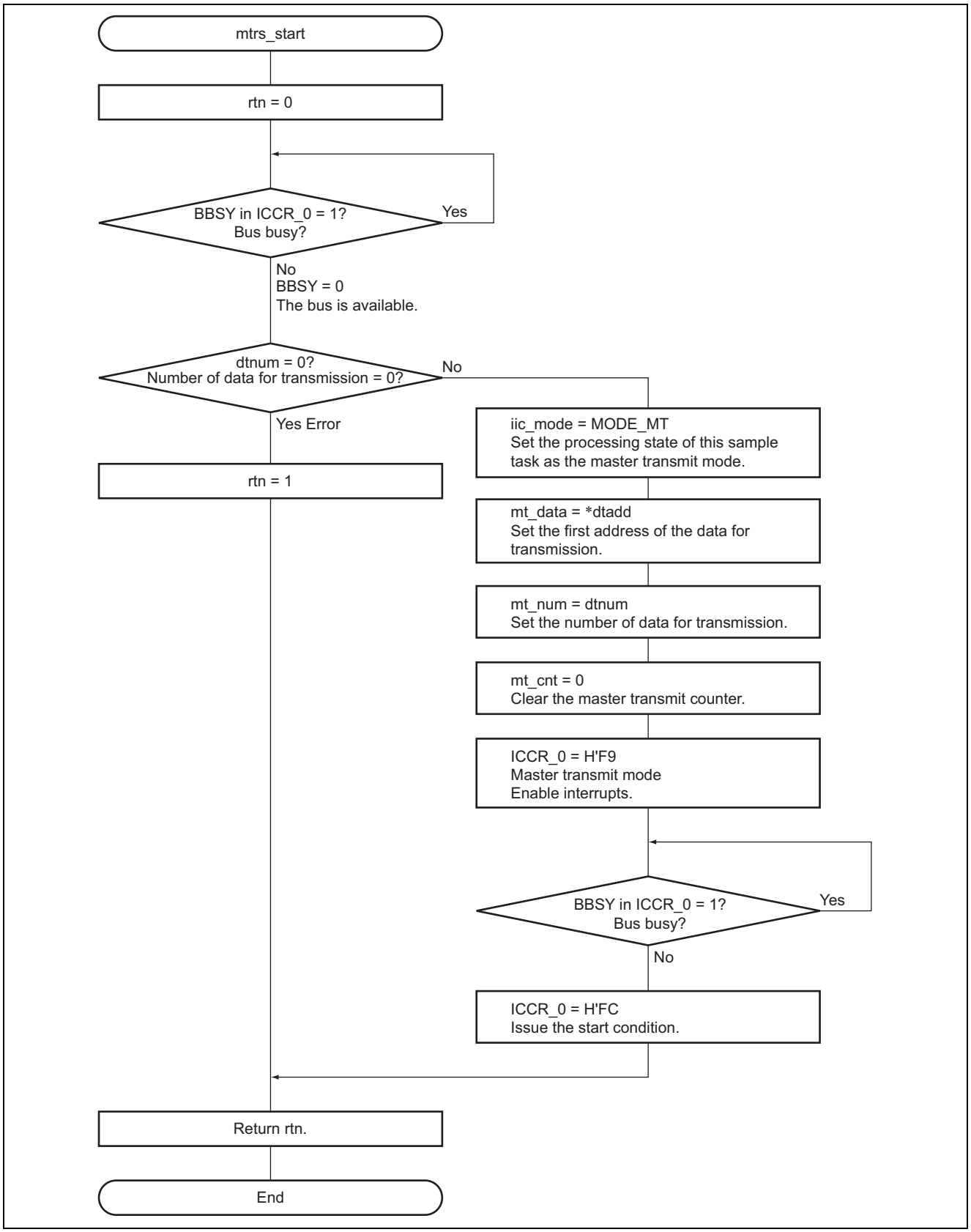
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78[*1]

Bit	Bit Name	Setting	R/W	Function
6	IEIC	1	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	Transmit/Receive Select 11: Master transmit mode
3	ACKE	1	R/W	Acknowledge Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0/1	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)[*2]	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	1/0	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. The start condition is issued when BBSY = 1 and SCP = 0. 1: This bit is always read as 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

5. Flow Chart


mtrs_start
rtn = 0
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
dtnum = 0?
Number of data for transmission = 0?
No
Yes Error
rtn = 1
iic_mode = MODE_MT
Set the processing state of this sample task as the master transmit mode.
mt_data = *dtadd
Set the first address of the data for transmission.
mt_num = dtnum
Set the number of data for transmission.
mt_cnt = 0
Clear the master transmit counter.
ICCR_0 = H'F9
Master transmit mode
Enable interrupts.
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
ICCR_0 = H'FC
Issue the start condition.
Return rtn.
End

5.7.3 Function mrcv_start

1. Overview
   This function sets up the task for I²C bus interface master reception and issues the start condition.
2. Arguments

Type	Name of Variable	Description
const unsigned char	*dtadd	First address of received data
unsigned short	dtnum	Number of data (bytes) received

3. Return value

Type	Description
unsigned char	0: Arguments were normal. 1: Arguments were abnormal.

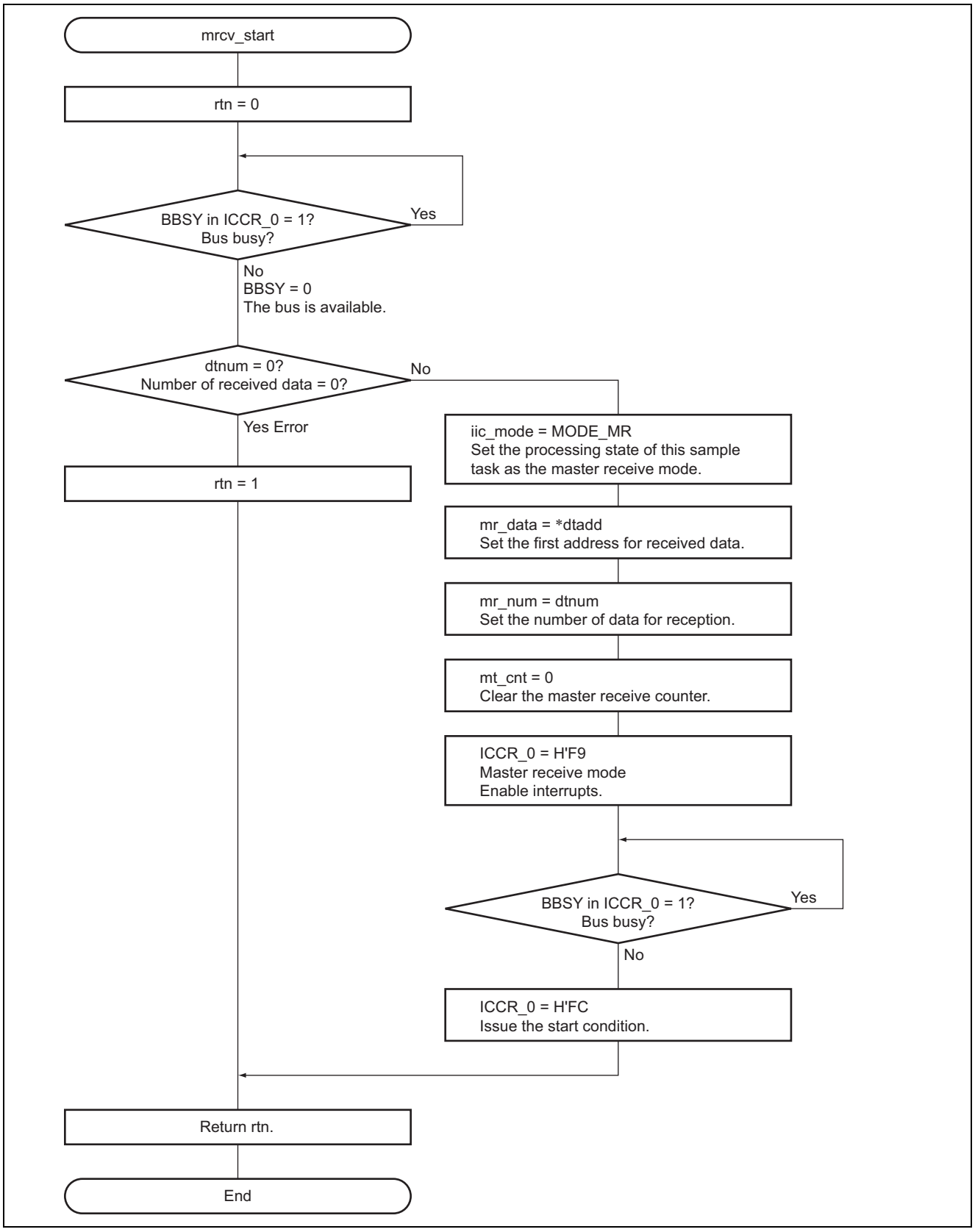
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78[*1]

Bit	Bit Name	Setting	R/W	Function
6	IEIC	1	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	Transmit/Receive Select 11: Master transmit mode
3	ACKE	1	R/W	Acknowledge Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0/1	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)[*2]	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	1/0	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. The start condition is issued when BBSY = 1 and SCP = 0. 1: This bit is always read as 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

5. Flow Chart


mrcv_start
rtn = 0
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
dtnum = 0?
Number of received data = 0?
No
Yes Error
rtn = 1
iic_mode = MODE_MR
Set the processing state of this sample task as the master receive mode.
mr_data = *dtadd
Set the first address for received data.
mr_num = dtnum
Set the number of data for reception.
mt_cnt = 0
Clear the master receive counter.
ICCR_0 = H'F9
Master receive mode
Enable interrupts.
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
ICCR_0 = H'FC
Issue the start condition.
Return rtn.
End

5.7.4 Function mrandrd_start

1. Overview
   This function sets up the task for random reading, including generation of a start condition to initiate reading from the EEPROM.
2. Arguments

Type	Name of Variable	Description
const unsigned char	*mrbuf	Location where the random-read data is to be stored
unsigned short	mtbuf	EEPROM memory address

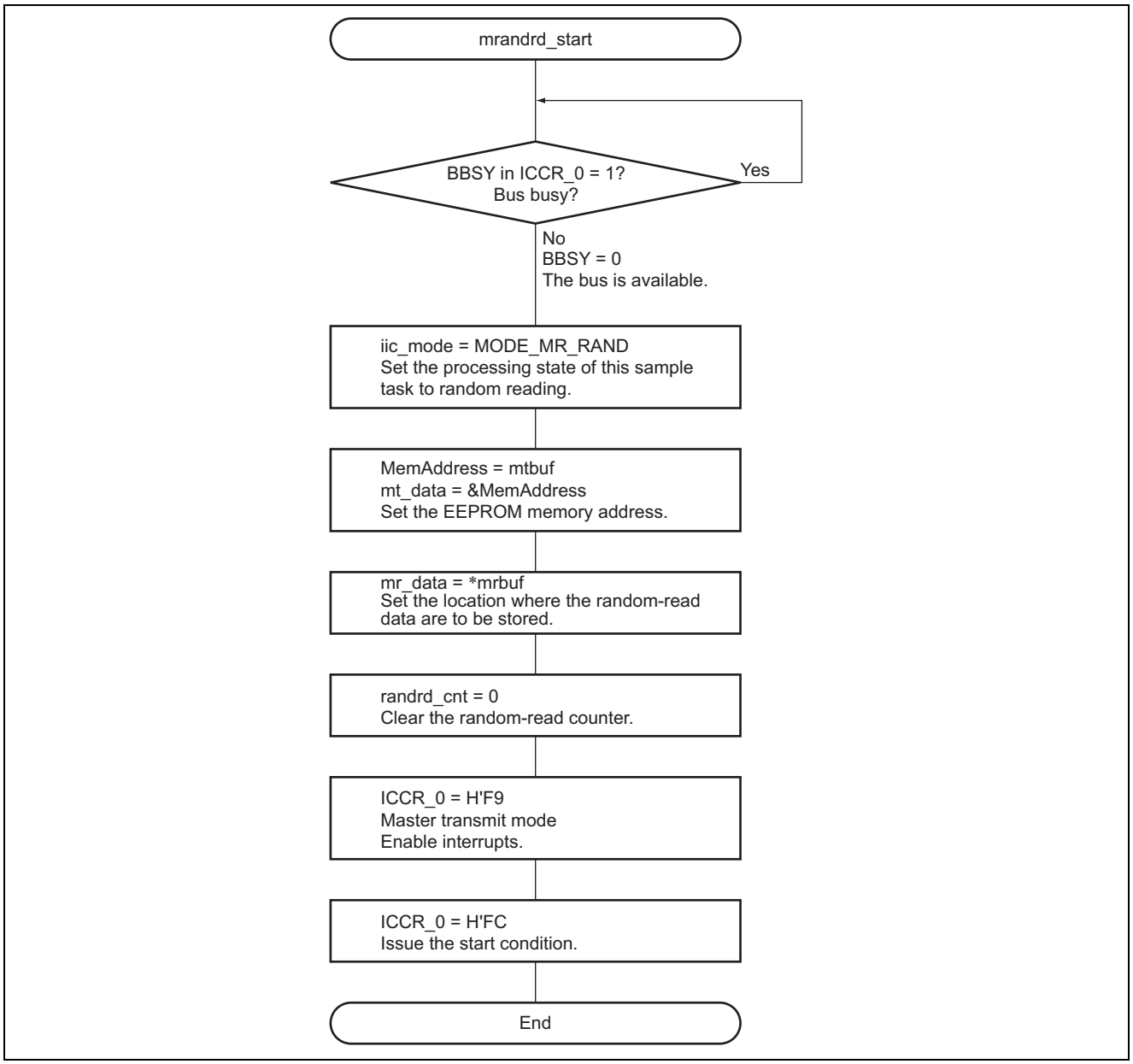
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78*1

Bit	Bit Name	Setting	R/W	Function
6	IEIC	1	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	Transmit/Receive Select 11: Master transmit mode
3	ACKE	1	R/W	Acknowledge Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0/1	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)*2	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	1/0	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. The start condition is issued when BBSY = 1, SCP = 0. 1: This bit is always read as 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

5. Flow Chart


mrandrd_start
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
iic_mode = MODE_MR_RAND
Set the processing state of this sample task to random reading.
MemAddress = mtbuf
mt_data = &MemAddress
Set the EEPROM memory address.
mr_data = *mrbuf
Set the location where the random-read data are to be stored.
randrd_cnt = 0
Clear the random-read counter.
ICCR_0 = H'F9
Master transmit mode
Enable interrupts.
ICCR_0 = H'FC
Issue the start condition.
End

5.7.5 Function iici0_int

1. Overview
   Handler for I²C bus interface interrupts. According to the state of operations, this function calls the functions for receiving the stop condition, master transmission, master reception, and random reading.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78*1

Bit	Bit Name	Setting	R/W	Function
4	TRS	Undefined	R/W	Transmit/Receive Select 0: Receive mode 1: Transmit mode

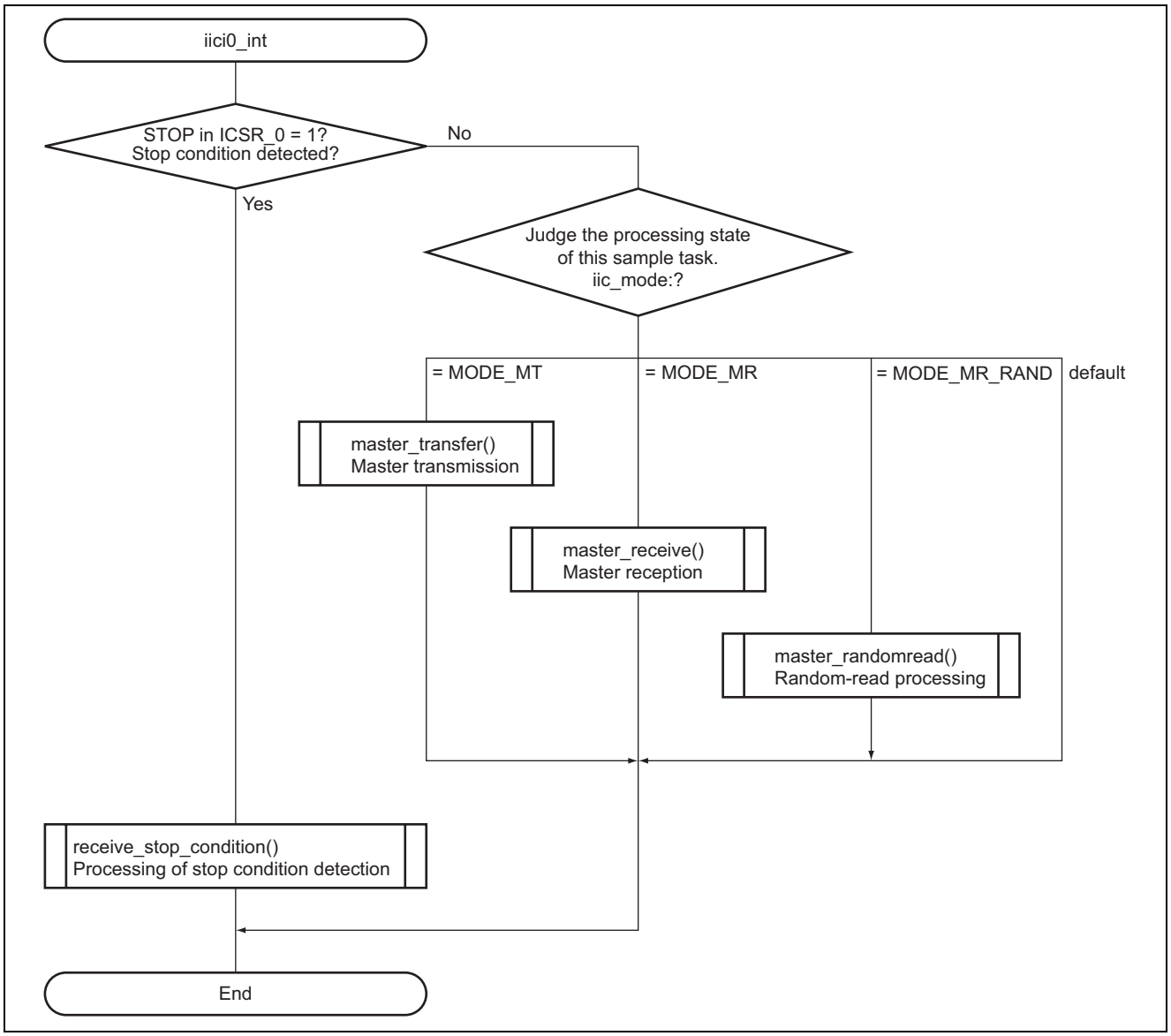
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79*1

Bit	Bit Name	Setting	R/W	Function
6	STOP	Undefined	R/(W)*2	Normal Stop Condition Detection Flag [Setting condition] • Detection of a stop condition after completion of frame transfer in slave mode [Clearing condition] • Writing a 0 to this bit after reading it as 1. • Clearing the IRIC flag to 0

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

5. Flow Chart


iici0_int
STOP in ICSR_0 = 1?
Stop condition detected?
No
Yes
Judge the processing state
of this sample task.
iic_mode:?
= MODE_MT
= MODE_MR
= MODE_MR_RAND
default
master_transfer()
Master transmission
master_receive()
Master reception
master_randomread()
Random-read processing
receive_stop_condition()
Processing of stop condition detection
End

5.7.6 Function receive_stop_condition

1. Overview
   This function handles processing on detection of the stop condition.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78*1

Bit	Bit Name	Setting	R/W	Function
1	IRIC	0	R/W	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1

Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

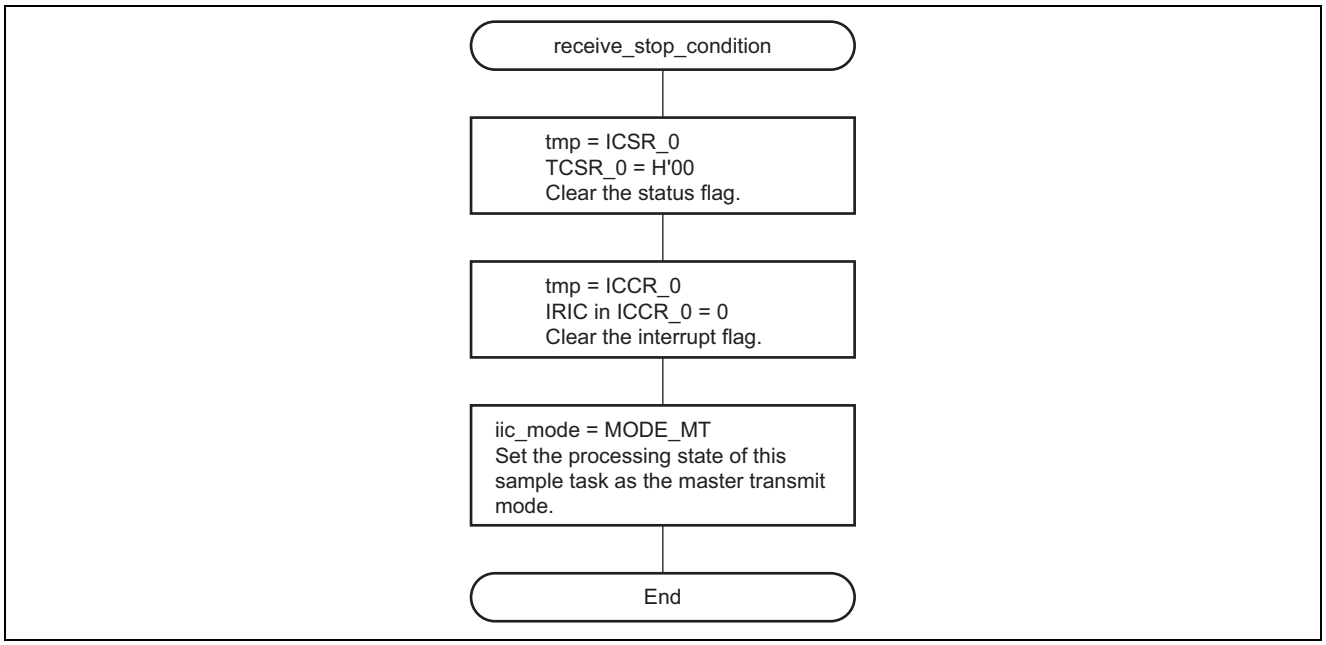
- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79*1

Bit	Bit Name	Setting	R/W	Function
7	ESTP	0	R/(W)*2	Error Stop Condition Detection Flag [Setting condition] Detected erroneous stop condition • Detection of a stop condition during frame transfer in slave mode [Clearing condition] No erroneous stop condition • Writing of 0 to this bit after reading it as 1 • Clearing of the IRIC flag to 0
6	STOP	1	R/(W)*2	Normal Stop Condition Detection Flag [Setting condition] • Detection of a stop condition by the I²C bus interface after it has finished transferring a frame in slave mode [Clearing condition] • Writing of 0 to this bit after reading it as 1 • Clearing of the IRIC flag to 0

Bit	Bit Name	Setting	R/W	Function
5	IRTR	0	R/(W)*2	I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag [Setting condition] In I²C bus interface slave mode • Setting of the TDRE or RDRF flag to 1 when AASX = 1 In other modes • Setting of the TDRE or RDRF flag to 1 [Clearing condition] • Writing of 0 to this bit after reading it as 1 • Clearing of the IRIC flag
3	AL	0	R/(W)*2	Arbitration Lost [Setting condition] Failure in bus contention (loss of arbitration) • Different values for the internal SDA signal and SDA pin on a rising edge of SCL in master transmit mode. • The internal SCL line being at the high level on a falling edge of SCL in master transmit mode [Clearing condition] • Writing of data to ICDR (transmit mode) or reading of data from ICDR (receive mode) • Writing of 0 to this bit after reading it as 1
2	AAS	0	R/(W)*2	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 when the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or when the general call address (H'00) is detected. [Setting condition] • In slave receive mode with FS = 0: detection of the slave address • In slave receive mode with FS = 0: detection of the general call address [Clearing condition] • Writing of data to ICDR (transmit mode) or reading of data from ICDR (receive mode) • Writing of 0 to this bit after reading it as 1 • Transition of the interface to master mode
0	ACKB	0	R/W	Acknowledge Bit In receive mode, sets the value of the bit to be sent at acknowledge timing here. 0: Outputs 0 at acknowledge timing. 1: Outputs 1 at acknowledge timing.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

5. Flow Chart


receive_stop_condition
tmp = ICSR_0
TCSR_0 = H'00
Clear the status flag.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
iic_mode = MODE_MT
Set the processing state of this sample task as the master transmit mode.
End

5.7.7 Function master_transfer

1. Overview
   Master-transmission process which is called from the I²C bus interface interrupt handler. In this case, the interrupt source will be the transmit-data empty interrupt for each byte of transmitted data. When arbitration is lost, it places the interface in slave receive mode.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78[*1]

Bit	Bit Name	Setting	R/W	Function
7	ICE	1	R/W	I²C Bus Interface Enable 0: Disables the IIC module and initializes its internal state. SAR and SARX can be accessed. 1: Enables transfer via the IIC module (pins SCL and SCA are driving the bus). ICMR and ICDR can be accessed.
6	IEIC	0	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	Transmit/Receive Select 11: Master transmit mode
3	ACKE	0	R/W	Acknowledge Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)[*2]	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	0	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. The stop condition is issued when BBSY = 0 and SCP = 0. 1: Reading always returns a value of 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79*1

Bit	Bit Name	Setting	R/W	Function
0	ACKB	Undefined	R/W	Acknowledge Bit In transmit mode, the value of the acknowledge data returned from the receiver device is loaded into the ACKB bit. 0: Indicates that the receiver device has acknowledged the data (signal is 0). 1: Indicates that the receiver device has not acknowledged the data (signal is 1).

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

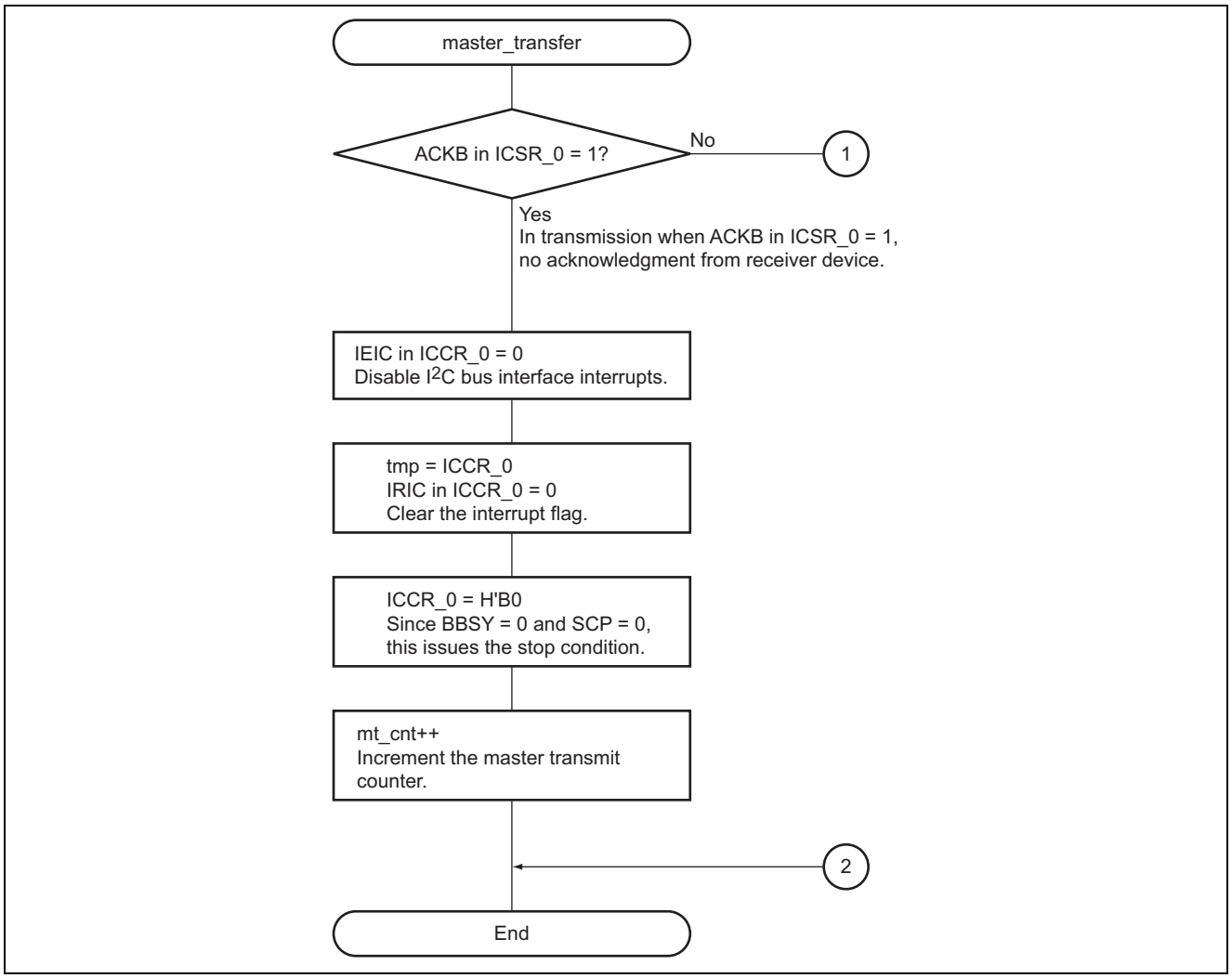
- I²C Bus Data Register_0 (ICDR_0) Address H'FFFF7E*1

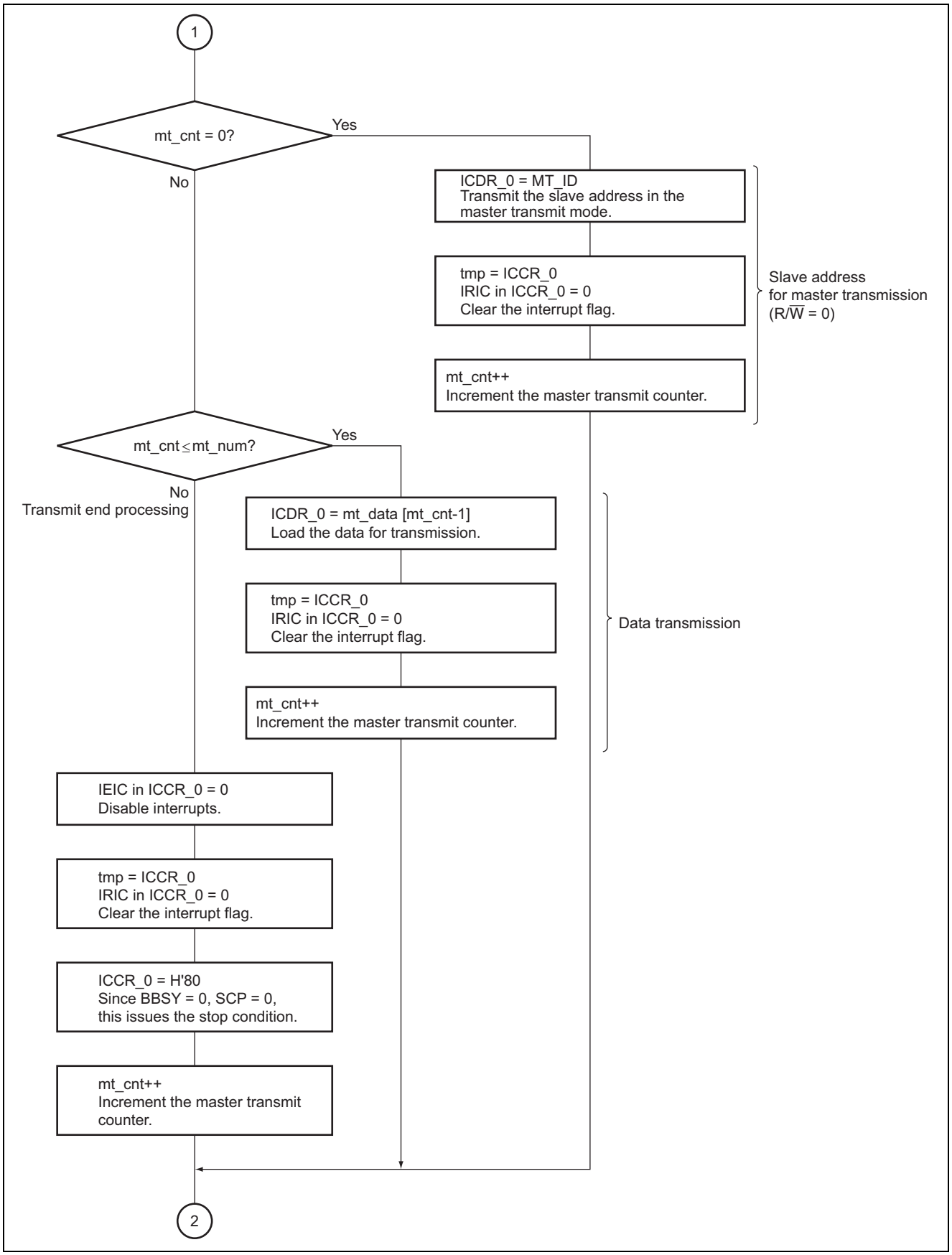
  Function: ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is internally divided into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU; ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the states of internal flags such as TDRE and RDRF.

  Setting: MT_ID, mt_data[mt_cnt-1]

Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

5. Flow Chart


master_transfer
ACKB in ICSR_0 = 1?
No
1
Yes
In transmission when ACKB in ICSR_0 = 1,
no acknowledgment from receiver device.
IEIC in ICCR_0 = 0
Disable I2C bus interface interrupts.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
ICCR_0 = H'B0
Since BBSY = 0 and SCP = 0,
this issues the stop condition.
mt_cnt++
Increment the master transmit
counter.
2
End


1
mt_cnt = 0?
Yes
No
ICDR_0 = MT_ID
Transmit the slave address in the master transmit mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mt_cnt++
Increment the master transmit counter.
Slave address for master transmission (R/W = 0)
mt_cnt≤mt_num?
Yes
No
Transmit end processing
ICDR_0 = mt_data [mt_cnt-1]
Load the data for transmission.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mt_cnt++
Increment the master transmit counter.
Data transmission
IEIC in ICCR_0 = 0
Disable interrupts.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
ICCR_0 = H'80
Since BBSY = 0, SCP = 0, this issues the stop condition.
mt_cnt++
Increment the master transmit counter.
2

5.7.8 Function master_receive

1. Overview
   Master-reception processing which is called by the I²C bus interface interrupt handler. In this case, the interrupt source will be the receive-data full interrupt for each byte of received data.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78*1

Bit	Bit Name	Setting	R/W	Function
6	IEIC	0	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	B'10	R/W	Master/Slave Select
4	TRS	& B'11	R/W	Transmit/Receive Select 10: Master receive mode 11: Master transmit mode
2	BBSY	0	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)*2	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	1	W	Start Condition/Stop Condition Prohibit 0: Writing 0 here issues a start or stop condition, according to the value of the BBSY flag. The stop condition is issued when BBSY = 0 and SCP = 0. 1: This bit is always read as 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79[*1]

Bit	Bit Name	Setting	R/W	Function
5	IRTR	0	R/(W)[*2]	I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag [Setting condition] In I²C bus interface slave mode • Setting of the TDRE or RDRF flag to 1 when AASX = 1 In other modes • Setting of the TDRE or RDRF flag to 1 [Clearing condition] • Writing of 0 to this bit after reading it as 1 • Clearing of the IRIC flag
3	AL	0	R/(W)[*2]	Arbitration Lost [Setting condition] Failure in bus contention (loss of arbitration) • Different values for the internal SDA signal and SDA pin on a rising edge of SCL in master transmit mode. • The internal SCL line being at the high level on a falling edge of SCL in master transmit mode [Clearing condition] • Writing of data to ICDR (transmit mode) or reading of data from ICDR (receive mode) • Writing of 0 to this bit after reading it as 1
0	ACKB	0	R/W	Acknowledge Bit In receive mode, sets the value of the bit to be sent at acknowledge timing here. 0: Outputs 0 at acknowledge timing. 1: Outputs 1 at acknowledge timing.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Data Register_0 (ICDR_0) Address: H'FFFF7E[*1]

Function: ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is internally divided into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU; ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the states of internal flags such as TDRE and RDRF.

Setting: MT_ID

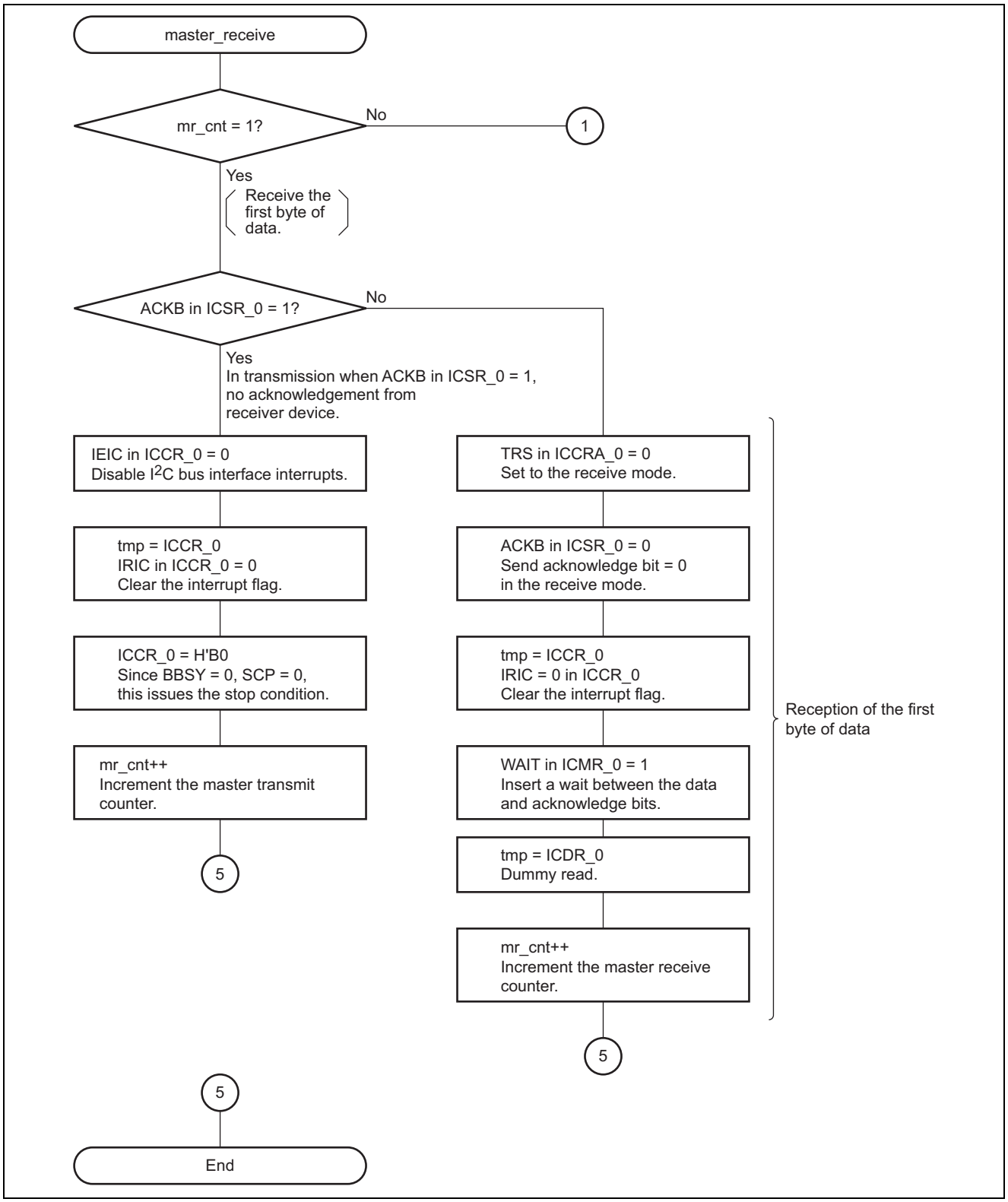
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

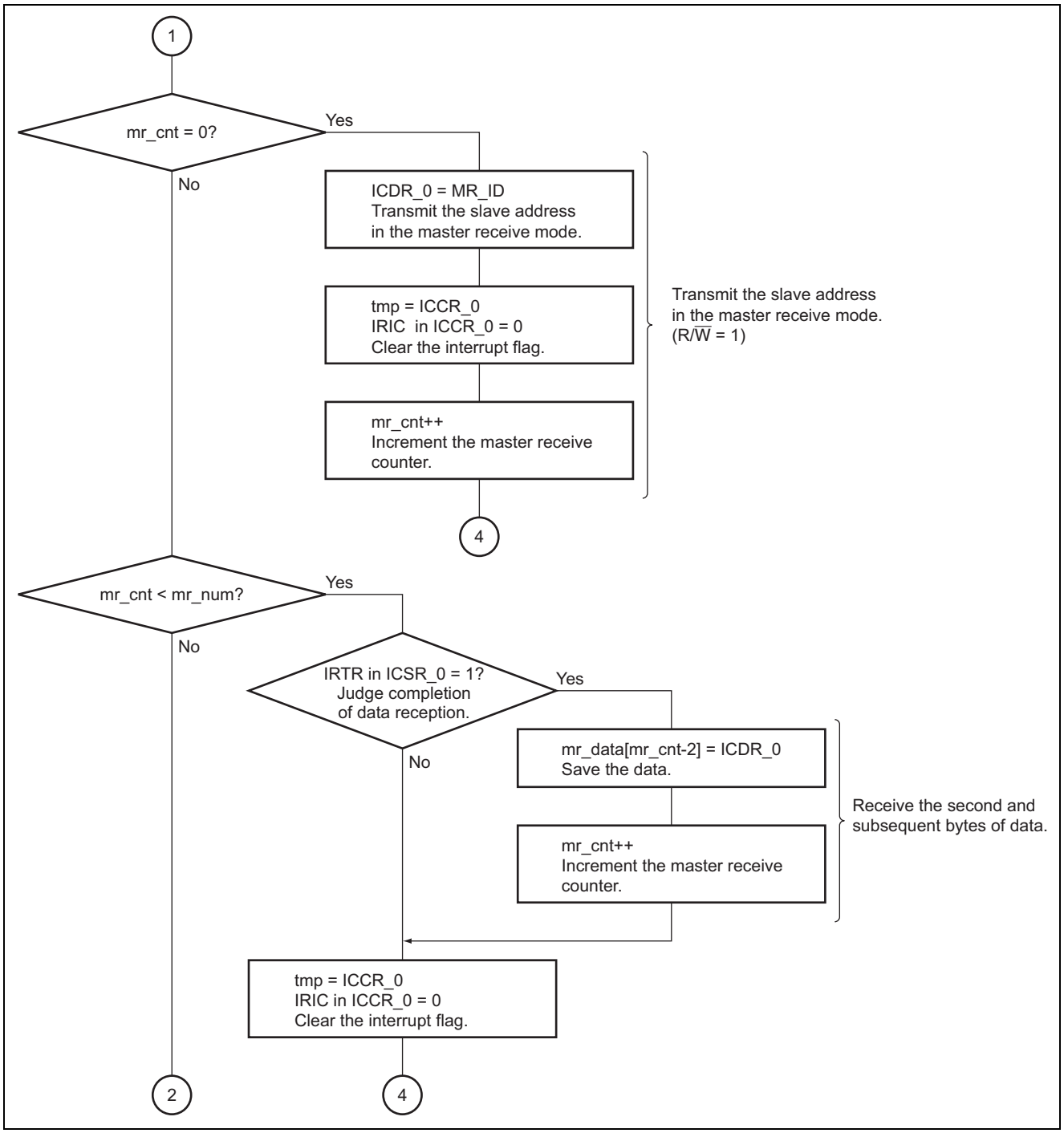
- I²C Bus Mode Register_0 (ICMR_0) Address: H'FFFF7F[*1]

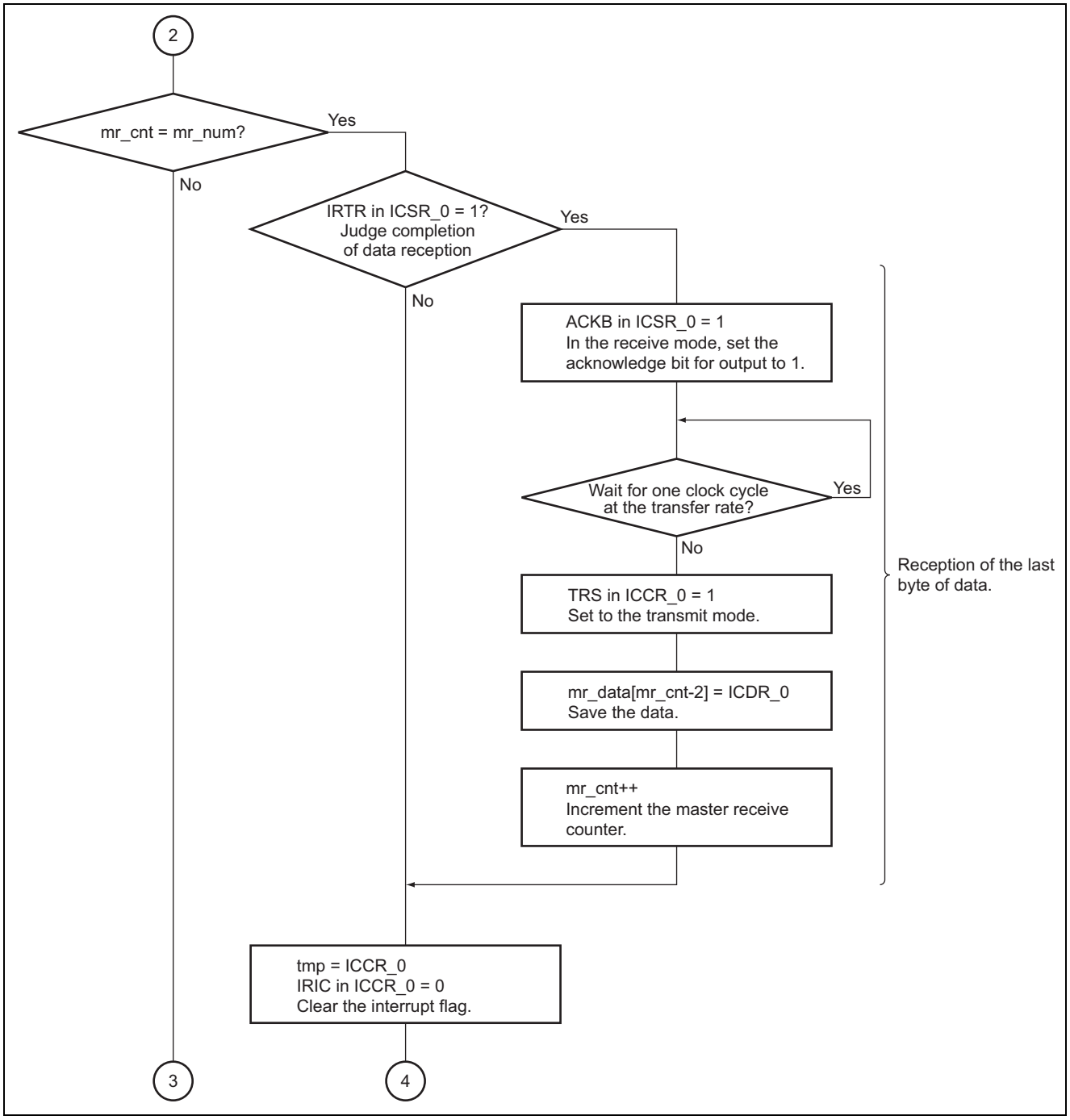
Bit	Bit Name	Setting	R/W	Function
6	WAIT	0/1	R/W	Wait Insertion Bit 0: Transfers data and acknowledge bits consecutively. 1: Inserts a wait between data and acknowledge bits.

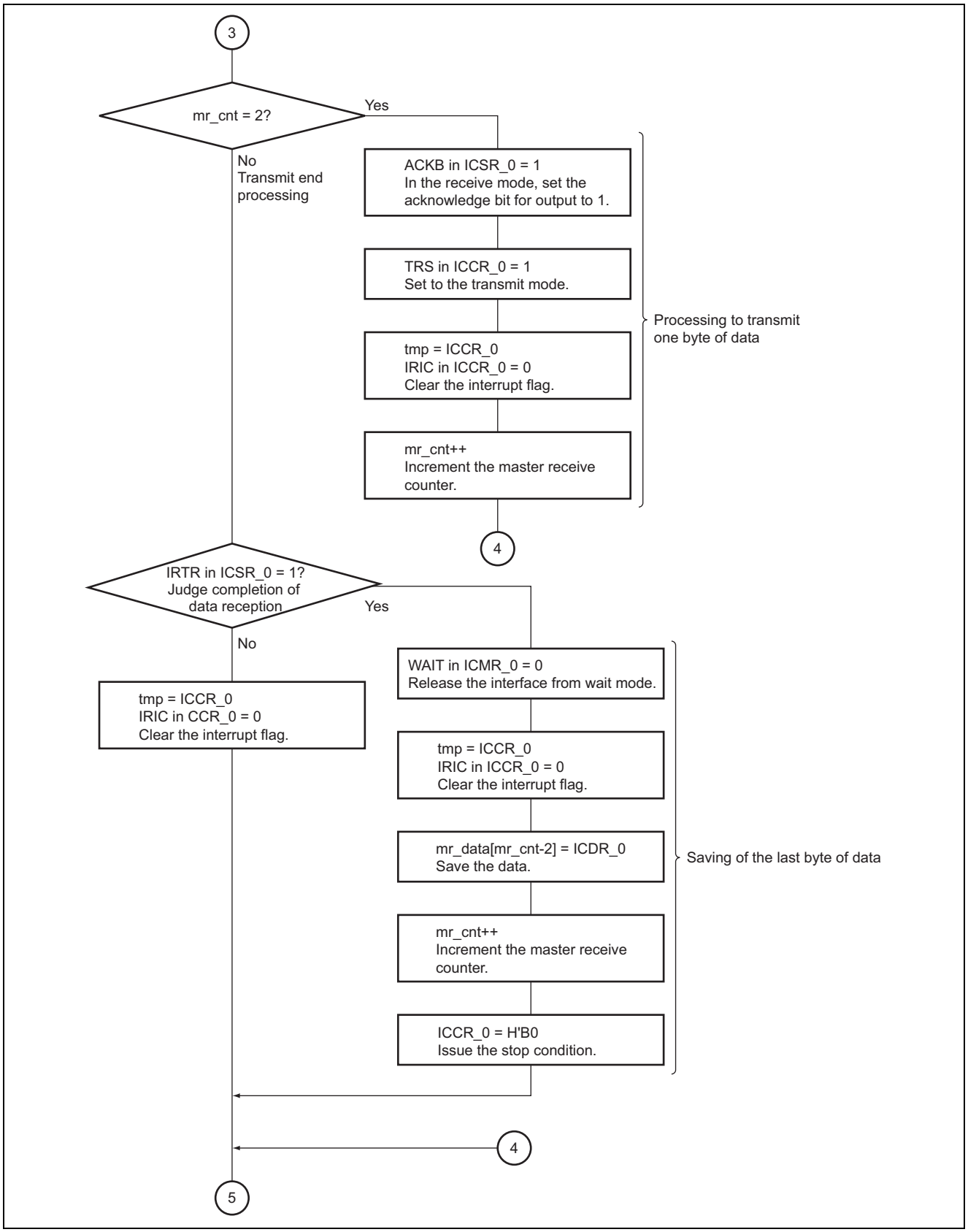
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

5. Flow Chart


master_receive
mr_cnt = 1?
No
1
Yes
Receive the first byte of data.
ACKB in ICSR_0 = 1?
No
Yes
In transmission when ACKB in ICSR_0 = 1, no acknowledgement from receiver device.
IEIC in ICCR_0 = 0
Disable I2C bus interface interrupts.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
ICCR_0 = H'B0
Since BBSY = 0, SCP = 0, this issues the stop condition.
mr_cnt++
Increment the master transmit counter.
5
TRS in ICCRA_0 = 0
Set to the receive mode.
ACKB in ICSR_0 = 0
Send acknowledge bit = 0 in the receive mode.
tmp = ICCR_0
IRIC = 0 in ICCR_0
Clear the interrupt flag.
WAIT in ICMR_0 = 1
Insert a wait between the data and acknowledge bits.
tmp = ICDR_0
Dummy read.
mr_cnt++
Increment the master receive counter.
5
Reception of the first byte of data
5
End


1
mr_cnt = 0?
Yes
No
ICDR_0 = MR_ID
Transmit the slave address
in the master receive mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mr_cnt++
Increment the master receive
counter.
Transmit the slave address
in the master receive mode.
(R/W = 1)
4
mr_cnt < mr_num?
Yes
No
IRTR in ICSR_0 = 1?
Judge completion
of data reception.
Yes
No
mr_data[mr_cnt-2] = ICDR_0
Save the data.
mr_cnt++
Increment the master receive
counter.
Receive the second and
subsequent bytes of data.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
2
4


2
mr_cnt = mr_num?
Yes
No
IRTR in ICSR_0 = 1?
Judge completion
of data reception
Yes
No
ACKB in ICSR_0 = 1
In the receive mode, set the
acknowledge bit for output to 1.
Wait for one clock cycle
at the transfer rate?
Yes
No
TRS in ICCR_0 = 1
Set to the transmit mode.
mr_data[mr_cnt-2] = ICDR_0
Save the data.
mr_cnt++
Increment the master receive
counter.
Reception of the last
byte of data.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
3
4


3
mr_cnt = 2?
Yes
No
Transmit end processing
ACKB in ICSR_0 = 1
In the receive mode, set the acknowledge bit for output to 1.
TRS in ICCR_0 = 1
Set to the transmit mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mr_cnt++
Increment the master receive counter.
Processing to transmit one byte of data
4
IRTR in ICSR_0 = 1?
Judge completion of data reception
Yes
No
WAIT in ICMR_0 = 0
Release the interface from wait mode.
tmp = ICCR_0
IRIC in CCR_0 = 0
Clear the interrupt flag.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mr_data[mr_cnt-2] = ICDR_0
Save the data.
mr_cnt++
Increment the master receive counter.
ICCR_0 = H'B0
Issue the stop condition.
Saving of the last byte of data
4
5

5.7.9 Function master_randomread

1. Overview
   Master-reception processing which is called by the I²C bus interface interrupt handler. In this case, the interrupt source will be the receive-data full interrupt for each byte of received data.
2. Arguments
   None
3. Return value
   None
4. Internal registers used
   The following describes internal registers used in this sample task. The settings are those used in this sample task rather than the initial settings.

- I²C Bus Control Register_0 (ICCR_0) Address: H'FFFF78[*1]

Bit	Bit Name	Setting	R/W	Function
6	IEIC	0/1	R/W	I²C Bus Interface Interrupt Enable 0: Disables interrupts. 1: Enables interrupts.
5	MST	B'10	R/W	Master/Slave Select
4	TRS	& B'11	R/W	Transmit/Receive Select 10: Master receive mode 11: Master transmit mode
3	ACKE	0/1	R/W	Acknowledgment Bit Judgment Select 0: Ignores the value of the acknowledge bit and transfers data continuously. 1: Interrupts continuous transfer when the acknowledge bit is 1.
2	BBSY	0/1	R/W	Bus Busy [Setting condition] • Detection of the start condition [Clearing condition] • Detection of the stop condition
1	IRIC	0	R/(W)[*2]	I²C Bus Interface Interrupt Request Flag [Setting condition] • Generation of an interrupt [Clearing condition] • Writing of 0 to this bit after reading it as 1
0	SCP	0/1	W	Start Condition/Stop Condition Prohibit 0: Writing a 0 here issues a start or stop condition, according to the value of the BBSY flag. The stop condition is issued when BBSY = 0 and SCP = 0. Start condition is issued at BBSY = 1, SCP = 0. 1: Reading always returns a value of 1 (the initial value). Writing of 1 has no effect.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Status Register_0 (ICSR_0) Address: H'FFFF79[*1]

Bit	Bit Name	Setting	R/W	Function
5	IRTR	Undefined	R/(W)[*2]	I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag [Setting condition] In I²C bus interface slave mode • Setting of the TDRE or RDRF flag to 1 when AASX = 1 In other modes • Setting of the TDRE or RDRF flag to 1 [Clearing condition] • Writing of 0 to this bit after reading it as 1 • Clearing of the IRIC flag
0	ACKB	0/1	R/W	Acknowledge Bit In receive mode, sets the value of the bit to be sent at acknowledge timing here. 0: Outputs 0 at acknowledge timing. 1: Outputs 1 at acknowledge timing.

Notes: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.
2. Only 0 can be written here, to clear the flag.

- I²C Bus Data Register_0 (ICDR_0) Address: H'FFFF7E[*1]

Function: ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is internally divided into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU; ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the states of internal flags such as TDRE and RDRF.

Setting: MT_ID, MR_ID, mt_data[0]

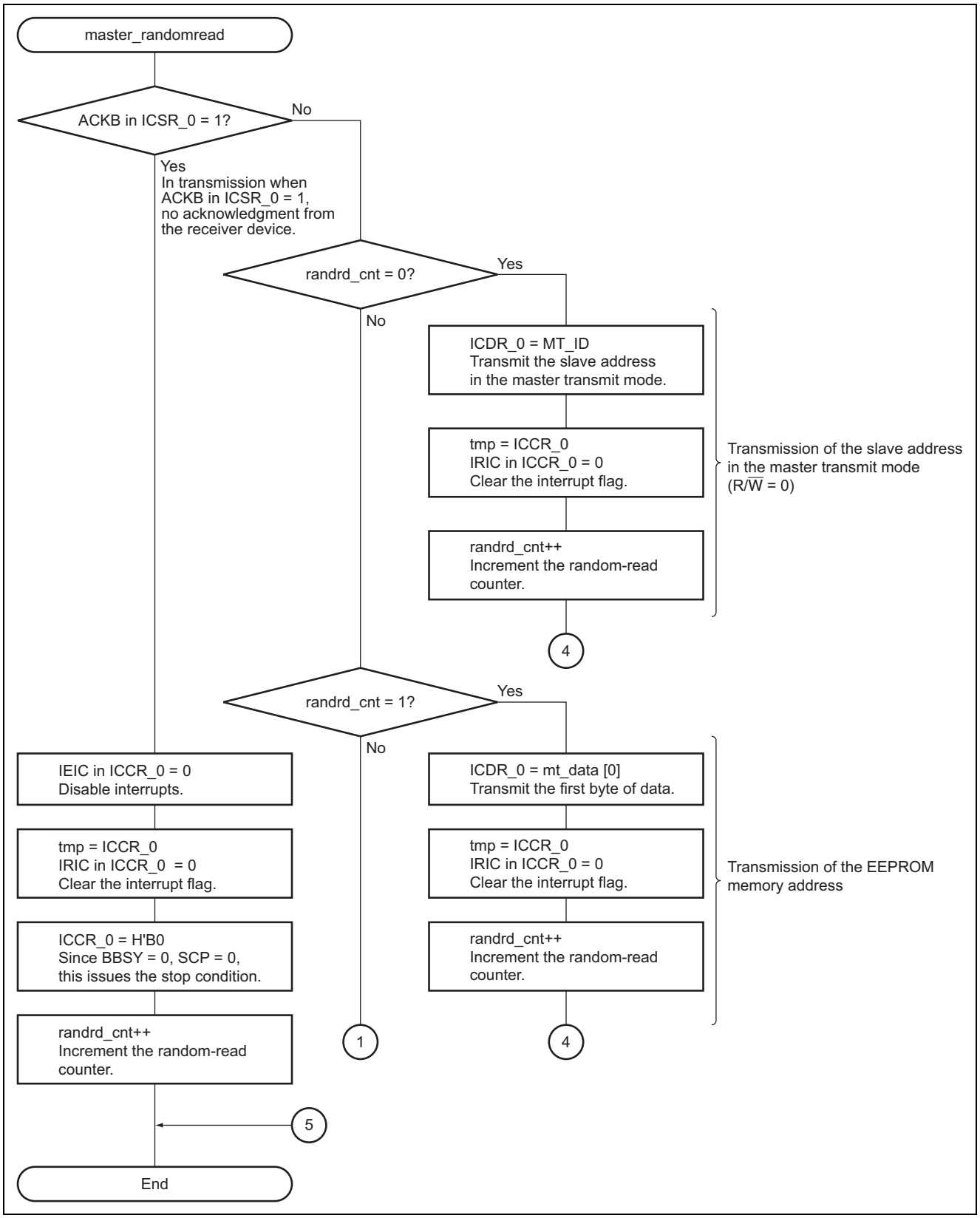
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

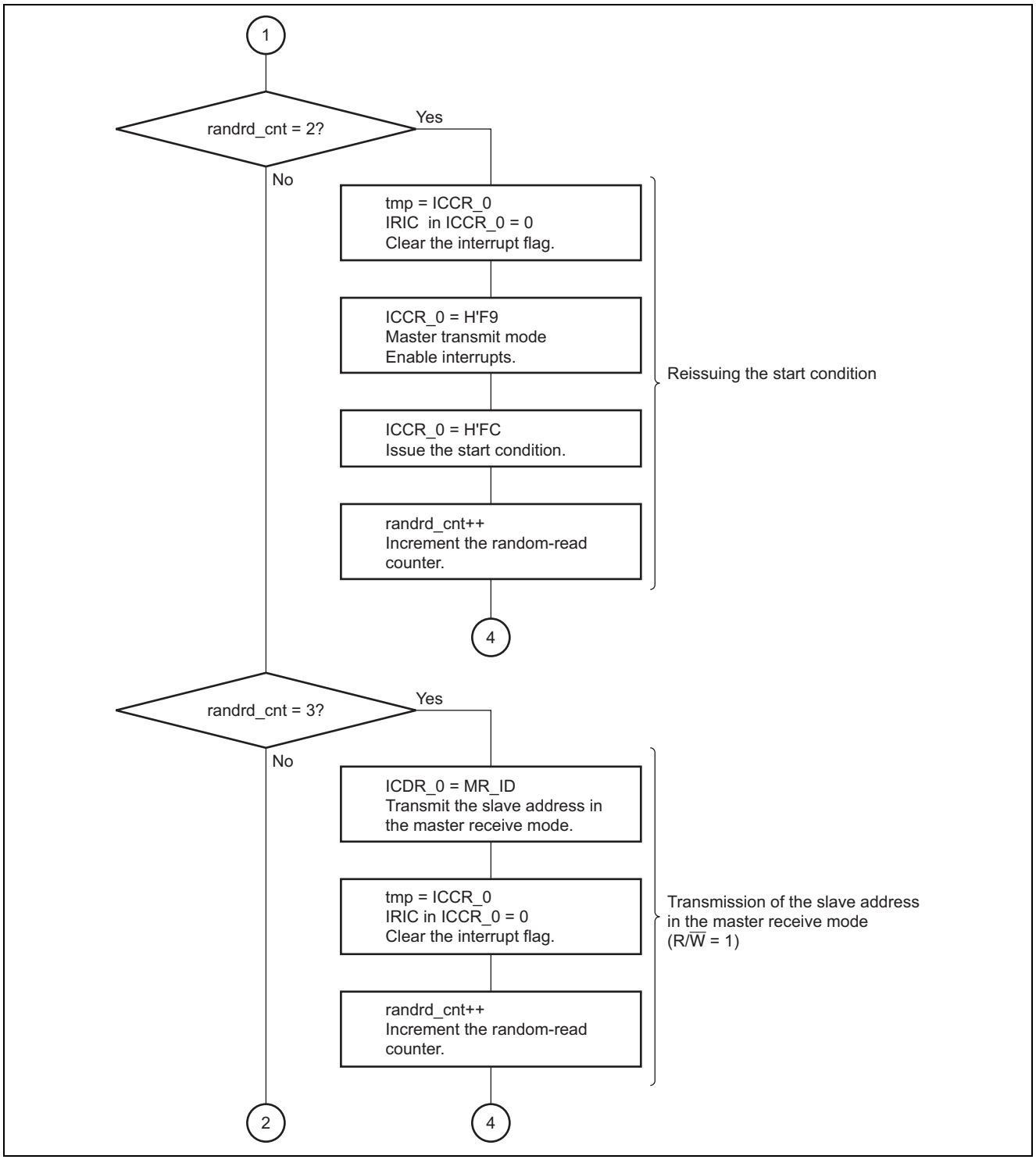
- I²C Bus Mode Register_0 (ICMR_0) Address: H'FFFF7F[*1]

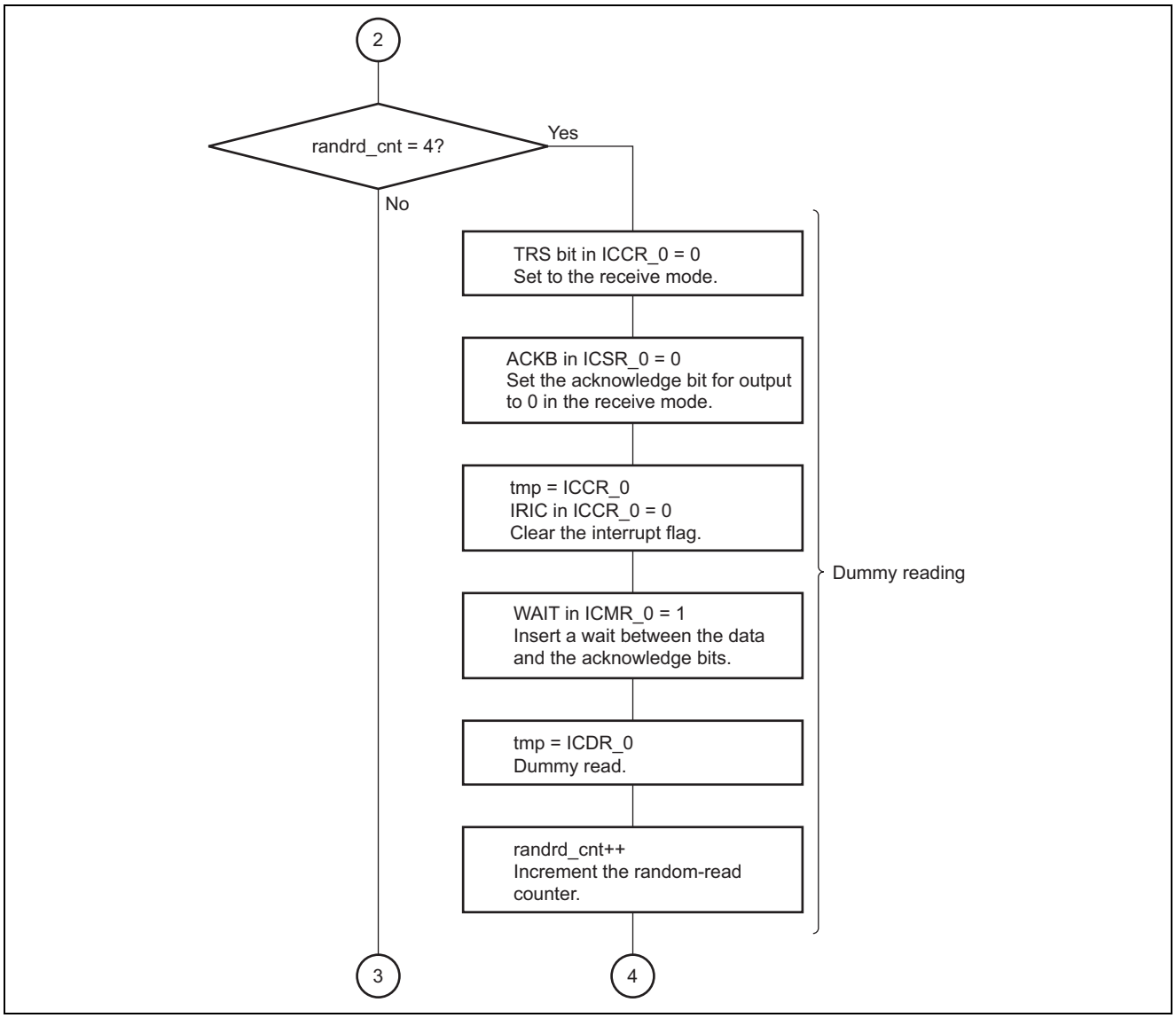
Bit	Bit Name	Setting	R/W	Function
6	WAIT	0/1	R/W	Wait Insertion Bit 0: Transfers data and acknowledge bits consecutively. 1: Inserts a wait between data and acknowledge bits.

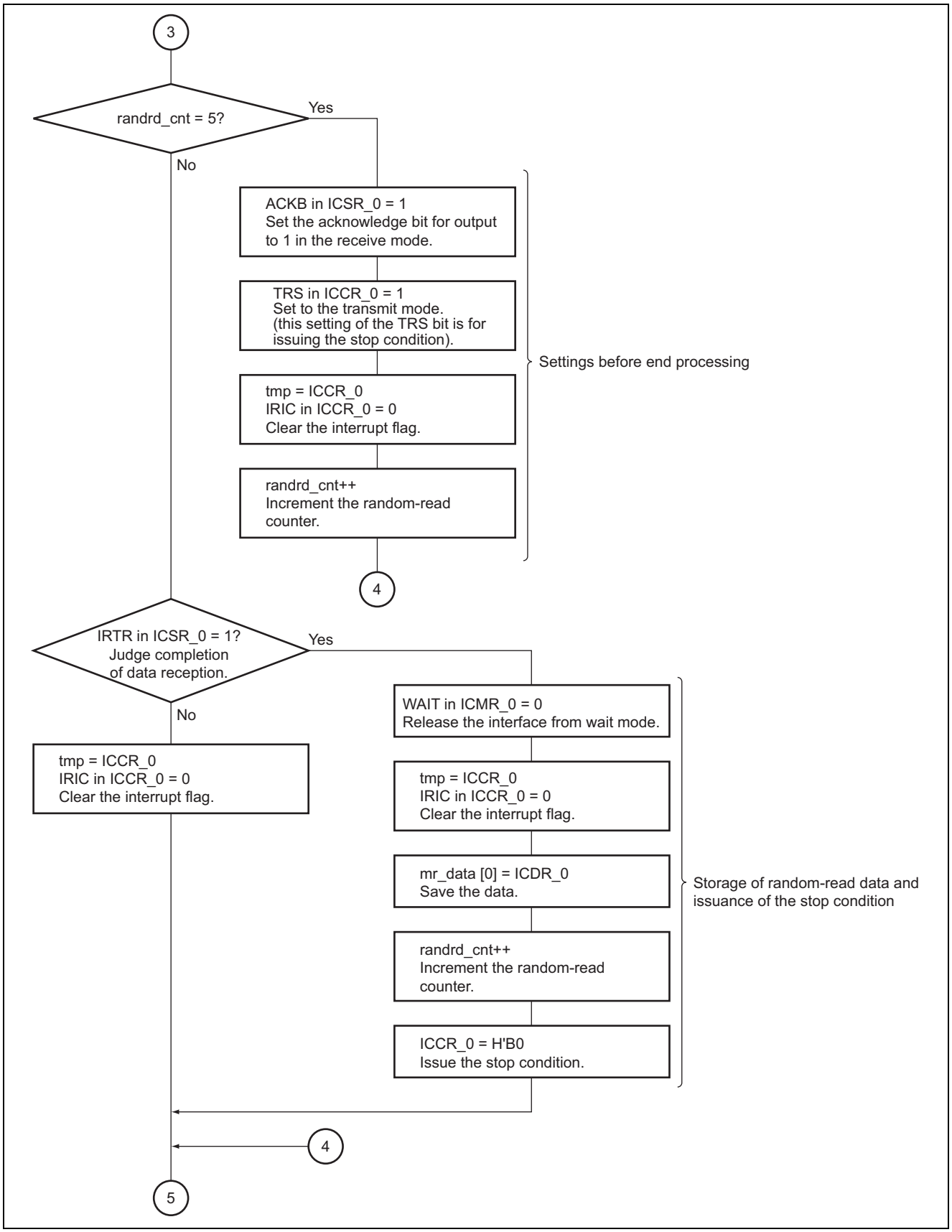
Note: 1. Only accessible when the ICE bit in ICCR_0 is set to 1.

5. Flow Chart


master_randomread
ACKB in ICSR_0 = 1?
No
Yes
In transmission when ACKB in ICSR_0 = 1, no acknowledgment from the receiver device.
randrd_cnt = 0?
Yes
No
ICDR_0 = MT_ID
Transmit the slave address in the master transmit mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
randrd_cnt++
Increment the random-read counter.
Transmission of the slave address in the master transmit mode (R/W = 0)
4
randrd_cnt = 1?
Yes
No
IEIC in ICCR_0 = 0
Disable interrupts.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
ICCR_0 = H'B0
Since BBSY = 0, SCP = 0, this issues the stop condition.
randrd_cnt++
Increment the random-read counter.
1
ICDR_0 = mt_data [0]
Transmit the first byte of data.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
randrd_cnt++
Increment the random-read counter.
4
Transmission of the EEPROM memory address
5
End


1
randrd_cnt = 2?
Yes
No
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
ICCR_0 = H'F9
Master transmit mode
Enable interrupts.
ICCR_0 = H'FC
Issue the start condition.
randrd_cnt++
Increment the random-read counter.
Reissuing the start condition
4
randrd_cnt = 3?
Yes
No
ICDR_0 = MR_ID
Transmit the slave address in the master receive mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
randrd_cnt++
Increment the random-read counter.
Transmission of the slave address in the master receive mode (R/W = 1)
2
4


2
randrd_cnt = 4?
Yes
No
TRS bit in ICCR_0 = 0
Set to the receive mode.
ACKB in ICSR_0 = 0
Set the acknowledge bit for output to 0 in the receive mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
WAIT in ICMR_0 = 1
Insert a wait between the data and the acknowledge bits.
tmp = ICDR_0
Dummy read.
randrd_cnt++
Increment the random-read counter.
Dummy reading
3
4


3
randrd_cnt = 5?
Yes
No
ACKB in ICSR_0 = 1
Set the acknowledge bit for output to 1 in the receive mode.
TRS in ICCR_0 = 1
Set to the transmit mode.
(this setting of the TRS bit is for issuing the stop condition).
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
randrd_cnt++
Increment the random-read counter.
Settings before end processing
4
IRTR in ICSR_0 = 1?
Judge completion of data reception.
Yes
No
WAIT in ICMR_0 = 0
Release the interface from wait mode.
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
mr_data [0] = ICDR_0
Save the data.
randrd_cnt++
Increment the random-read counter.
ICCR_0 = H'B0
Issue the stop condition.
Storage of random-read data and issuance of the stop condition
tmp = ICCR_0
IRIC in ICCR_0 = 0
Clear the interrupt flag.
4
5

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jan.31.07	—	First edition issued

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