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H8/300L SLP Series

Simultaneously Measuring Four Voltages by Multi-channel A/D Conversion

Introduction

Input voltages on four channels are measured using the built in A/D converter and the results are stored in RAM.

Target Device

H8/38024

Contents

1. Specifications

1. Voltages input from four channels are simultaneously measured by using the built-in A/D converter.
2. As shown in figure 1.1, voltage signals are input to the H8/38024 through four channels and their A/D-converted results are stored in RAM.

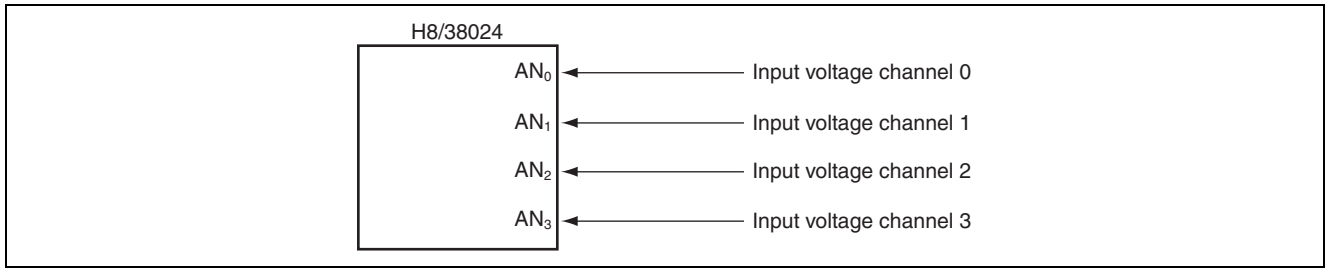


Figure 1.1 Voltage Measurement by 4-Channel A/D Conversion

2. Description of Functions

1. In this sample task, voltages are measured by 4-channel A/D conversion using the built-in A/D converter.
   A. Figure 2.1 shows the block diagram of the A/D converter described below.
      - The A/D Result Register (ADRRH, ADRRL) is a 16-bit read-only register and stores the results of A/D conversion. The upper 8-bits of the converted 10-bit data are stored in ADRRH, and the lower 2 bits are stored in bits 7 and 6 of ADRRL.
      - The A/D Mode Register (AMR) is an 8-bit readable/writable register that sets an A/D conversion speed and designates analog input pins. The A/D conversion speed is set to 12.4 µs in this sample task.
      - The A/D Start Register (ADSR) is an 8-bit readable/writable register that is used to start and stop A/D conversion.
      - Analog Input Pins 0 to 7 (AN_0 to AN_7) are input pins for Input Voltage Channels 0 to 7.
      - In this sample task, the voltages on analog input pins 0 to 3 (AN_0 to AN_3) are measured by 4-channel A/D conversion.
      - Analog Power Supply (AVcc) is the power supply and reference voltage pin of the analog signal processing section.
      - Analog Ground (AVss) is the grounding and reference voltage pin of the analog signal processing section.

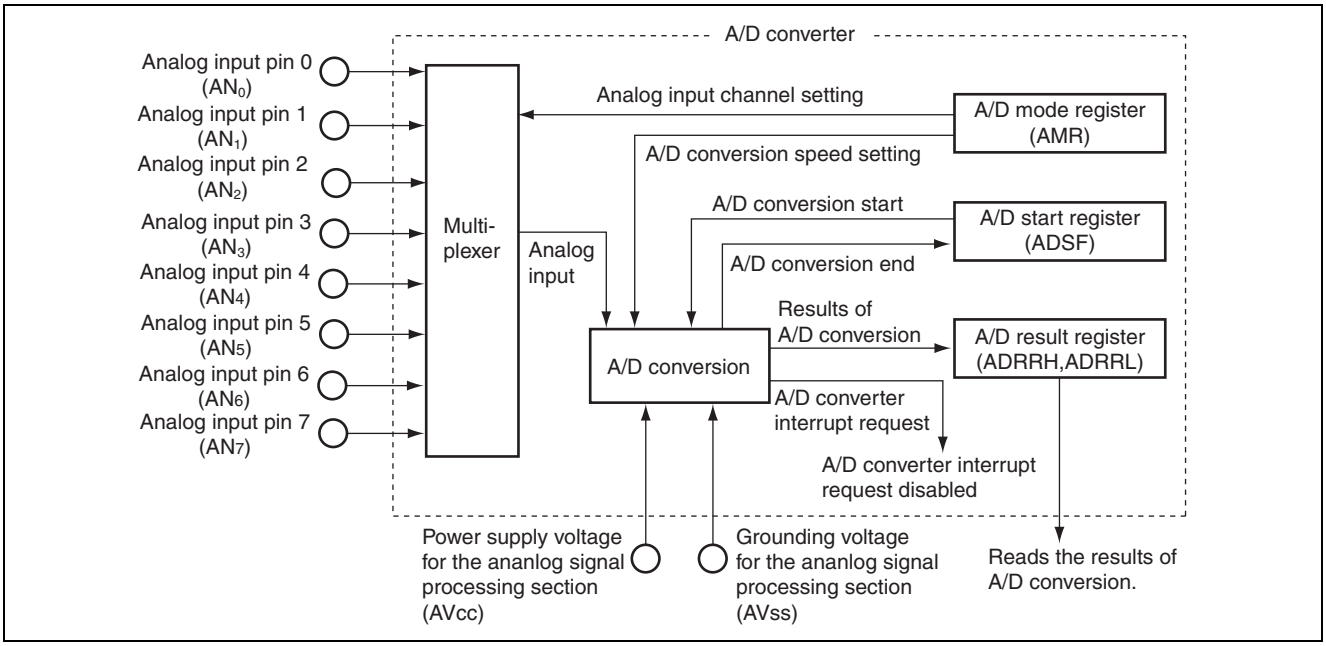


Figure 2.1 Block Diagram of the A/D Converter

2. Table 2.1 shows function allocation in this sample task. The functions are allocated as shown in table 2.1 to measure voltages by 4-channel A/D conversion.

Table 2.1 Function Allocation

Function	Function Allocation
AMR	Sets A/D conversion speed and designates analog input pins.
ADSF	Starts and stops the A/D conversion.
ADRRH, ADRRL	Stores the A/D-converted results.
AN_0 to AN_7	Input pins for input voltage channels 0 to 7 (in this sample task, AN_0 to AN_3 are used)
AVcc	Power supply and reference voltage pin of the analog signal processing section
AVss	Ground and reference voltage pin of the analog signal processing section

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. Voltage measurement by 4-channel A/D conversion is implemented through the hardware processing and software processing shown in the figure.

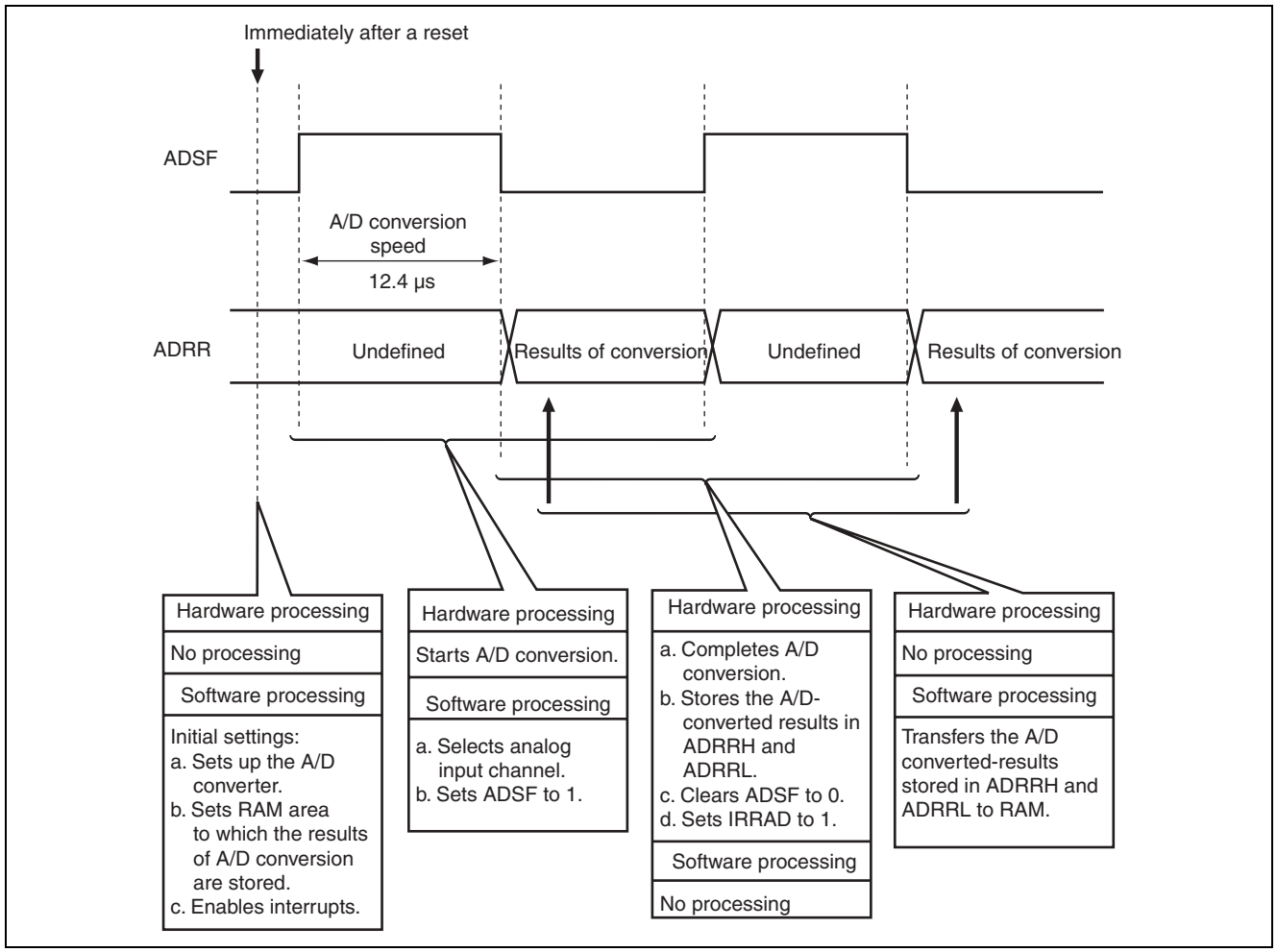


Figure 3.1 Operation Principle of Voltage Measurement by 4-Channel A/D Conversion

4. Description of Software

4.1 Modules

Table 4.1 describes the module in this sample task.

Table 4.1 Description of Module

Module	Label	Function
Main Routine	main	Sets up the A/D converter, enables interrupts, selects analog input channels, starts A/D conversion, transfers the A/D-converted results stored in ADRRH and ADRRL to RAM after A/D conversion is finished, and ends when A/D conversion on analog input channels 0 to 3 is finished.

4.2 Arguments

The arguments used in this sample task are described in Table 4.2.

Table 4.2 Description of Arguments

Argument	Function	Used in	Data Length	Input/ Output
addata[0]	Stores A/D conversion results of Analog Input Channel 0.	Main Routine	2 byte	Output
addata[1]	Stores A/D conversion results of Analog Input Channel 1.	Main Routine	2 byte	Output
addata[2]	Stores A/D conversion results of Analog Input Channel 2.	Main Routine	2 byte	Output
addata[3]	Stores A/D conversion results of Analog Input Channel 3.	Main Routine	2 byte	Output

4.3 Internal registers

Table 4.3 describes the internal registers involved in this sample task.

Table 4.3 Description of Internal Registers

Register		Function	Address	Setting
AMR	CKS	A/D Mode Register (Clock Select) If CKS = 0, A/D conversion speed is set to 12.4 µs.	H'FFC6 Bit 7	0
	CH3 CH2 CH1 CH0	A/D Mode Register (Channel Select 3 to 0) AN_0 is selected if CH3 = 0, CH2 = 1, CH1 = 0 and CH0 = 0. AN_1 is selected if CH3 = 0, CH2 = 1, CH1 = 0 and CH0 = 1. AN_2 is selected if CH3 = 0, CH2 = 1, CH1 = 1 and CH0 = 0. AN_3 is selected if CH3 = 0, CH2 = 1, CH1 = 1 and CH0 = 1.	H'FFC6 Bit 3 Bit 2 Bit 1 Bit 0	CH3 = 0 CH2 = 1 CH1 = 0 CH0 = 0
ADSR	ADSF	A/D Start Register (A/D Start Flag) If ADSF = 0, A/D conversion is complete. If ADSF = 1, A/D conversion is started.	H'FFC7 Bit 7	0
ADRRH		A/D Result Register H Stores the upper 8 bits of the results of A/D conversion.	H'FFC4	Undefined
ADRRL		A/D Result Register L Stores the lower 2 bits of the results of A/D conversion.	H'FFC5	Undefined
PMRB	IRQ1	Port Mode Register B (PB3/AN3/IRQ1 pin switch) If IRQ1 = 0, PB3/AN3/IRQ1 pin functions as PB3/AN3 input pin If IRQ1 = 1, PB3/AN3/IRQ1 pin functions as IRQ1/TMIC input pin	H'FFEE Bit 3	0

4.4 Description of RAM

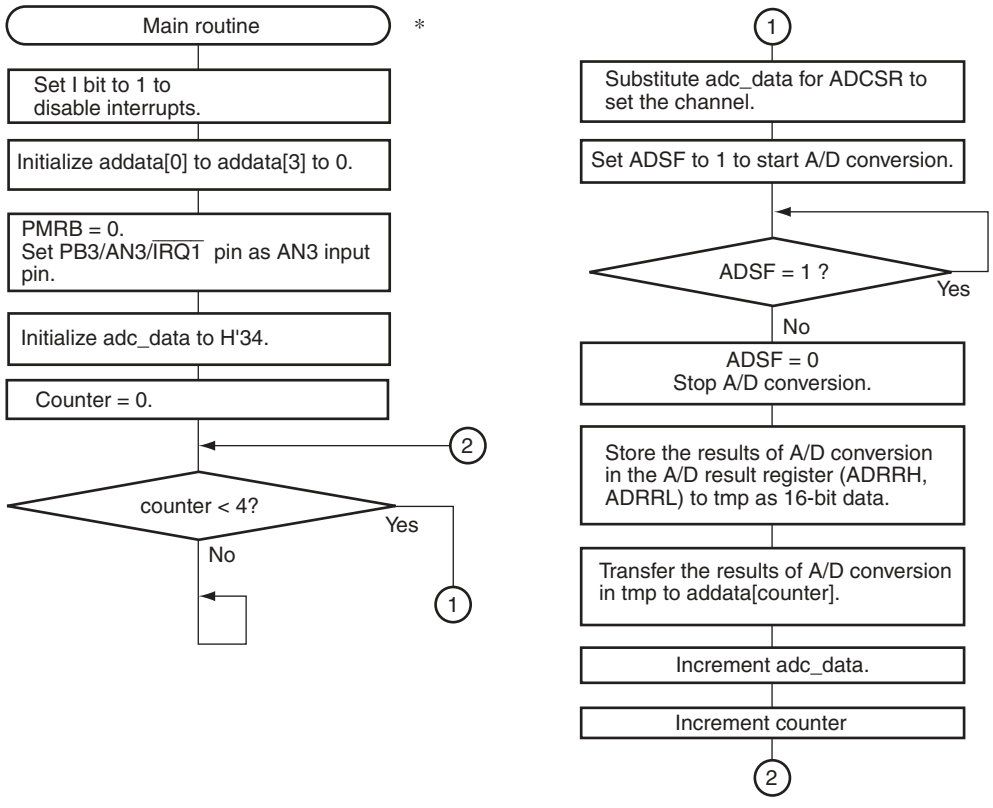
Table 4.4 describes the RAM area used in this sample task.

Table 4.4 Description of RAM

Label	Function	Address	Used in
addata[0]	A data variable for RAM storage	H'FB80	Main Routine
addata[1]	A data variable for RAM storage	H'FB82	Main Routine
addata[2]	A data variable for RAM storage	H'FB84	Main Routine
addata[3]	A data variable for RAM storage	H'FB86	Main Routine
Counter	Counts the number of A/D conversions repeated in 4-channel A/D conversion.	H'FB88	Main Routine

5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Voltage Measurement by 4-Channel A/D                                                                               */
/*   Converter'                                                                                                         */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : A/D Converter                                                                                                     */
/*                                                                                                                      */
/*  External Clock : 16MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7: 1;       /* bit7 */
    unsigned char   b6: 1;       /* bit6 */
    unsigned char   b5: 1;       /* bit5 */
    unsigned char   b4: 1;       /* bit4 */
    unsigned char   b3: 1;       /* bit3 */
    unsigned char   b2: 1;       /* bit2 */
    unsigned char   b1: 1;       /* bit1 */
    unsigned char   b0: 1;       /* bit0 */
};

#define     ADRRH       *(volatile unsigned char *)0xFFC4        /* Timer Mode Register A                */
#define     ADRRL       *(volatile unsigned char *)0xFFC5        /* Timer Counter A                      */
#define     AMR         *(volatile unsigned char *)0xFFC6        /* A/D Control/Status Register          */
#define     AMR_BIT     (*(struct BIT *)0xFFC6)                  /* A/D Control/Status Register          */
#define     CKS         ADCSR_BIT.b7                             /* A/D Clock Select                     */
```

```
#define     CH3         ADCSR_BIT.b3                        /* Channel Select 2                         */
#define     CH2         ADCSR_BIT.b2                        /* Channel Select 2                         */
#define     CH1         ADCSR_BIT.b1                        /* Channel Select 1                         */
#define     CH0         ADCSR_BIT.b0                        /* Channel Select 0                         */
#define     ADSR        *(volatile unsigned int *)0xFFC7    /* A/D Data Register A                      */
#define     ADSR_BIT    (*(struct BIT *)0xFFC7)             /* A/D Data Register A                      */
#define     ADSF        ADSR_BIT.b7                         /* A/D Clock Select                         */
#define     PMRB        *(volatile unsigned char *)0xFFEE   /* Port Mode Register B                     */

/************************************************************************************************************************/
/*  Function define                                                                                                     */
/************************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );

/************************************************************************************************************************/
/*  RAM define                                                                                                          */
/************************************************************************************************************************/
unsigned int    addata[4];
unsigned char   counter;

/************************************************************************************************************************/
/*  Vector Address                                                                                                      */
/************************************************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {                          /* 0x0000 - 0x000F                          */
    INIT                                                    /* 0x0000 Reset Vector                      */
};

#pragma section                                             /* P                                        */
/************************************************************************************************************************/
/*  Main Program                                                                                                        */
/************************************************************************************************************************/
void    main ( void )
{
    unsigned char   adc_data;
    unsigned int    tmp;

    set_imask_ccr(1);                                       /* Interrupt Disable                        */

    addata[0] = 0;                                          /* Clear addata[0]                          */
    addata[1] = 0;                                          /* Clear addata[1]                          */
    addata[2] = 0;                                          /* Clear addata[2]                          */
    addata[3] = 0;                                          /* Clear addata[3]                          */

    PMRB = 0;                                               /* PB3/AN3 input select                     */

    adc_data = 0x34;                                        /* Clear adc_data                           */

    for(counter = 0; counter < 4; counter++){               /* A/D Convert END ?                        */
        AMR = adc_data;                                     /* Select A/D Convert Time &                */
                                                            /*                      Analog Input Channel */

        ADSF = 1;                                           /* Start A/D Convert                        */
```

```
        while(ADSF == 1){                                   /* A/D Convert End ?                */
            ;
        }

        ADSF = 0;                                           /* Stop A/D Convert                 */

        tmp  = (ADRRH << 2) | (ADRRL >> 6);

        addata[counter] = tmp;                              /* Store A/D Result Data            */

        adc_data++;                                         /* Increment AMR Set Data           */
    }

    while(1){
        ;
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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