SH7670 Group

Hi-Speed USB 2.0 Board Design Guidelines

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Introduction

This application note presents guidelines for designing boards that include hi-speed USB 2.0 functionality.

Target Devices

The application examples described in this document can be used with the following devices.

SH7670, SH7671, SH7672, and SH7673

These devices are referred to as the SH767x in this document.

Note: The content presented in this application note consists of examples for reference purposes based on the USB standard. This application note makes no guarantees concerning signal quality. When including these circuits and programs in an actual system, the complete system must be tested and evaluated thoroughly. The customer must take responsibility for determining the applicability of the contents of this application note.

Contents

1. Introduction

This document uses the USB 2.0 host/function module pin names in its descriptions. Table 1 presents an overview of the USB 2.0 host/function module pin names.

Table 1 USB 2.0 Host/Function Module Pin Names

Pin No. SH767x	Pin Name	I/O	Function	Description
Y9	DP	I/O	USB D+ data	USB bus D+ data.
Y8	DM	I/O	USB D- data	USB bus D- data.
W9	VBUS	Input	VBUS input	Connect to the USB bus VBUS signal.
Y11	REFRIN	Input	Reference input	Connect to the AG33 pin through a 5.6 kΩ ±1% resistor.
W12	USB_X1	Input	USB crystal oscillator/ external clock	Connect the USB crystal oscillator element. Alternatively, an external clock may be input to the USB_X1 pin.
Y12	USB_X2	Output		
Y10	AV33	Input	Transceiver block analog pin power supply	Pin 3.3 V analog system power supply
W10	AG33	Input	Transceiver block analog pin ground	Pin 3.3 V analog system ground
Y7	DV33	Input	Transceiver block digital pin power supply	Pin 3.3 V digital system power supply
W8	DG33	Input	Transceiver block digital pin ground	Pin 3.3 V digital system ground
U11	AV12	Input	Transceiver block analog core power supply	Core 1.2 V analog system power supply
V11	AG12	Input	Transceiver block analog core ground	Core 1.2 V analog system ground
U9	DV12	Input	Transceiver block digital core power supply	Core 1.2 V digital system power supply
U8	DG12	Input	Transceiver block digital core ground	Core 1.2 V digital system ground
U10	UV12	Input	USB 2.0 host/function module 480 MHz system power supply	480 MHz system power supply
V10	UG12	Input	USB 2.0 host/function module 480 MHz system ground	480 MHz system ground
*	VccQ	Input	I/O circuit power supply	I/O pin 3.3 V power supply
	VssQ	Input	I/O circuit ground	I/O pin 3.3 V ground
	Vcc	Input	Power supply	Core internal 1.2 V power supply
	Vss	Input	Ground	Core internal 1.2 V ground

Note: * The VccQ, VssQ, Vcc, and Vss power supply pins are for I/O and core power supplies for ICs other than the USB IC.

2. USB Transmission Path

The term USB transmission path here refers to the wiring pattern that connects the USB connector to the USB transceiver.

The USB 2.0 standard includes the Hi-Speed, Full-Speed, and Low-Speed modes. Since of these, the Hi-Speed mode has a 480 Mbps communications rate, the USB transmission path must be designed as a high-frequency circuit. Impedance control is required for the USB transmission path.

This section presents important notes on wiring pattern design for the USB transmission path.

- The characteristic impedance required for the USB Hi-Speed transmission path is a differential impedance of 90 Ω ±15%.
- The pattern width and pattern spacing will differ with the board thickness, materials, and layer structure for impedance control. Consult with the circuit board manufacturer for details.
- The length of the wiring pattern from the IC to the USB connector must be designed so that the maximum delay time stipulated in the USB standard is not exceeded. We recommend using shorter wiring lengths in consideration of the waveform quality for Hi-Speed USB. Table 2 lists the pattern design values for the USB transmission path in printed circuit boards made from typical materials considering the maximum delay times.

Table 2 USB Transmission Path Wiring Pattern Design Values for Maximum Delay Times

	Maximum Delay Time (USB Standard)	Wiring Length*	D+/D- Wiring Length Difference
Host controller	3 ns	No longer than 300 mm	No longer than 2.5 mm
Function controller	1 ns	No longer than 100 mm	No longer than 2.5 mm

Note: * When the wiring delay is 100 ps/cm.

- The layer below the USB transmission path should be a solid ground plane. This solid ground plane must extend at least 2 mm beyond the USB transmission path. The power supply for the solid ground plane will be DG33.
- Do not run any other signals in the vicinity of the USB transmission path. In particular, keep clock, data, and any other paths that have rapid signal variations as far away from the USB transmission path as possible. Also, do not allow the USB transmission path to cross any other signals.
- We recommend using a ground guard ring separated by at least 2 mm from the outside of the transmission path in the same layer (top layer) as the USB transmission path.
- The USB transmission path should be formed on the same layer without via connections. Also, do not split the USB transmission path.
- The USB transmission path separation should be the same for the whole path.
- The USB transmission path must be isolated from oscillators, power supply circuits, and other I/O connectors.
- The USB transmission path should be as straight a path as possible. If the USB transmission path must bend in the layout, use a gentle bend of 135 degrees or an arc. Do not any sharp (right angle) bends in the USB transmission path.
- We recommend providing a ground guard ring around the clock, reset, read, write, and chip select signals.

Figure 1 shows an example of a USB transmission path wiring pattern design for a host controller, and figure 2 shows an example of a USB transmission path wiring pattern design for a function controller.

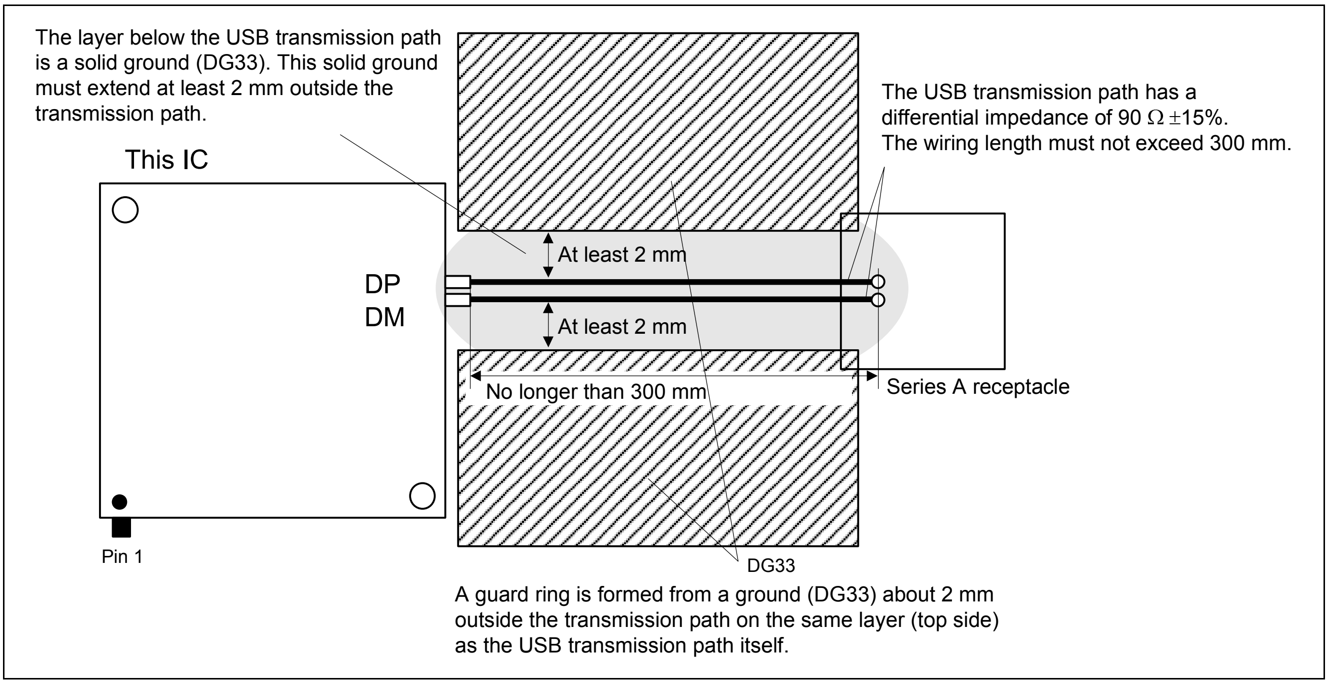


Figure 1 Host Controller USB Transmission Path Pattern Design Example

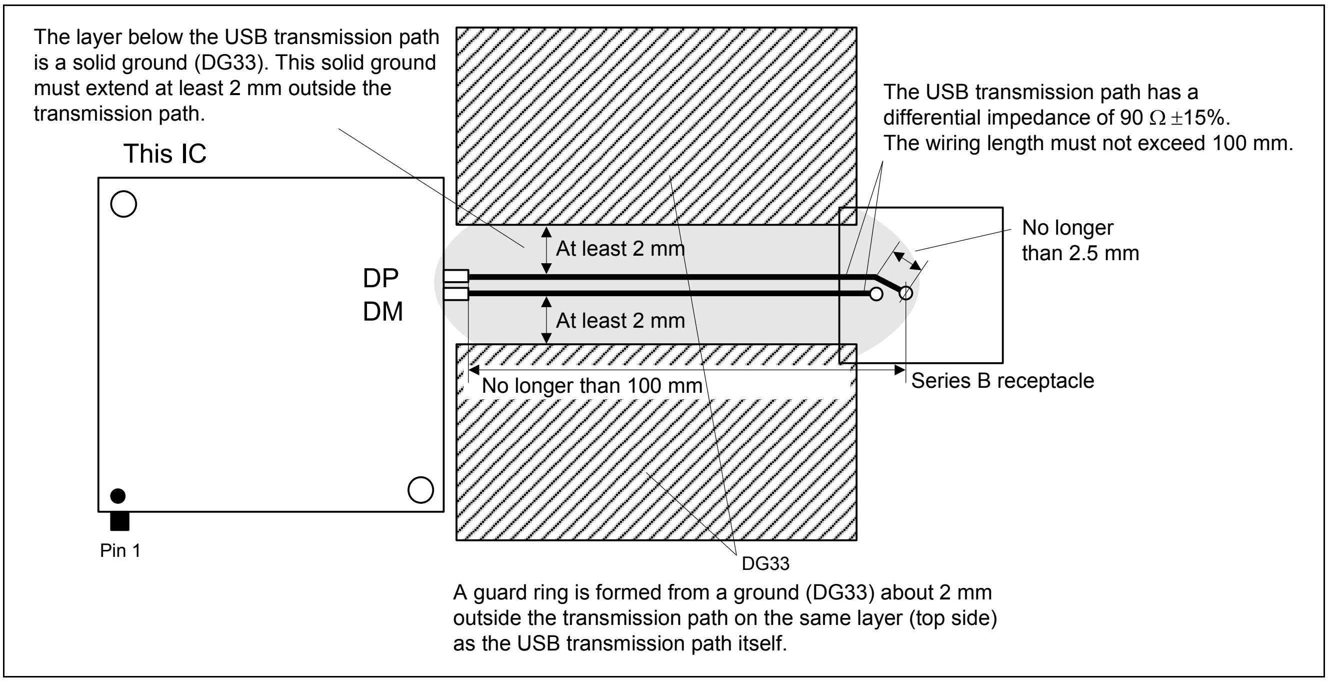


Figure 2 Function Controller USB Transmission Path Pattern Design Example

3. Power Supply and Ground Patterns

This section presents important notes on power supply and ground pattern design.

Separate power supply and ground systems for digital and analog signals should be provided. Tables 3 and 4 list the types of the power supply and ground systems.

Table 3 USB Power Supply Types

Pin Name	USB Power Supply Types Analog power supply (1.2 V)	Digital power supply (1.2 V)	Analog power supply (3.3 V)	Digital power supply (3.3 V)
AV12	○			
DV12		○*1		
UV12		○*1		
AV33			○	
DV33				○*2
Vcc		○*1		
VccQ				○*2

○: Indicates a power supply system that is used.

Notes: 1. DV12, UV12, and Vcc are connected internally in the IC.
2. DV33 and VccQ are connected internally in the IC.

Table 4 USB Ground Types

Pin Name/ USB Connector	USB Ground Types Analog ground (AGND)	Digital ground (DGND)
AG12	○*3	
DG12		○*4
UG12		○*4
AG33	○*3	
DG33		○*4
Vss		○*4
VssQ		○*4
USB connector ground (includes the frame ground)		○

○: Indicates a ground system that is used.

Notes: 3. AG12 and AG33 are connected internally in the IC.
4. DG33, DG12, UG12, Vss and VssQ are connected internally in the IC.

- Pins connected internally in the IC should be connected on the circuit board with low impedance.
- The power supply and ground patterns should have as wide an area as is possible in the pattern design.
- We recommend using either tantalum capacitors or ceramic capacitors with good high-frequency characteristics for the power supply capacitors.
- Since aluminum electrolytic capacitors can affect the eye pattern observed during testing, they should only be used after thoroughgoing design and testing.
- We recommend locating the decoupling capacitors with values of 0.001 µF, 0.01 µF, 0.1 µF, and 10 µF near the USB power supply pins. Figure 3 shows an example of decoupling capacitor positioning.

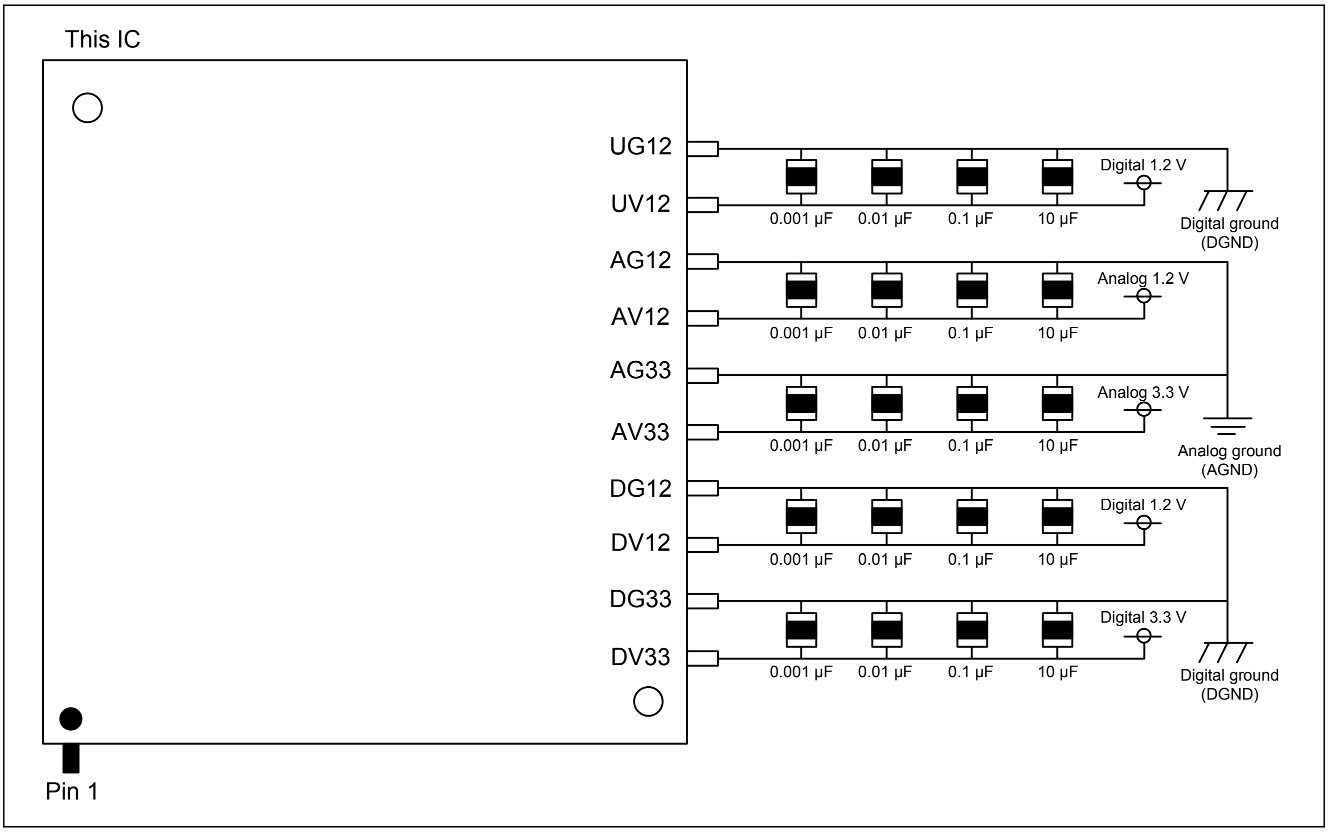


Figure 3 Decoupling Capacitor Positioning Example

4. Oscillator Circuit

This section presents important notes on oscillator circuit design.

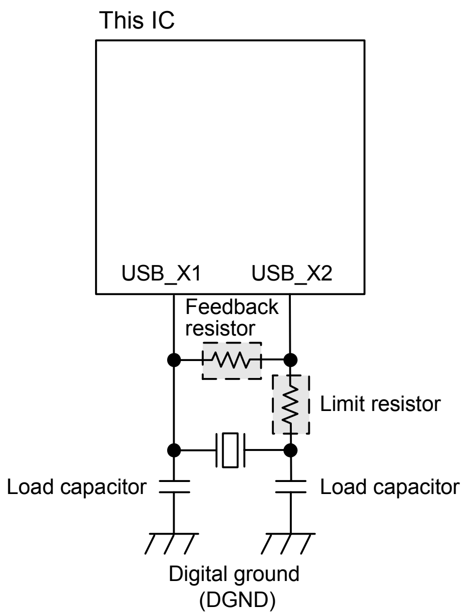
- The oscillator circuit should be positioned as close as possible to the USB_X1 USB clock input pin. We recommend surrounding the USB_X1 pin with a ground guard ring.
- Use a circuit that meets the frequency specifications listed in table 5 for the oscillator circuit.

Table 5 USB_X1 Clock Input Frequencies

Function Used	Frequency Specification (fEX)
When hi-speed transmission is used	48 MHz ±100 ppm
When hi-speed transmission is not used, but the host controller function is used	48 MHz ±500 ppm
When hi-speed transmission is not used and the host controller function is not used as well	48 MHz ±2500 ppm

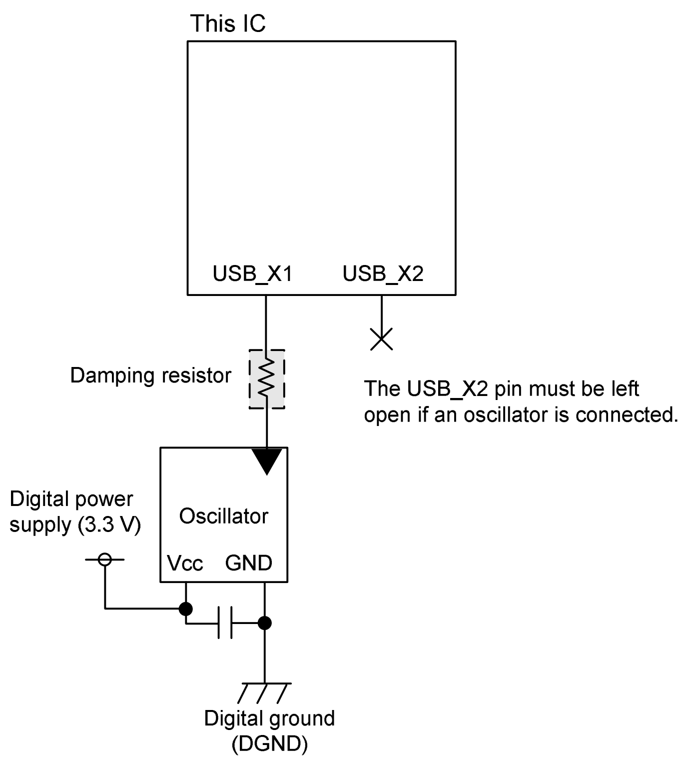
- If a crystal element is used, determine the circuit constants in consultation with the crystal element manufacturer.

Figure 4 shows a sample crystal element connection and figure 5 shows a sample oscillator connection.



Note: The values of the feedback resistor, limit resistor, and load capacitors must be determined based on and evaluation of matching to the oscillator characteristics for the crystal element used. Depending on the oscillator characteristics, the feedback resistor and limit resistor may not be required.

Figure 4 Crystal Element Connection Example



Note: Since overshoot or undershoot may occur depending on the oscillator used, we recommend providing a place in the pattern where a damping resistor can be inserted.

Figure 5 Oscillator Connection Example

5. VBUS Power Supply Circuit

This section presents important notes on VBUS power supply circuit design.

- When using this IC as a host controller, design the application so that the added capacitance of the VBUS line is at least 120 µF.
- When using this IC as a function controller, design the application so that the added capacitance of the VBUS line is in the range 1.0 to 10 µF.
- Since there are cases where impedance mismatch when the USB cable is connected can cause overshoot in the VBUS line, a filter circuit must be provided. Add a capacitor with a value in the range 1.0 to 10 µF and a resistor with a value in the range 100 Ω to 1 kΩ as a filter circuit. Note that the final values of these components must be determined by confirming that overshoot does not occur in the actual circuit board. Do not use a resistor with a value in excess of 1 kΩ during this determination.
- When using this IC as a host controller, it must be able to provide the VBUS power supply to function equipment. We recommend using a power switch IC (referred to as the USB power supply switch IC below) that includes a USB power supply bus overcurrent limiter function for VBUS power supply control.

  Determine the limit value for the VBUS power supply line current based on the application system power supply and the current values required by the USB function equipment that will be communicating over the bus. Also, refer to the circuit examples and other information provided in the datasheet for the USB power supply switch IC used when designing the VBUS power supply control circuit.

Figure 6 shows a VBUS power supply circuit example when this IC is used as a host controller, and figure 7 shows a VBUS power supply circuit example when this IC is used as a function controller.

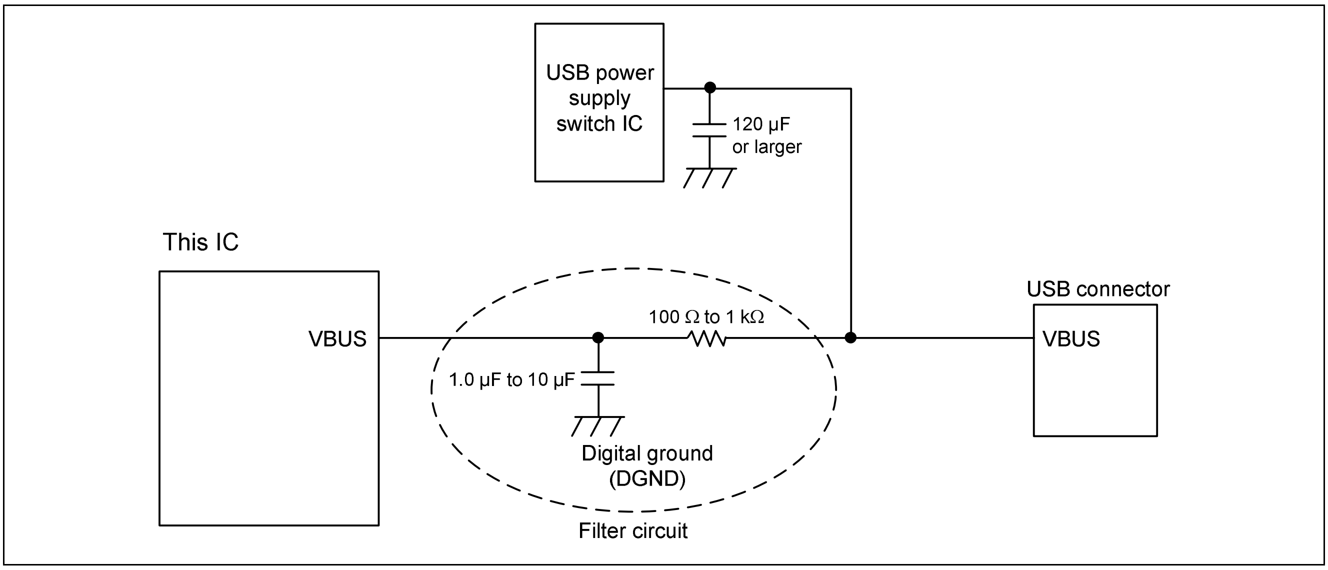


Figure 6 Host Controller VBUS Circuit Example

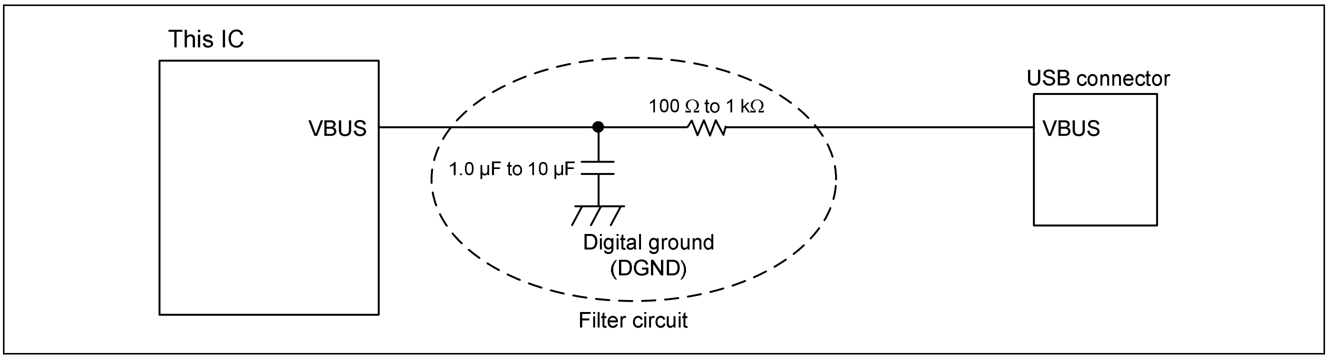


Figure 7 Function Controller VBUS Circuit Example

6. REFRIN Pin

This section presents important notes on the design of circuits associated with the REFRIN pin.

- Connect a 5.6 kΩ ±1% resistor (referred to as the reference resistor below) between the REFRIN pin and AG33.
- Position the reference resistor as close as possible to the IC.
- Connect the REFRIN pin, the reference resistor, and AG33 with pattern traces that are as wide and as short as possible.
- Connect the reference resistor and AG33 with a dedicate trace in the pattern, and connect its final end to the analog ground. This trace must be designed so that there are no shared impedances with any other signals.
- To avoid crosstalk, do not allow any signals with rapid changes (such as DP, DM, clock, address, data, or control signals) in the vicinity of the reference resistor or its pattern traces to cross or run in parallel with those traces. We recommend surrounding the reference resistor and its pattern with a ground guard ring.

Figure 8 shows the circuit diagram for the REFRIN pin and a pattern design example.

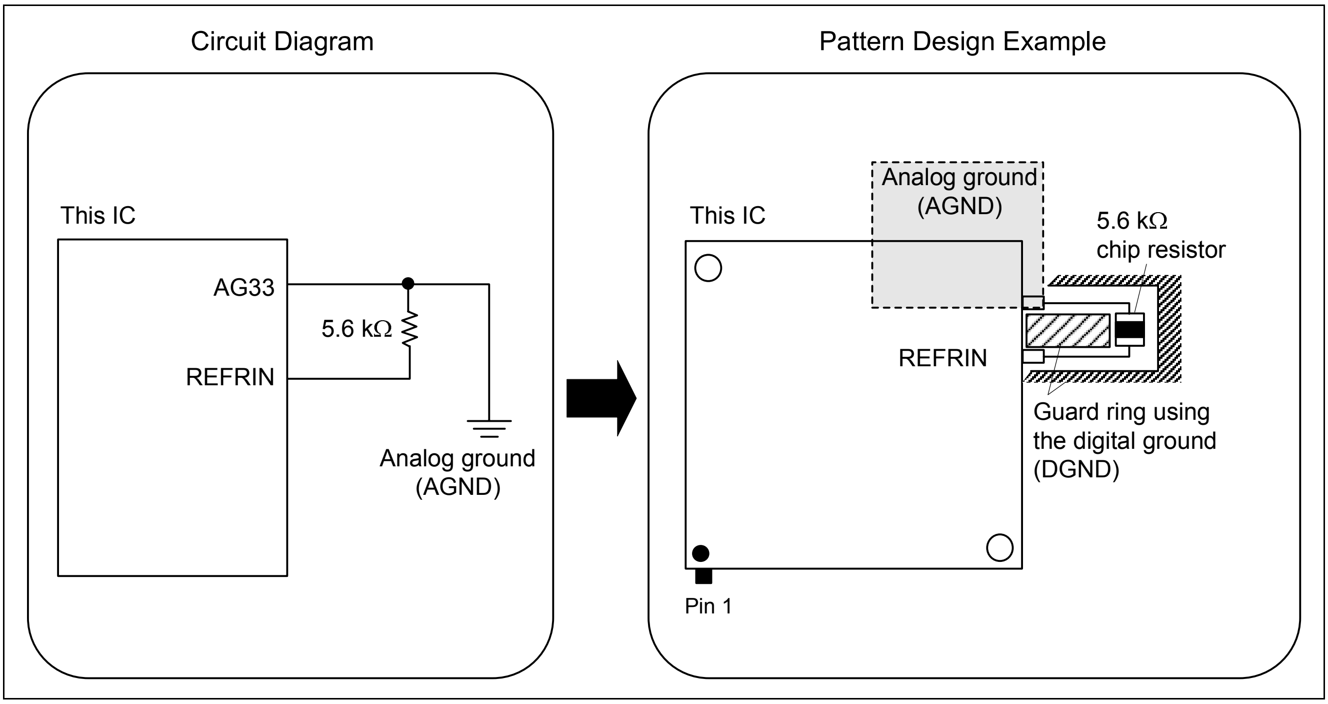


Figure 8 REFRIN Pin Circuit Diagram and Pattern Design Example

7. EMI/ESD Countermeasures

This section presents important notes on EMI and ESD countermeasures.

- If components used as EMI or ESD countermeasures, such as inductors and diodes, are mounted in the USB transmission path, they must be placed close to the USB transmission path and their connection lines made as short as possible.
- Only use components that support the USB 2.0 standard as EMI or ESD countermeasure components. Note that mounting EMI or ESD countermeasure components may result in USB transmission path impedance mismatching and waveform disruptions. Therefore the components used must be chosen based on thorough testing and evaluation.

Figure 9 shows a sample circuit diagram when EMI and ESD countermeasure components are used.

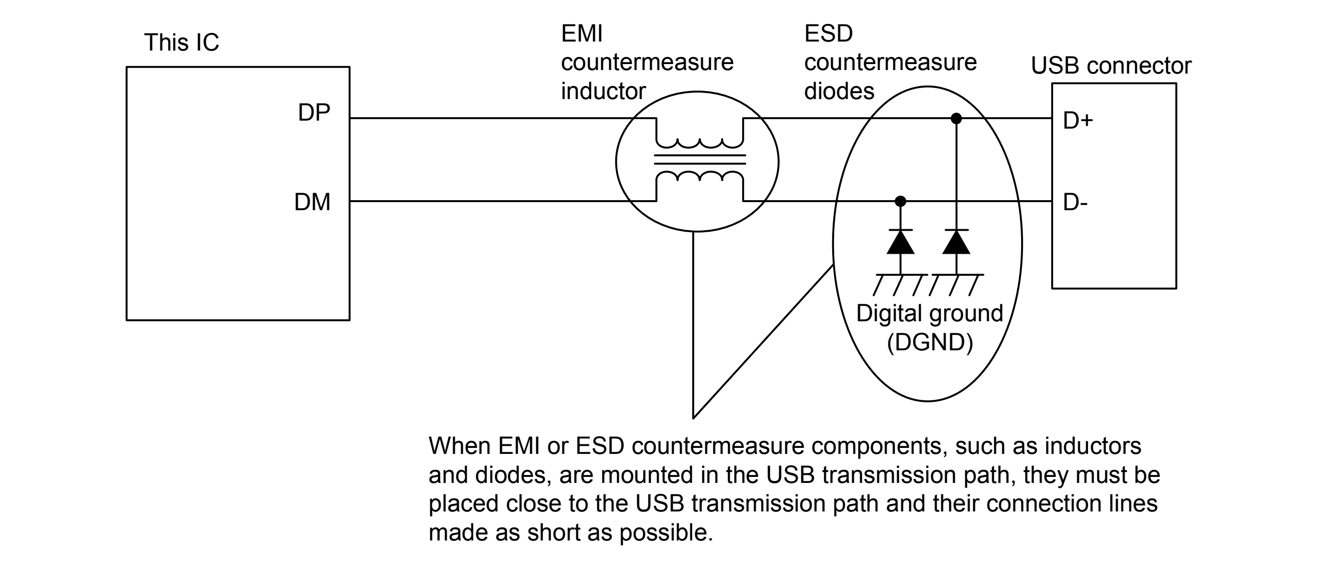


Figure 9 EMI and ESD Countermeasure Circuit Diagram Example

8. Reference Documents

- Hardware Manual
  SH7670 Group Hardware Manual Revision.2.00
  (The latest version can be downloaded from the Renesas Electronics Web site.)

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.04.11	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Colophon 1.1