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SH7670 Group

Example of BSC Flash Memory Connection

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Summary

This document describes a common case of setting up the bus state controller (BSC) in the form of a practical example of connection between flash memory and a normal space of the SH7670/SH7671/SH7672/SH7673.

Target Device

SH7670 MCU

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1. Introduction

1.1 Specifications

- 8-MB NOR-type flash memory (4 Mwords × 16 bits) is connected, with a 16-bit data bus width, to the SH7670.
- The bus state controller (BSC) of the SH7670 is used to set up conditions for the execution of read and write operations.

1.2 Module Used

- Bus state controller (BSC)

1.3 Applicable Conditions

MCU	SH7670
Operating Frequency	Internal clock: 200 MHz
	Bus clock: 66.6 MHz
	Peripheral clock: 33.3 MHz
Integrated Development	Renesas Electronics
Environment	High-performance Embedded Workshop Ver.4.03.00
C Compiler	Renesas Electronics SuperH RISC engine Family
	C/C++ compiler package Ver.9.01 Release 01
Compiler Options	Default setting in the High-performance Embedded Workshop
	(-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all
	-infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7670 Group Example of Initialization

2. Description of the Sample Application

2.1 Operational Overview of Function Used

The BSC of SH7670 is used to control externally connected flash memory. Table 1 shows the specifications of the flash memory used in this sample program.

Table 1 Flash Memory Specifications Used in this Sample Program

Item	Flash Memory Specification	
Product Type No.	S29GL064A90TFIR4 (manufactured by SPANSION)	
Configuration	8 Mbytes (4 Mwords $\times$ 16 bits $\times$ 1)	
Access Time	At random access:	90 ns (Max)
	At page read:	25 ns (Max)
Boot Block	Bottom boot	

Figure 1 is the memory map. Specifications to suit the type of memory to be connected and set up the corresponding data bus width are made per CS space. In this sample program, flash memory is connected to the CS0 space.
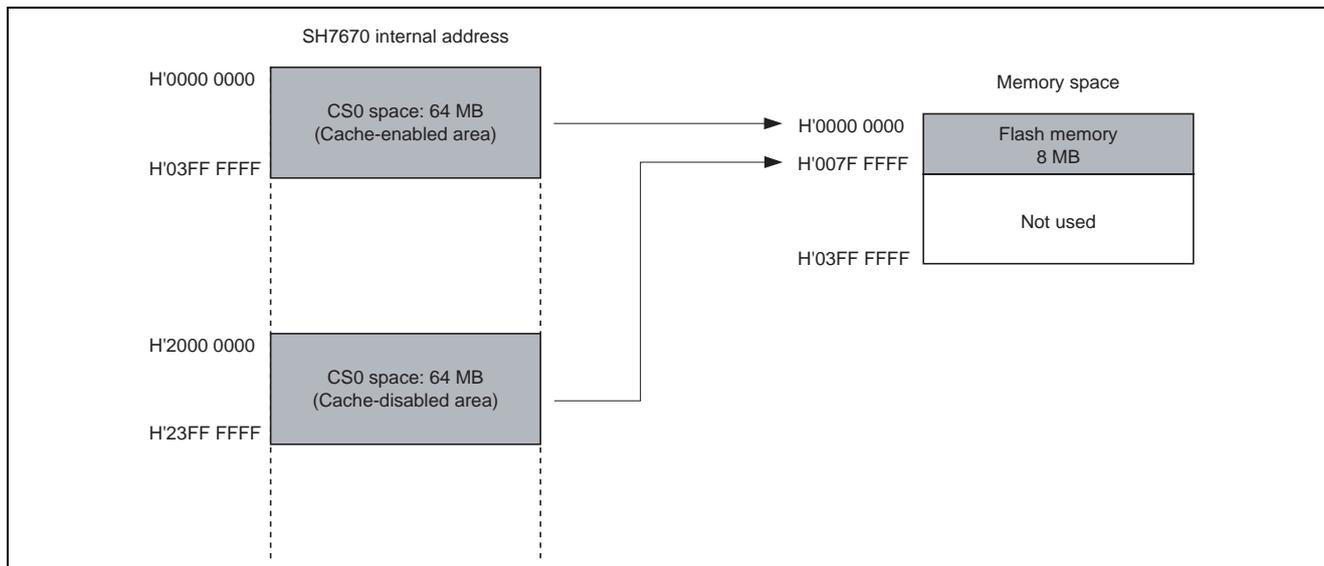

Figure 1 Memory Map of Flash Memory

Figure 2 shows an example of a circuit used to connect flash memory.

SH7670 is connected to S29GL064A90TFIR4 with a 16-bit data bus width. To set up the S29GL064A90TFIR4 to operate with a data-bus width of 16 bits, the BYTE pin is fixed to the high level. To set up the CS0 space of the SH7670 for the same bus width, the MD_BW pin is fixed to the low level. As pins A22 to A17 of the SH7670 are set up as port pins immediately after power is supplied, these pins are pulled down.
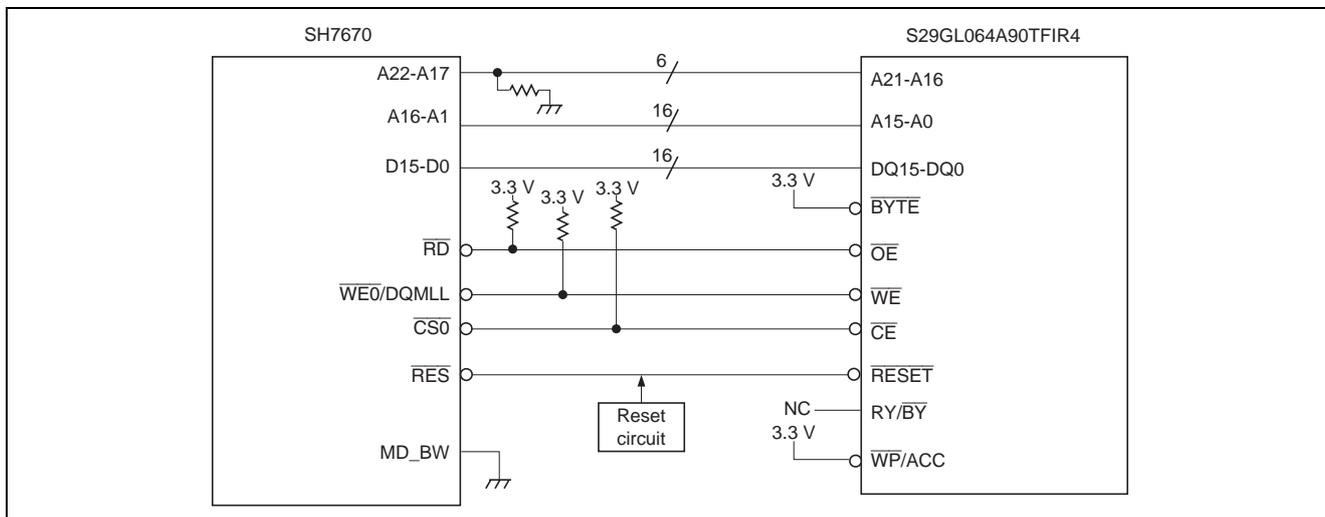

Figure 2   Sample Circuit for the Connection of Flash Memory

Table 2 shows pin functions of the SH7670. Pins A22 to A17 are initially set for operation as I/O pins. The pin-function controller (PFC) must thus be used to switch the functions of these pins.

Table 2   SH7670 Pin Functions

SH7670 Pin	Input/Output	Initial Pin Function	Function
A22 to A17	Output	I/O port (PA22 to PA17)	Address bus
A16 to A1	Output	A16 to A1	Address bus
D15 to D0	Input/output	D15 to D0	Data bus
RD	Output	RD	Read pulse signal (read data output enable signal)
WE0	Output	WE0	Indicates byte writing on D7 to D0
CS0	Output	CS0	Chip selection
MD_BW	Input	MD_BW	Selects initial values for the data-bus width in the CS0 space. This cannot be changed after a power-on reset.

MD_BW	Data Bus Width
0	16 bits
1	8 bits

2.2   Procedure for Setting of Functions Used

Table 3 gives an example of the bus state controller settings. For details on the individual registers, please refer to the section on the bus state controller in *the SH7670 Group Hardware Manual.*

Figure 3 shows an example of the procedure for setting up the bus state controller.

Table 3   Example of Bus State Controller Setting

| Name of Register	Address	Setting Value	Function
CS0 space bus control register (CS0BCR)	H'FFFC 0004	H'1000 0400	IWW[2:0] = B'001: Idle period in cycles for insertion between writing and reading and between writing and writing: 1 IWRWD[2:0], IWRWS[2:0], IWRRD[2:0], IWRRS[2:0] = B'000: No idle cycles inserted TYPE[2:0] = B'000: Normal space ENDIAN = "0": Arranged in big endian BSZ[1:0] = B'10: 16-bit data bus width Note: Values written to the BSZ[1:0] bits (bits to specify data bus width) in this register will be ignored. Please set the MD_BW pin to specify the width of the data bus in the CS0 space.
CS0 space wait control register (CS0WCR)	H'FFFC 0028	H'0000 0AC1	SW[1:0] = B'01: Delay from address and $\overline{CS0}$ assertion to $\overline{RD}$ or $\overline{WE}$ assertion in cycles: 1.5 WR[3:0] = B'0101: Number of access-wait cycles: 5 WM = B'1: Ignore external wait input HW[1:0] = B'01: Delay from $\overline{RD}$ or $\overline{WE}$ negation to address and $\overline{CS}$ negation in cycles: 1.5
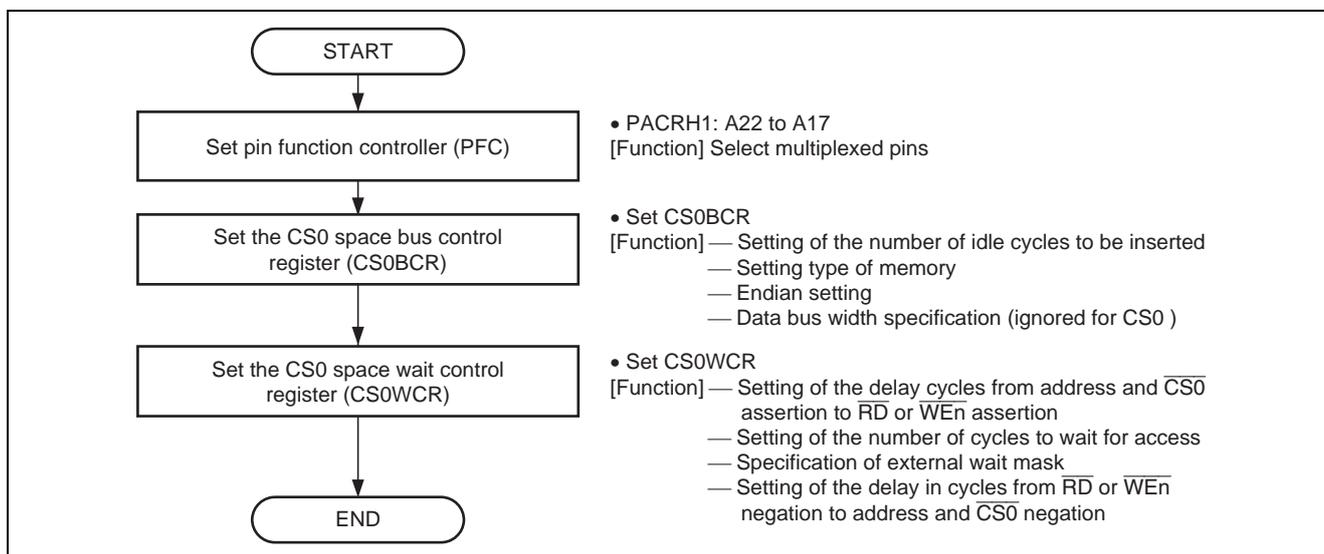
Figure 3   Example of the Procedure for Setting up the Bus State Controller (CS0 Space)

2.3 Operation of the Sample Program

In this sample program, we set the numbers of wait cycles required to support the access speed of the memory unit (S29GL064A90TFIR4) to be connected. The SH7670 establishes a frequency of 66.67 MHz (tcyc = 15 ns) as an operating condition for the bus clock. For the AC characteristics of the SH7670 and S29GL064A90TFIR4, please refer to the datasheets for the individual devices.

The settings for wait cycles in this sample program are as follows.

1. Extension of CS assertion period
   — Delay cycle (Th) from address and CS0 assertion to RD and WE0 assertion
   In this sample program, the delay cycle is set to 1.5 cycles (Th = 1.5). The equation below confirms that this setting satisfies the tCS (chip enable setup time) requirement of the S29GL064A90TFIR4.

   $$tCS\ (Min) \leq tcyc \times (Th - 0.5) + tWED1\ (Min) - tCSD1\ (Max)$$

   — Delay cycle (Tf) from RD and WE0 negation to the address and CS0 negation
   In this sample program, the delay cycle is set to 1.5 cycles (Tf = 1.5). The equation below confirms that this setting satisfies the tAH (address hold time) requirement of the S29GL064A90TFIR4.

   $$tAH\ (Min) \leq tcyc \times (Tw + 2 + (Tf - 0.5)) + tAD1\ (Min) - tWED1\ (Max)$$

2. Access wait cycle
   Wait cycle (Tw) between T1 and T2 cycles. In this sample program, the setting is 5 cycles (Tw = 5).
   The equations below confirm that this setting satisfies the bus-timing requirement of the S29GL064A90TFIR4 and SH7670.
   — tRDS1 (read data setup time 1) of SH7670

   $$tRDS1\ (Min) \leq tcyc \times (Tw + 2 + (Th - 0.5)) - tAD1\ (Max) - tACC$$
   $$tRDS1\ (Min) \leq tcyc \times (Tw + 2 + (Th - 0.5)) - tCSD1(Max) - tCE$$
   $$tRDS1\ (Min) \leq tcyc \times (Tw + 2) - tRSD\ (Max) - tOE$$

   — tRDH1 (read data hold time 1)

   $$tRDH1\ (Min) \leq tOH\ (Min)$$

   — tRC (read cycle time) of S29GL064A90TFIR4

   $$tRC\ (Min) \leq tcyc \times (Tw + 2 + (Th - 0.5) + (Tf - 0.5))$$

   — tWC (write cycle time) of S29GL064A90TFIR4

   $$tWC\ (Min) \leq tcyc \times (Tw + 2 + (Th - 0.5) + (Tf - 0.5))$$

   — tAS (address setupt time) of S29GL064A90TFIR4

   $$tAS\ (Min) \leq tcyc \times (Tw + 2 + (Th - 0.5) + (Tf - 0.5))$$

   — tWP (write pulse width) of S29GL064A90TFIR4

   $$tWP\ (Min) \leq tcyc \times (Tw + 1)$$

   — tDS (data setup time) of S29GL064A90TFIR4

   $$tDS\ (Min) \leq tcyc \times (Tw + 1 + (Th - 0.5)) - tWDD1\ (Max) + tWED1\ (Min)$$

   — tDH (data hold time) of S29GL064A90TFIR4

   $$tDH\ (Min) \leq tWDH3\ (Min)$$

3. Wait between access cycles
   Wait between access cycles is the wait setting for insertion between consecutive rounds of access. In this sample program, 1 cycle (Taw = 1) is set as the number of cycles to wait between cycles of writing and reading or of writing and writing.
   The equation below confirms that this satisfies the tWPH (H write pulse width) requirement of the S29GL064A90TFIR4.

   $$tWPH\ (Min) \leq tcyc \times (1 + (Th - 0.5) + (Tf - 0.5) + Taw)$$

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Figure 4 shows the timing of flash memory reading when Th = 1.5, Tw = 4 and Tf = 1.5 with the bus clock running at 66.67 MHz (the settings are not the same as those in the sample program).
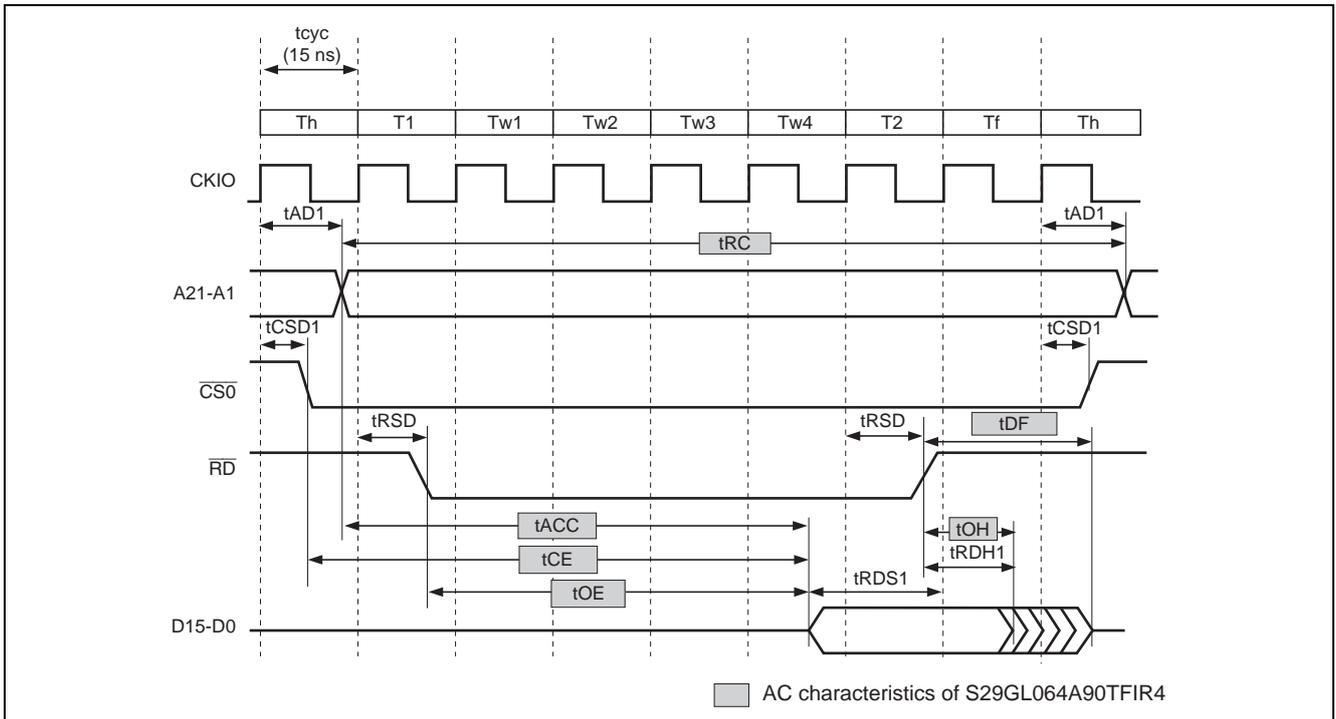

Figure 4   Timing of Flash Memory Reading (with the bus clock at 66.67 MHz)

Figure 5 shows the timing of flash memory writing when Th = 1.5, Tw = 4, Tf = 1.5 and wait between write-write cycles (Taw) = 1 with the bus clock running at 66.67 MHz (the settings are not the same as those in the sample program).
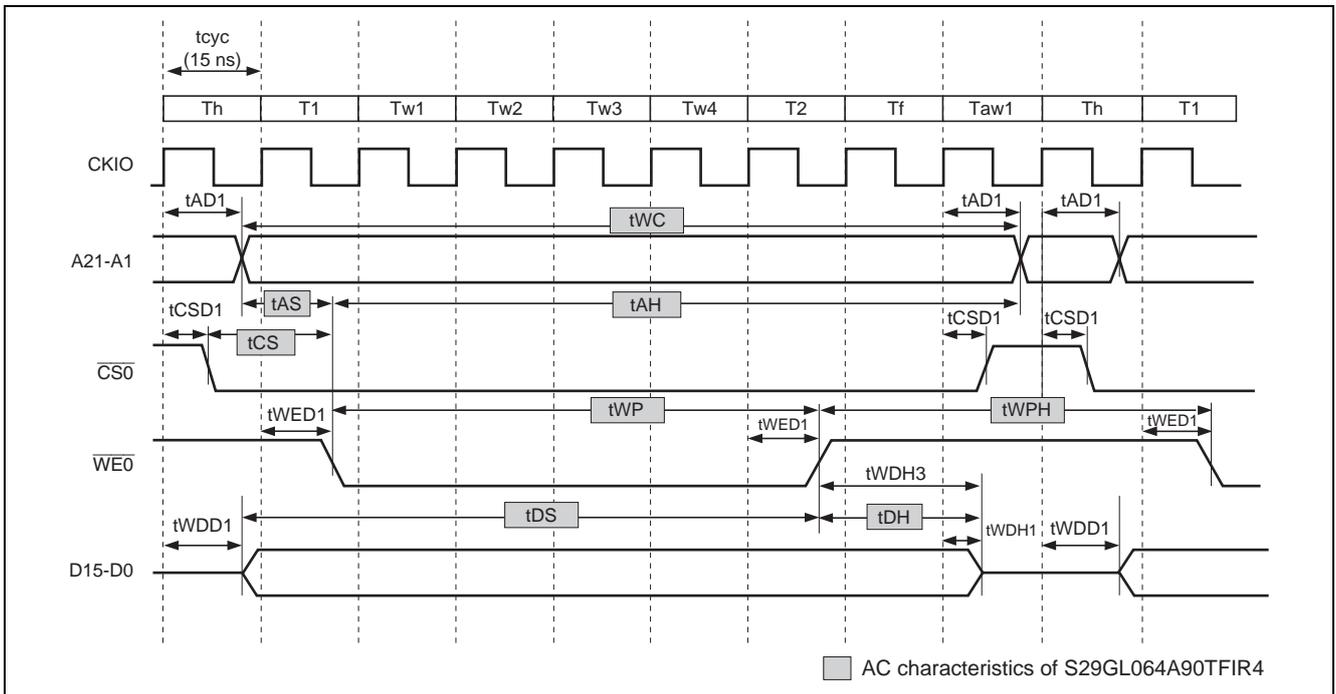
Figure 5   Timing of Flash Memory Writing (with the bus clock at 66.67 MHz)

3.   Sample Program Listing

3.1   Sample program list "bsc_cs0.c" (1)

```
1    /*****************************************************************************
2    *    DISCLAIMER
3    *
4    *    This software is supplied by Renesas Electronics Corporation and is only
5    *    intended for use with Renesas products. No other uses are authorized.
6    *
7    *    This software is owned by Renesas Electronics Corporation and is protected under
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24   *    By using this software, you agree to the additional terms and
25   *    conditions found by accessing the following link:
26   *    http://www.renesas.com/disclaimer
27   *****************************************************************************
28   * Copyright (C) 2007(2010) Renesas Electronics Corporation. All rights reserved.
29   *""FILE COMMENT""*********** Technical reference data *************************
30   *    System Name : SH7671 Sample Program
31   *    File Name   : bsc_cs0.c
32   *    Abstract    : SH7671 Initial Settings
33   *    Version     : 1.00.03
34   *    Device      : SH7671
35   *    Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36   *                : C/C++ compiler package for the SuperH RISC engine family
37   *                :                           (Ver.9.01 Release01).
38   *    OS          : None
39   *    H/W Platform: M3A-HS71(CPU board)
40   *    Description :
41   *****************************************************************************
42   *    History     : Jul.03,2007 ver.1.00.00
43   *                : Dec.18,2009 ver.1.00.01 Updated header comments
44   *                : Apr.07,2010 ver.1.00.02 Changed the company name and device name
45   *                : Oct.08,2010 ver.1.00.03 Changed the copyright
46   *""FILE COMMENT END""*****************************************************/
47   #include "iodefine.h"
48
49   /* ==== Prototype Declaration ==== */
50   void io_init_bsc_cs0(void);
```

3.2   Sample program list "bsc_cs0.c" (2)

```
51
52    #pragma section ResetPRG
53    /*""FUNC COMMENT""*********************************************************
54     * ID          :
55     * Outline      : CS0 setting
56     *-----------------------------------------------------------------------
57     * Include      : "iodefine.h"
58     *-----------------------------------------------------------------------
59     * Declaration  : void io_init_bsc_cs0(void);
60     *-----------------------------------------------------------------------
61     * Description  : Pin function controller (PFC) and bus state controller (BSC)
62     *              : are set, and the access timing to the FlashMemory of CS0 area
63     *              : is set.
64     *-----------------------------------------------------------------------
65     * Argument     : void
66     *-----------------------------------------------------------------------
67     * Return Value : void
68     *-----------------------------------------------------------------------
69     * Note         :
70    *""FUNC COMMENT END""*****************************************************/
71    void io_init_bsc_cs0(void)
72    {
73
74      /* ==== PFC settings ==== */
75      PORT.PACRH1.WORD = 0x1554;      /* Set A17-A22 */
76
77      /* ==== CS0BCR settings ==== */
78      BSC.CS0BCR.LONG = 0x10000400UL;
79                                  /* Idle Cycles between Write-read Cycles */
80                                  /*  and Write-write Cycles :1idle cycles */
81                                  /* Data Bus Size:16-bit size */
82
83      /* ==== CS0WCR settings ====  */
84      BSC.CS0WCR.LONG = 0x00000ac1UL;
85                                  /* Number of Delay Cycles from Adress, */
86                                  /*  CS0# Assertion to RD#,WEn Assertion */
87                                  /*  :1.5cycles */
88                                  /* Number of Access Wait Cycles:5cycles */
89                                  /* Delay Cycles from RD,WEn# negation to */
90                                  /*  Address,CSn# negation:1.5cycles */
91    }
92
93    /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7670 Group Hardware Manual Rev. 2.00
  The latest version of the hardware user's manual can be downloaded from the Renesas Electronics website.

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Revision Record

| Rev. | Date | Description | |
		Page	Summary
1.00	Nov.19.08	—	First edition issued
1.01	Oct.15.10	—	Changed the sample program (AC Switching Characteristics are removed)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141