
SH7450 Group, SH7451 Group

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Data Communication Using the DRO and DRI

Abstract

This document describes sample code for performing data communication using the direct RAM output interface (DRO) and direct RAM input interface (DRI) in the SH7450 Group and SH7451 Group (hereinafter referred to collectively as the SH7450).

Products

SH7450 Group, SH7451 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU. In addition, although the sample code presented in this application note has been confirmed to operate as intended, refer to the latest version of the hardware manual and perform a thorough evaluation before using.

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1. Specifications

The sample code uses the DRI to capture data output by the DRO. It can be used to perform loop-back communication on a single SH7450 evaluation board or data communication between two evaluation boards. DRO and DRI initialization, DRO data output, and DRI data capture are controlled by toggle switches mounted on the evaluation board. Table 1.1 lists the peripheral functions and their applications, table 1.2 lists control details for the toggle switches, and figures 1.1 and 1.2 show usage examples. For details on the functions of the pins shown in the figures, see table 4.1.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
DRO (direct RAM output interface)	Outputs data from the SH7450 on-chip SHwyRAM.
DRI (direct RAM input interface)	Captures parallel data to the SH7450 on-chip SHwyRAM.

Table 1.2 Toggle Switch Control Details

Toggle Switch	Input	Control Details
S7	"H"	DRI initialization enable
	"L"	DRI initialization disable
S6	"H"	DRO initialization enable
	"L"	DRO initialization disable
S5	"H"	DRI data capture enable
	"L"	DRI data capture disable
S4	"H"	DRO data output enable
	"L"	DRO data output disable

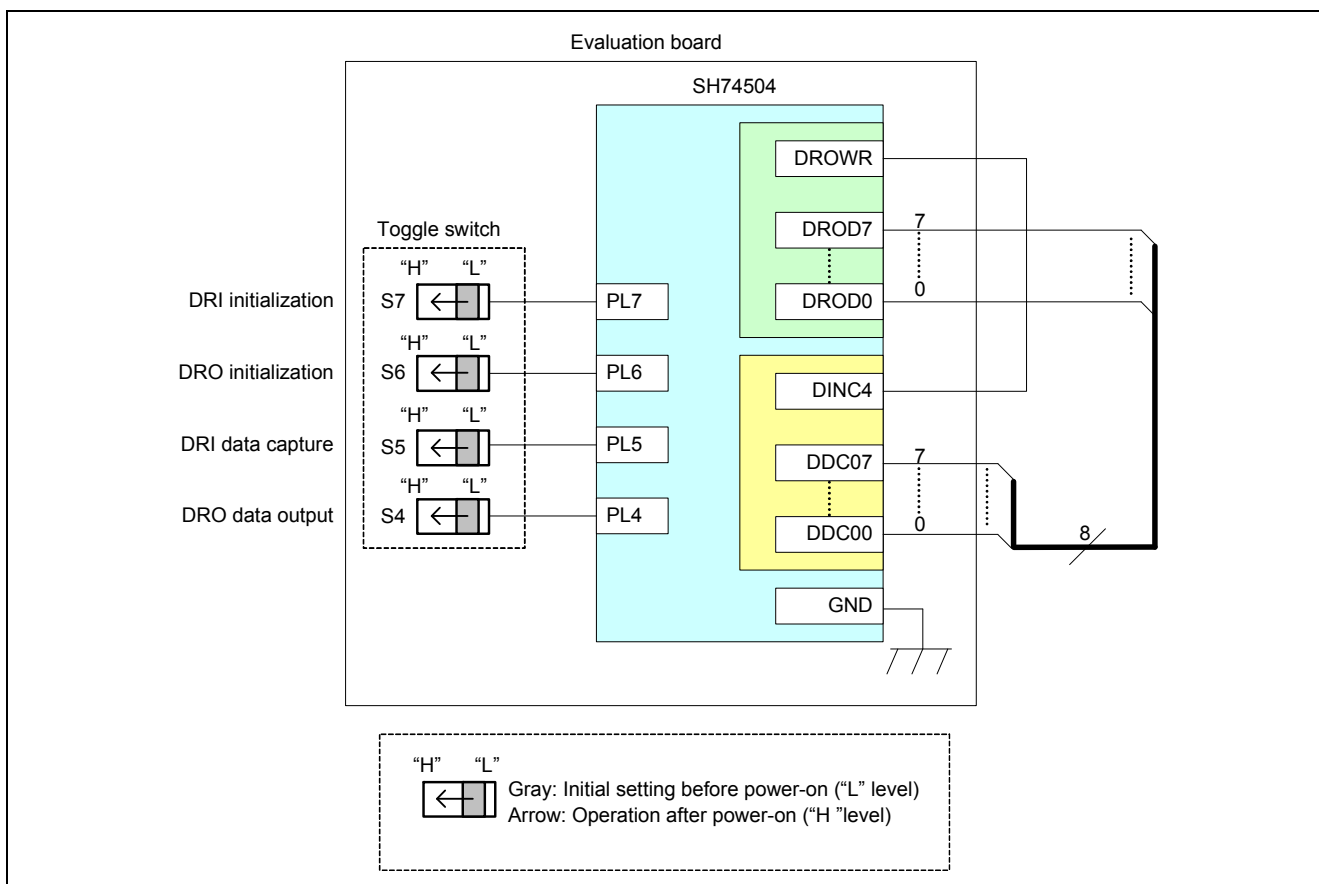


Figure 1.1 Usage Example: Loop-Back Communication

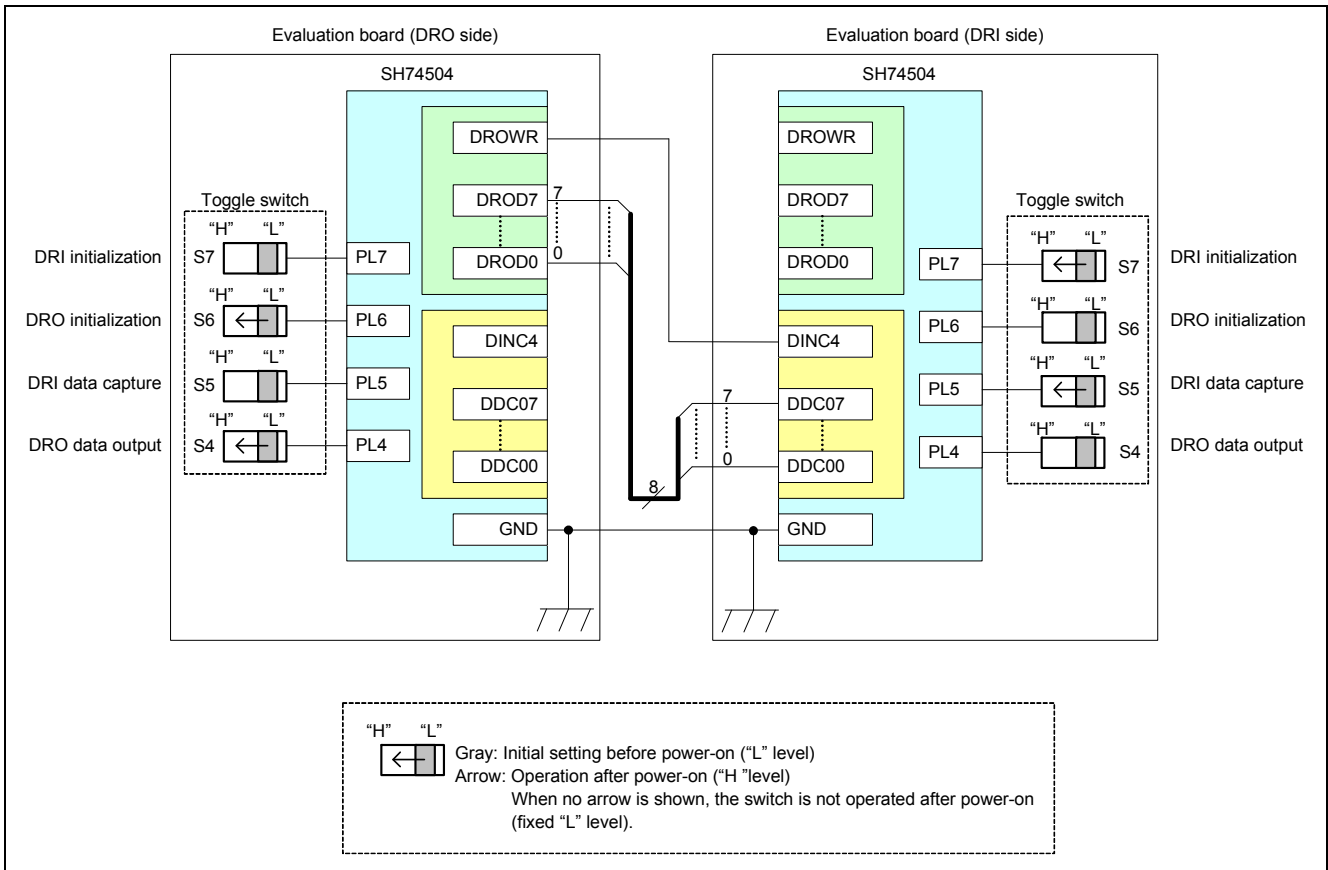


Figure 1.2 Usage Example: Data Communication between Evaluation Boards

2. Confirmed Operating Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU	SH7450 Group, SH7451 Group
Operating frequencies	Input clock: 20 MHz CPU clock (Ick): 240 MHz SHwy clock (SHck): 80 MHz Peripheral clock (Pck): 40 MHz Peripheral A clock (PAck): 80 MHz
Operating voltage	PVcc = Vcc = PLLVcc = AVcc = 5 V, Vdd = 1.5 V
Operating mode	Single-chip mode
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Version 4.09.00.007 (HEW)
C/C++ compiler	Renesas Electronics C/C++ compiler package for SuperH RISC engine family V.9.04 Release 00 Options: The following options are the HEW default settings. -cpu=sh4a -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Sample code version	Version 1.00
Evaluation board used	SH7450 evaluation board (product No.: R0K474504C000BR/R0K474504C010BR)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

SH7450 Group/SH7451 Group Register Definition Header File (R01AN0190EJ0102)

4. Hardware

4.1 Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Description
PH7/DDC07 to PH0/DDC00	Input	DRI input data
PK5/DINC4	Input	DRI input event signal
PH15/DROD7 to PH8/DROD0	Output	DRO output data bus
PL2/DROWR	Output	DRO output data strobe
PL7 to PL4	Input	Level input for toggle switches S7 to S4

5. Software

5.1 Operation Overview

The sample code uses the DRI to capture 256 bytes of user-defined data (in the sample code, byte data with values from H'00 to H'FF) output by the DRO. Toggle switches S7 to S4 on the evaluation board are used to perform loop-back communication on a single evaluation board or data communication between two evaluation boards. Toggle switch S7 controls DRI initialization, toggle switch S6 controls DRO initialization, toggle switch S5 controls DRI data capture, and toggle switch S4 controls DRO data output. The description below provides an overview of the DRO and DRI settings used in the sample code and explains loop-back communication and data communication between evaluation boards.

Note: The sample code contains sections that perform an infinite loop. In actual use, processing should be added as needed to specify a duration limit for each infinite loop and to exit the loop afterward.

5.1.1 Overview of DRO and DRI Settings

Tables 5.1 and 5.2 provide an overview of the DRO and DRI settings used in the sample code.

Table 5.1 Overview of DRO Settings

Item	Description
Transfer format	Parallel output with strobe
Access area	SHwYRAM: Output of data in the area from H'1800 1000 to H'1800 10FF
Output data width	8 bits
Transfer rate	10Mbytes/s
Strobe polarity	"H" active
Timing adjustment	2 Pck selected for setup and hold
Interrupt request	Interrupt request mask (disabled)

Table 5.2 Overview of DRI Settings

Item	Description
Channel	DRI channel 2 (DRI2)
Input to DRI2	Pins DINC4 and DDC07 to DDC00
Operating frequency	80 MHz (PAck = 80 MHz)
Transfer format	Clock-synchronous parallel input
Access area	SHwYRAM: Capture data in the area from H'1800 0000 to H'1800 00FF
Data capture bus width	8 bits
Event counter	Not used
Bank switching function	DRI2 address counter 0 selected
Data capture event	DIN4 event detection
Data capture edge	Falling edge
Capture timing adjustment function	Default (PAck rising edge at event detection)
Decimation control function	Not used
Special modes	Not used

5.1.2 Loop-Back Communication

Using a single evaluation board, 256 bytes of user-defined data are output by the DRO and captured by the DRI. A description of the loop-back communication operating procedure and an overview of the operations performed are provided below. Figure 5.1 shows a timing chart.

To begin, set the input level of toggle switches S7 to S4 to “L” and then power on the evaluation board. After power-on, sequentially change the input level of toggle switches S7, S6, S5, and S4 to “H”, in that order. The sample code operations that occur when these steps are performed are as follows.

(1) DRI Initialization

When toggle switch S7 is moved to the “H” level, the following processes are performed once:

- Enabling of clock supply to the DRI
- Initialization of ports and control block used by the DRI

(2) DRO Initialization

When toggle switch S6 is moved to the “H” level, the following processes are performed once:

- Enabling of clock supply to DRO
- Initialization of ports and output control block used by the DRO

DROWR is selected as the port pin function, and the DRO strobe polarity select bit is set to “H” active. With these settings, DROWR outputs a “L” level signal when data has not been output.

(3) DRI Data Capture Enable

When toggle switch S5 is moved to the “H” level, DRI data capture is enabled. The DRI event detection method is set to the falling edge of an external signal input to the DRI (DINC4).

(4) DRO Data Output Enable

When toggle switch S4 is moved to the “H” level, DRO data output is enabled.

(5) DRO Data Output/DRI Data Capture (Continuous Operation Controlled by Hardware)

After items (1) to (4) above are processed, data output and capture take place repeatedly for 256 bytes. In synchronization with the rising edge of DROWR, the DRO outputs 256 bytes of SHwyRAM data from pins DROD7 to DROD0, 1 byte at a time. DRO operation ends after data output is completed. When the DRI detects the falling edge of DINC4, it captures 1 byte of data from pins DDC07 to DDC00 to the SHwyRAM, and this is repeated for 256 bytes. DRI operation ends after data capture is completed.

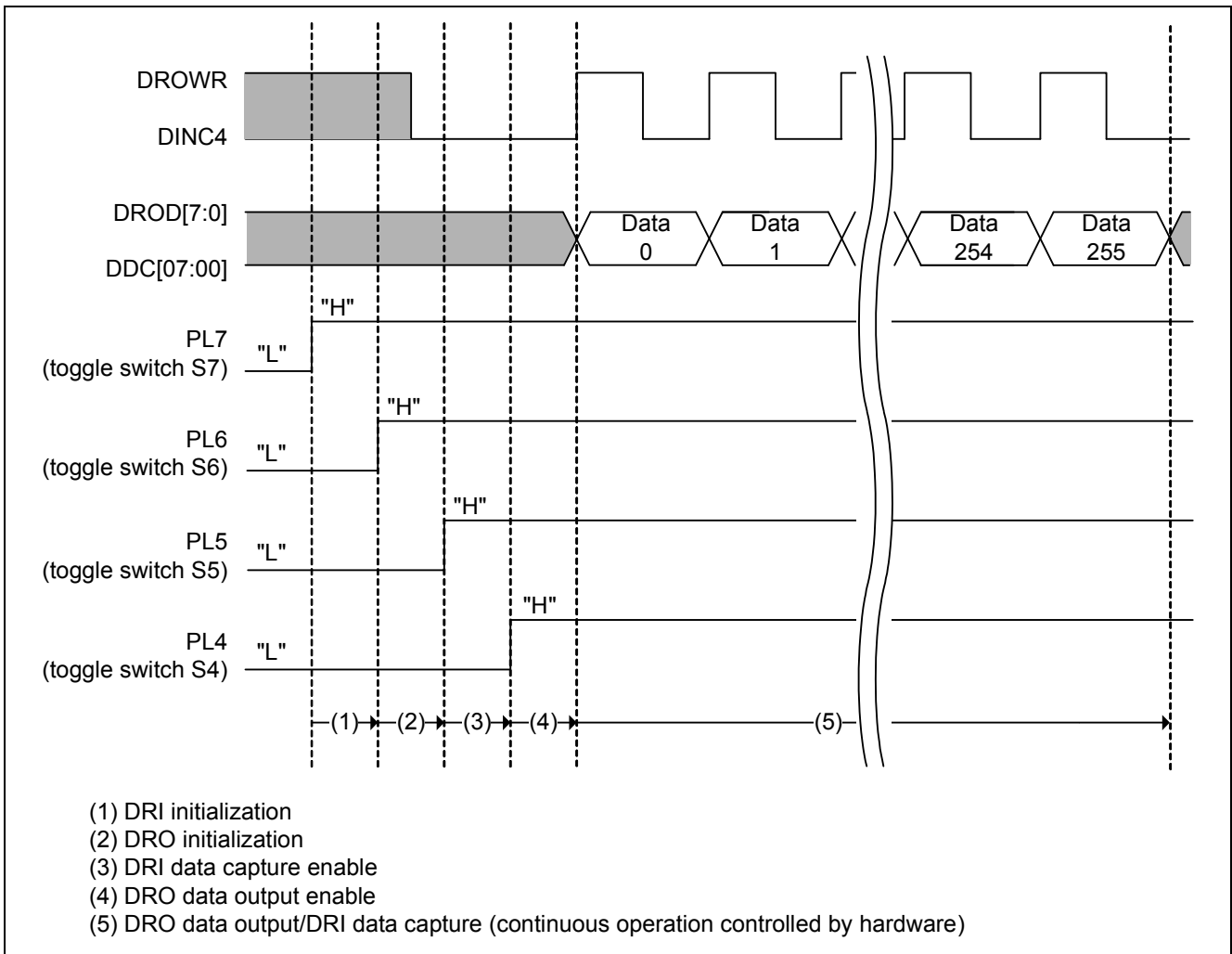


Figure 5.1 Timing Diagram of Loop-Back Communication

5.1.3 Data Communication between Evaluation Boards

When two evaluation boards are used, 256 bytes of user-defined data are output by the DRO-side evaluation board and captured by the DRI-side evaluation board. A description of the switch operating procedure for data communication between evaluation boards and an overview of the operations performed are provided below. Figure 5.2 shows a timing chart.

[DRO-Side Evaluation Board]

Set the input level of toggle switches S7 to S4 to “L” and then power on the evaluation board. After power-on, sequentially change the input level of toggle switches S6 and S4 to “H”, in that order. Before changing the input level of toggle switch S4 to “H”, make sure toggle switch S5 on the DRI-side evaluation board is set to “H” level. The sample code operations that occur when these steps are performed are described below.

(O-1) DRO Initialization

When toggle switch S6 is moved to the “H” level, the following processes are performed once:

- Enabling of clock supply to DRO
- Initialization of ports and output control block used by the DRO

DROWR is selected as the port pin function, and the DRO strobe polarity select bit is set to “H” active. With these settings, DROWR outputs a “L” level signal when data has not been output.

(O-2) DRO Data Output Enable Standby

The DRO data output disabled state is maintained while toggle switch S4 is set to “L” level.

(O-3) DRO Data Output Enable

When toggle switch S4 is moved to the “H” level, DRO data output is enabled.

(O-4) DRO Data Output

(Continuous Operation Controlled by Hardware)

After items (O-1) to (O-3) above are processed, the DRO outputs 256 bytes of SHwyRAM data, 1 byte at a time, from pins DROD7 to DROD0 in synchronization with the rising edge of DROWR. DRO operation ends after data output is completed.

[DRI-Side Evaluation Board]

Set the input level of toggle switches S7 to S4 to “L” and then power on the evaluation board. After power-on, sequentially change the input level of toggle switches S7 and S5 to “H”, in that order. Before changing the input level of toggle switch S5 to “H”, make sure toggle switch S6 on the DRO-side evaluation board is set to “H” level. The sample code operations that occur when these steps are performed are described below.

(I-1) DRI Initialization

When toggle switch S7 is moved to the “H” level, the following processes are performed once:

- Enabling of clock supply to DRI
- Initialization of ports and output control block used by the DRI

(I-2) DRI Data Capture Enable Standby

The DRI data capture disabled state is maintained while toggle switch S5 is set to “L” level.

(I-3) DRI Data Capture Enable

When toggle switch S5 is moved to the “H” level, DRI data capture is enabled. The DRI event detection method is set to the falling edge of an external signal input to the DRI (DINC4).

(I-4) DRI Data Capture

(Continuous Operation Controlled by Hardware)

After items (I-1) to (I-3) above are processed, the DRI detects the falling edge of DINC4, it captures 1 byte of data from pins DDC07 to DDC00 to the SHwyRAM, and this is repeated for 256 bytes. DRI operation ends after data capture is completed.

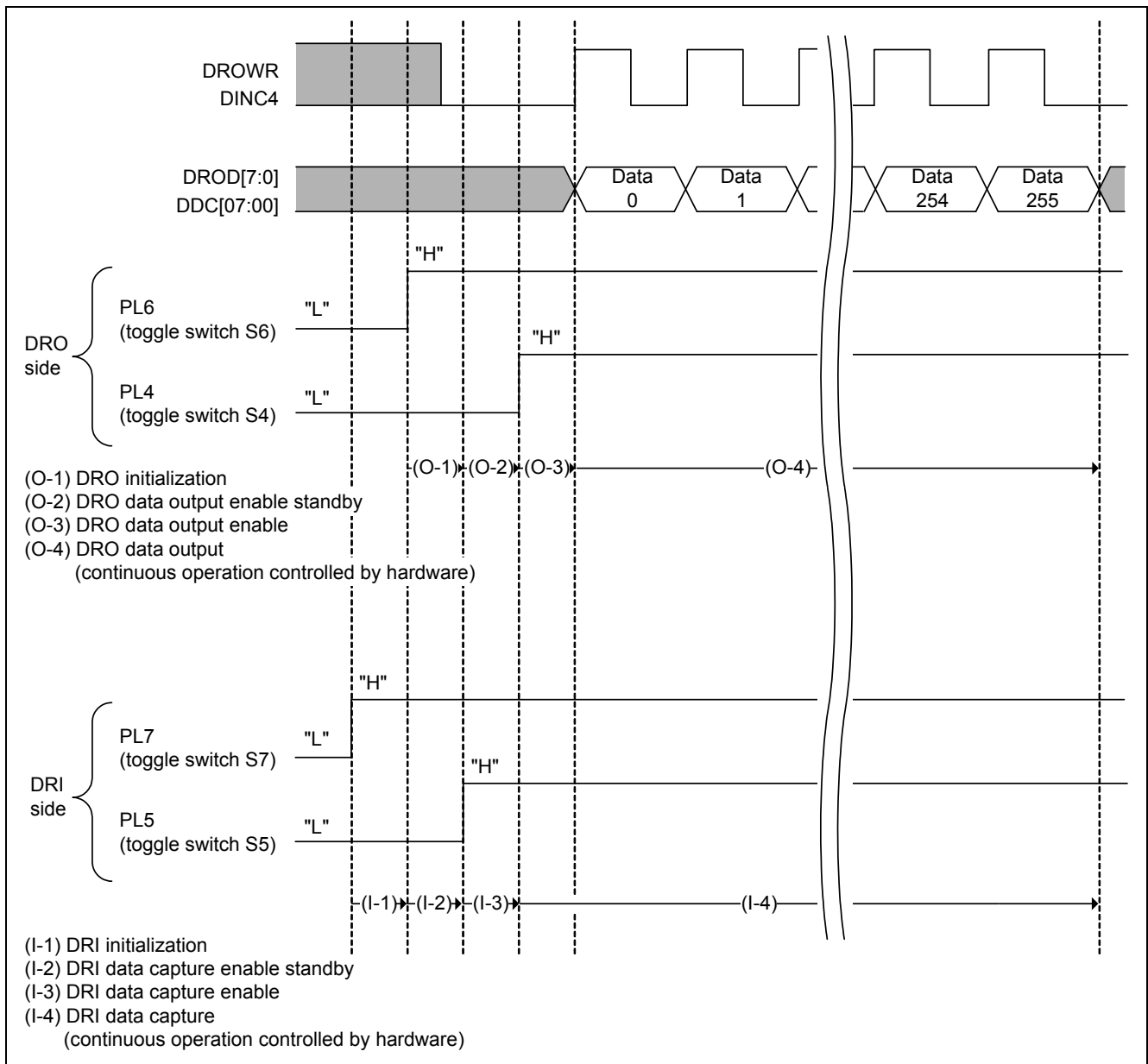


Figure 5.2 Timing Chart of Data Communication between Evaluation Boards

5.2 File Composition

Table 5.3 lists the files used in the sample code. Files not generated by the integrated development environment should not be listed in this table.

Table 5.3 Files Used in the Sample Code

File Name	Outline	Remarks
dri.c	DRI control program	
dri.h	DRI include headers for external referencing	
dro.c	DRO control program	
dro.h	DRO include headers for external referencing	
main.c	Main function program	
sh7450_iodefine_20100625.h	SH7450 Group/SH7451 Group register definition header file	

5.3 Constants

Table 5.4 lists the constants used in the sample code.

Table 5.4 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
DRI_EVENT_NO_INPUT	H'0	No input
DRI_EVENT_RISING_EDGE	H'1	Rising edge detection
DRI_EVENT_FALLING_EDGE	H'2	Falling edge detection
DRI_EVENT_BOTH_EDGE	H'3	Both edges detection
DRI_EVENT_DETECTION	DRI_EVENT_FALLING_EDGE	DRI event detection method
DRI_ACQUISITION_TIMING	H'0	Duration (Pck) from data capture event detection to data capture
DRI_DST_ADDR	H'1800 0000	SHwYRAM address for storing data captured by DRI
DRI_INPUT_INCOMPLETION	H'0	DRI data capture incomplete
DRI_INPUT_COMPLETION	H'1	DRI data capture complete
DRO_DRI_NUM_OF_DATA	H'100	DRO/DRI data transfer count
DRO_L_ACTIVE	H'0	"L" active
DRO_H_ACTIVE	H'1	"H" active
DRO_STROBE_POL	DRO_H_ACTIVE	DRO strobe polarity
DRO_SETUP_TIME	H'2	Output data setup time (Pck)
DRO_HOLD_TIME	H'2	Output data hold time (Pck)
DRO_SRC_ADDR	H'1800 1000	SHwYRAM address for storing DRO output data
DRO_OUTPUT_INCOMPLETION	H'0	DRO data output incomplete
DRO_OUTPUT_COMPLETION	H'1	DRO data output complete
EXEC_PROHIBITION	H'0	Execution disabled
EXEC_COMPLETION	H'1	Execution complete
PROCESSING_INCOMPLETION	H'0	Processing incomplete
PROCESSING_COMPLETION	H'1	Processing complete
TOGGLE_SWITCH_S7	PORT.PLDR.BIT.PL7DR* ¹	PL7 (toggle switch S7) input
TOGGLE_SWITCH_S6	PORT.PLDR.BIT.PL6DR* ¹	PL6 (toggle switch S6) input
TOGGLE_SWITCH_S5	PORT.PLDR.BIT.PL5DR* ¹	PL5 (toggle switch S5) input
TOGGLE_SWITCH_S4	PORT.PLDR.BIT.PL4DR* ¹	PL4 (toggle switch S4) input

Note: *1 Pointer to port L data register (PLDR) (address: H'FFFF 5D02).

(See the SH7450 Group/SH7451 Group peripheral function register definition file.)

5.4 Structure/Union List

Figure 5.3 shows the structures and unions used in the sample code.

```
typedef struct{                                /* Structure for storing DRO initialization parameters */
    unsigned short usStrPol;                    /* Strobe polarity */
    unsigned short usSetupTime;                /* Setup time */
    unsigned short usHoldTime;                 /* Hold time */
    unsigned long ulSrcAddr;                   /* Transfer source SHwyRAM address */
    unsigned long ulNumOfData;                 /* Output data count */
}DROINIT;

typedef struct{                                /* Structure for storing DRI initialization parameters */
    unsigned short usEvtDet;                   /* Event detection method */
    unsigned short usDataAcqTime;              /* Capture timing */
    unsigned long ulDstAddr;                   /* Transfer destination SHwyRAM address */
    unsigned long ulNumOfData;                 /* Capture event count */
}DRIINIT;
```

Figure 5.3 Structures/Unions Used in Sample Code

5.5 Variables

Table 5.5 lists the global variables.

Table 5.5 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	gucDroInitFlag	DRO initialization flag 0: Execution disabled 1: Execution complete	OutputInitCtrl
unsigned char	gucDroOutputStartFlag	DRO data output start flag 0: Execution disabled 1: Execution complete	OutputEnableCtrl, ProcessingStatus
unsigned char	gucDriInitFlag	DRI initialization flag 0: Execution disabled 1: Execution complete	InputInitCtrl
unsigned char	gucDriInputStartFlag	DRI data capture start flag 0: Execution disabled 1: Execution complete	InputEnableCtrl, ProcessingStatus
unsigned char	gucProcessingFlag	Processing status flag 0: Processing incomplete 1: Processing complete	main, ProcessingStatus
DROINIT	gstDroInitVal	DRO initialization parameter structure	ParameterInitExec, OutputInitCtrl
DRIINIT	gstDriInitVal	DRI initialization parameter structure	ParameterInitExec, InputInitCtrl
unsigned short	gusToggleSW7Lv	Toggle switch 7 state 0: "L" level 1: "H" level	ToggleSWRead, InputInitCtrl
unsigned short	gusToggleSW6Lv	Toggle switch 6 state 0: "L" level 1: "H" level	ToggleSWRead, OutputInitCtrl
unsigned short	gusToggleSW5Lv	Toggle switch 5 state 0: "L" level 1: "H" level	ToggleSWRead, InputEnableCtrl
unsigned short	gusToggleSW4Lv	Toggle switch 4 state 0: "L" level 1: "H" level	ToggleSWRead, OutputEnableCtrl

5.6 Functions

Table 5.6 lists the functions.

Table 5.6 Functions

Function Name	Outline
ParameterInitExec	Make initial settings.
ToggleSWRead	Read toggle switch states.
OutputInitCtrl	Control data output initialization.
OutputEnableCtrl	Control data output processing start.
InputInitCtrl	Control initialization of data input processing.
InputEnableCtrl	Control data input processing start.
ProcessingStatus	Get processing status.
DroInit	Initialize DRO.
DroStart	Start DRO data output.
DroOutputStatus	Get DRO data output status.
DriInit	Initialize DRI.
DriStart	Start DRI data capture.
DriInputStatus	Get DRI data capture status.

5.7 Function Specifications

The following tables list the sample code function specifications.

ParameterInitExec

Outline	Make initial settings.
Headers	dro.h, dri.h, sh7450_iodefne_20100625.h, typedefine.h
Declaration	void ParameterInitExec(void)
Description	This function initializes the ports used by toggle switches S7 to S4, initializes the global variables, creates the output data, and the SHwyRAM area to which data will be captured is cleared to 0.
Arguments	None
Returned value	None
Remarks	

ToggleSWRead

Outline	Read toggle switch states.
Header	sh7450_iodefne_20100625.h
Declaration	void ToggleSWRead(void)
Description	This function reads the input levels of toggle switches S7 to S4 from the input ports and updates the variables indicating the states of toggle switches S7 to S4.
Arguments	None
Returned value	None
Remarks	

OutputInitCtrl

Outline	Control data output initialization.
Header	dro.h
Declaration	void OutputInitCtrl(void)
Description	<ul style="list-style-type: none"> • This function controls execution of function DroInit according to the value of the DRO initialization flag and the state of toggle switch S6. • After execution of function DroInit completes, this function sets the DRO initialization flag to “execution complete”.
Arguments	None
Returned value	None
Remarks	

OutputEnableCtrl

Outline	Control data output processing start.
Header	dro.h
Declaration	void OutputEnableCtrl(void)
Description	<ul style="list-style-type: none"> • This function controls execution of function DroStart according to the value of the DRO initialization flag, the DRO data output start flag, and the state of toggle switch S4. • After execution of function DroStart completes, this function sets the DRO data output start flag to “execution complete”.
Arguments	None
Returned value	None
Remarks	

InputInitCtrl

Outline	Control data input processing initialization.
Header	dri.h
Declaration	void InputInitCtrl(void)
Description	<ul style="list-style-type: none"> • This function controls execution of function DriInit according to the value of the DRI initialization flag and the state of toggle switch S7. • After execution of function DriInit completes, this function sets the DRI initialization flag to “execution complete”.
Arguments	None
Returned value	None
Remarks	

InputEnableCtrl

Outline	Control data input processing start.
Header	dri.h
Declaration	void InputEnableCtrl(void)
Description	<ul style="list-style-type: none"> • This function controls execution of function DriStart according to the value of the DRI initialization flag, the DRI data capture start flag, and the state of toggle switch S5. • After execution of function DriStart completes, this function sets the DRI data capture start flag to “execution complete”.
Arguments	None
Returned value	None
Remarks	

ProcessingStatus

Outline	Get processing status.
Headers	dro.h, dri.h, typedefine.h
Declaration	void ProcessingStatus (void)
Description	<ul style="list-style-type: none"> • This function executes functions DroOutputStatus and DrilnputStatus. • When processing completes, this function sets the processing status flag to “processing complete”.
Arguments	None
Returned value	None
Remarks	

DroInnit

Outline	Initialize DRO.
Headers	dro.h, sh7450_iodefne_20100625.h, typedefine.h
Declaration	void DroInnit(DROINIT* stDroInnitVal)
Description	<ul style="list-style-type: none"> • This function starts supply of the clock to the DRO. • This function initializes the ports used by the DRO and the DRO output control block.
Arguments	1st argument: stDroInnitVal: Pointer to the structure for storing the DRO initialization parameters
Returned value	None
Remarks	<ul style="list-style-type: none"> • In order to set the DRO address counter register (DROADRCT), this function clears bits 31 to 19, 1, and 0, to 0, in ulDstAddr, a member of structure stDroInnitVal. • ulSrcAddr, a member of structure stDroInnitVal, should be set to a multiple of 32.

DroStart

Outline	Start DRO data output.
Headers	dro.h, sh7450_iodefne_20100625.h
Declaration	void DroStart (void)
Description	Enables DRO output.
Arguments	None
Returned value	None
Remarks	

DroOutputStatus

Outline	Get DRO data output status.
Headers	dro.h, sh7450_iodefne_20100625.h, typedefine.h
Declaration	int DroOutputStatus(void)
Description	<ul style="list-style-type: none"> • When data output equal to the transfer count is completed, this function returns a value of DRO_OUTPUT_COMPLETION (1). • When data output is incomplete, this function returns a value of DRO_OUTPUT_INCOMPLETION (0).
Arguments	None
Returned value	<ul style="list-style-type: none"> • Data output complete: DRO_OUTPUT_COMPLETION (1) • Data output incomplete: DRO_OUTPUT_INCOMPLETION (0)
Remarks	

DriInit

Outline	Initialize DRI.
Headers	dri.h, sh7450_iodefines_20100625.h, typedefines.h
Declaration	void DriInit(DRIINIT* stDriInitVal)
Description	<ul style="list-style-type: none"> • This function starts supply of the clock to the DRI. • This function initializes the ports used by the DRI and the DRI control block.
Arguments	1st argument: stDriInitVal: Pointer to the structure for storing the DRI initialization parameters
Returned value	None
Remarks	<ul style="list-style-type: none"> • In order to set the DRI2 address counter 0 (DRI2ADR0CT) register, this function clears to 0 bits 31 to 19, 1, and 0 in ulDstAddr, a member of structure stDriInitVal. • ulNumOfData, a member of structure stDriInitVal, should be set to a multiple of 32.

DriStart

Outline	Start DRI data capture
Headers	dri.h, sh7450_iodefines_20100625.h, typedefines.h
Declaration	void DriStart(DRIINIT* stDriInitVal);
Description	Selects the event detection method for external signals input to the DRI.
Arguments	1st argument: stDriInitVal: Pointer to the structure for storing the DRI initialization parameters
Returned value	None
Remarks	

DriInputStatus

Outline	Get DRI data capture status
Headers	dri.h, sh7450_iodefines_20100625.h, typedefines.h
Declaration	int DriInputStatus (void)
Description	<ul style="list-style-type: none"> • When data capture equal to the event count is completed, this function returns a value of DRI_INPUT_COMPLETION (1). • When data capture is incomplete, this function returns a value of DRI_INPUT_INCOMPLETION (0).
Arguments	None
Returned value	<ul style="list-style-type: none"> • Data capture complete: DRI_INPUT_COMPLETION (1) • Data capture incomplete: DRI_INPUT_INCOMPLETION (0)
Remarks	

5.8 Flowcharts

5.8.1 main Processing

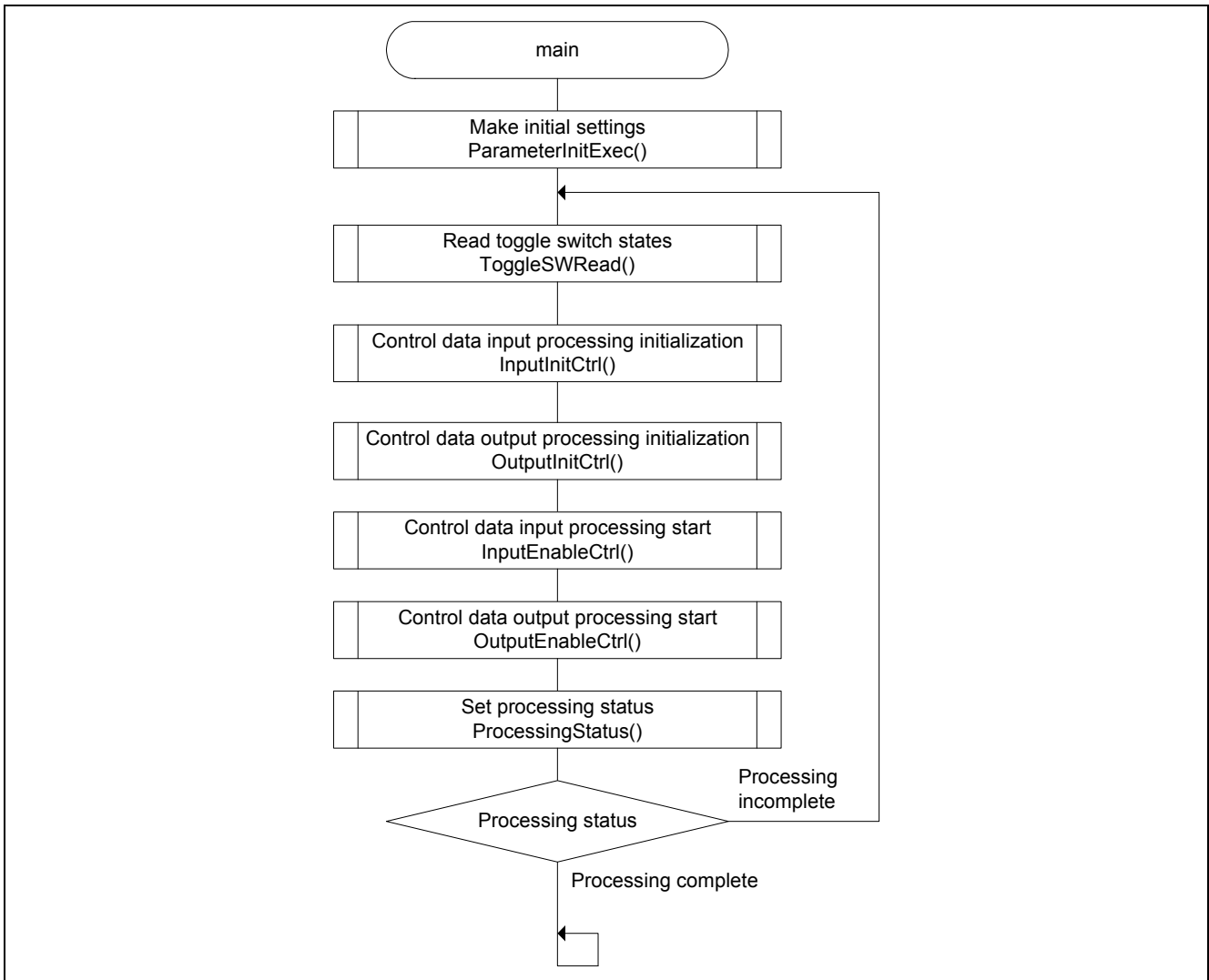


Figure 5.4 main Processing

5.8.2 ParameterInitExec Processing

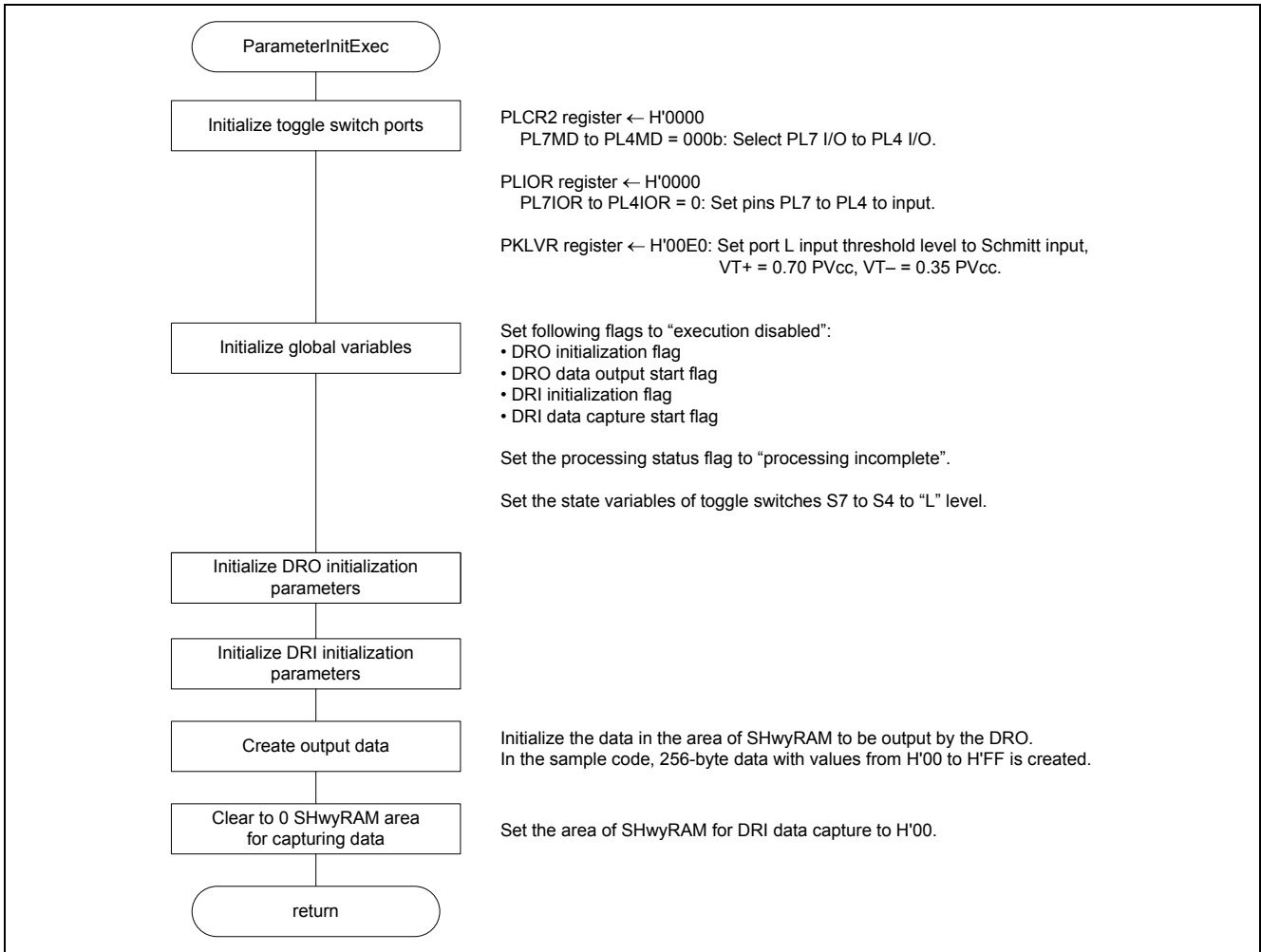


Figure 5.5 ParameterInitExec Processing

5.8.3 ToggleSWRead Processing

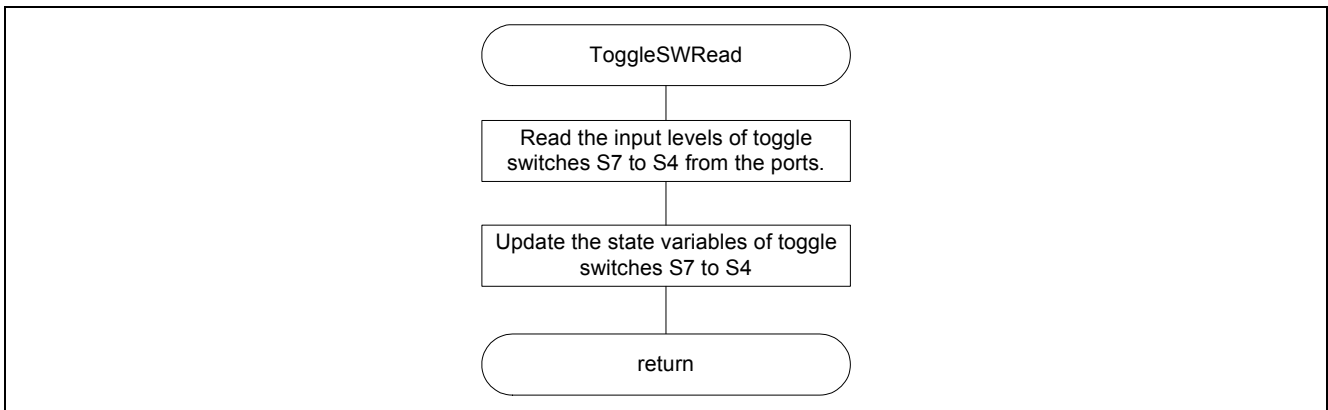


Figure 5.6 ToggleSWRead Processing

5.8.4 OutputInitCtrl Processing

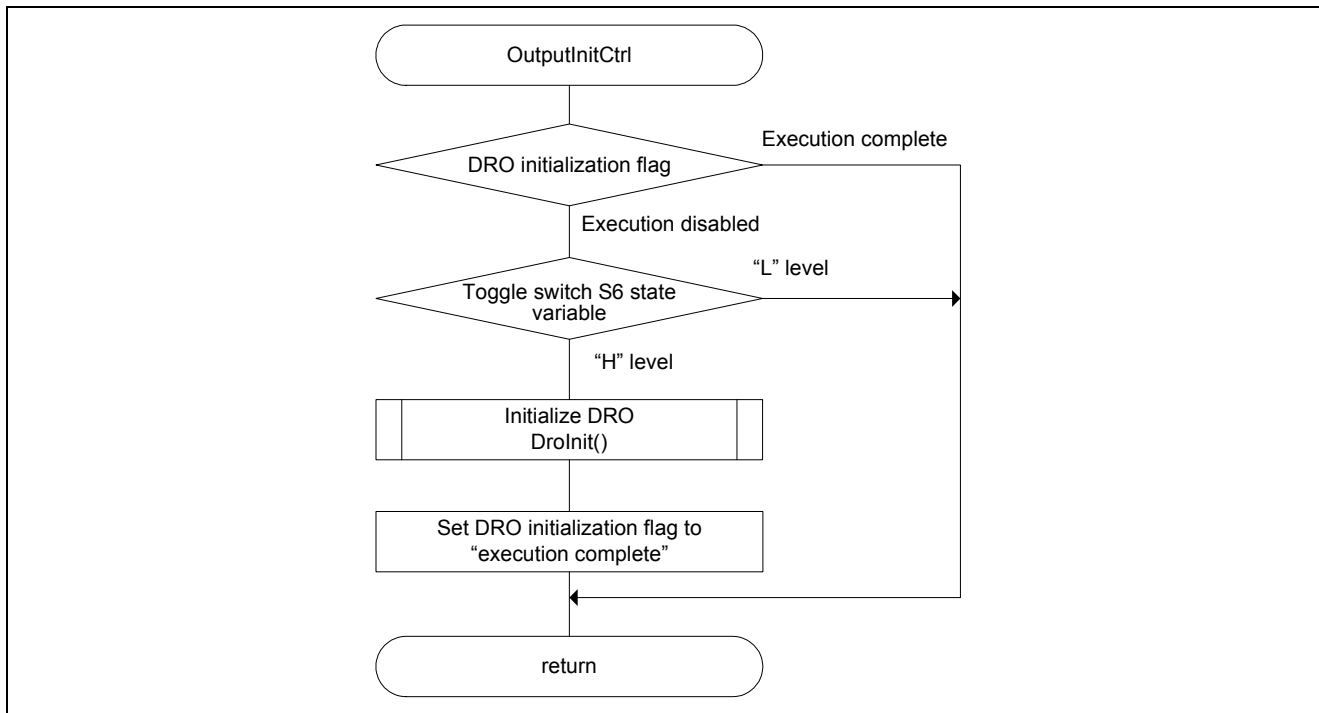


Figure 5.7 OutputInitCtrl Processing

5.8.5 OutputEnableCtrl Processing

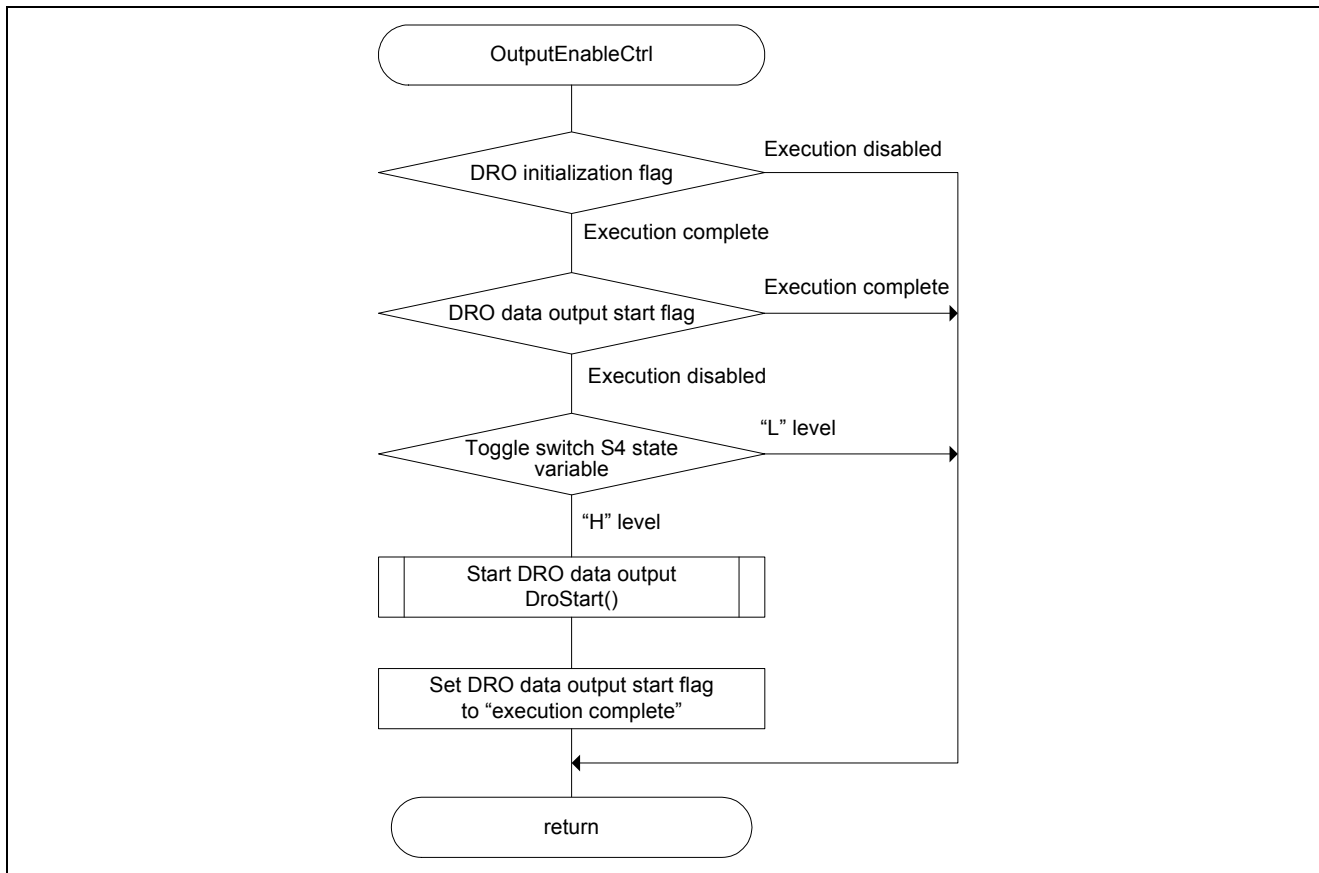


Figure 5.8 OutputEnableCtrl Processing

5.8.6 InputInitCtrl Processing

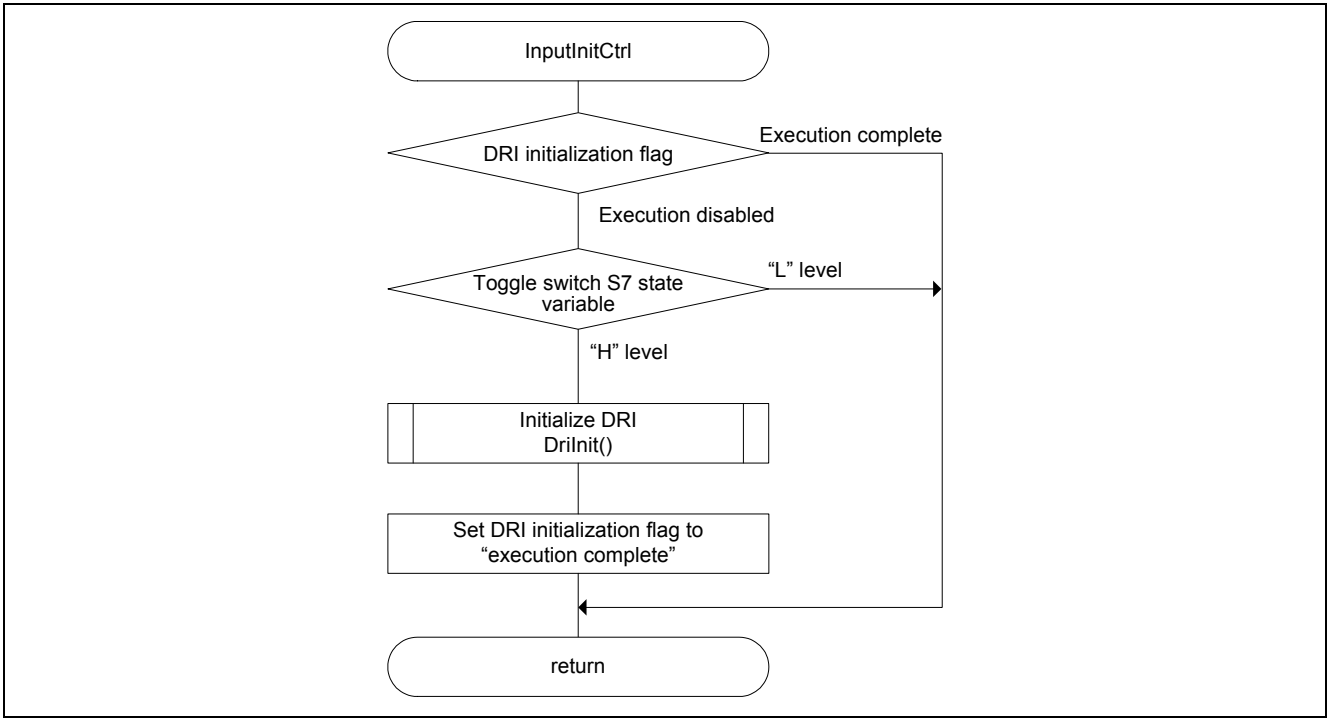


Figure 5.9 InputInitCtrl Processing

5.8.7 InputEnableCtrl Processing

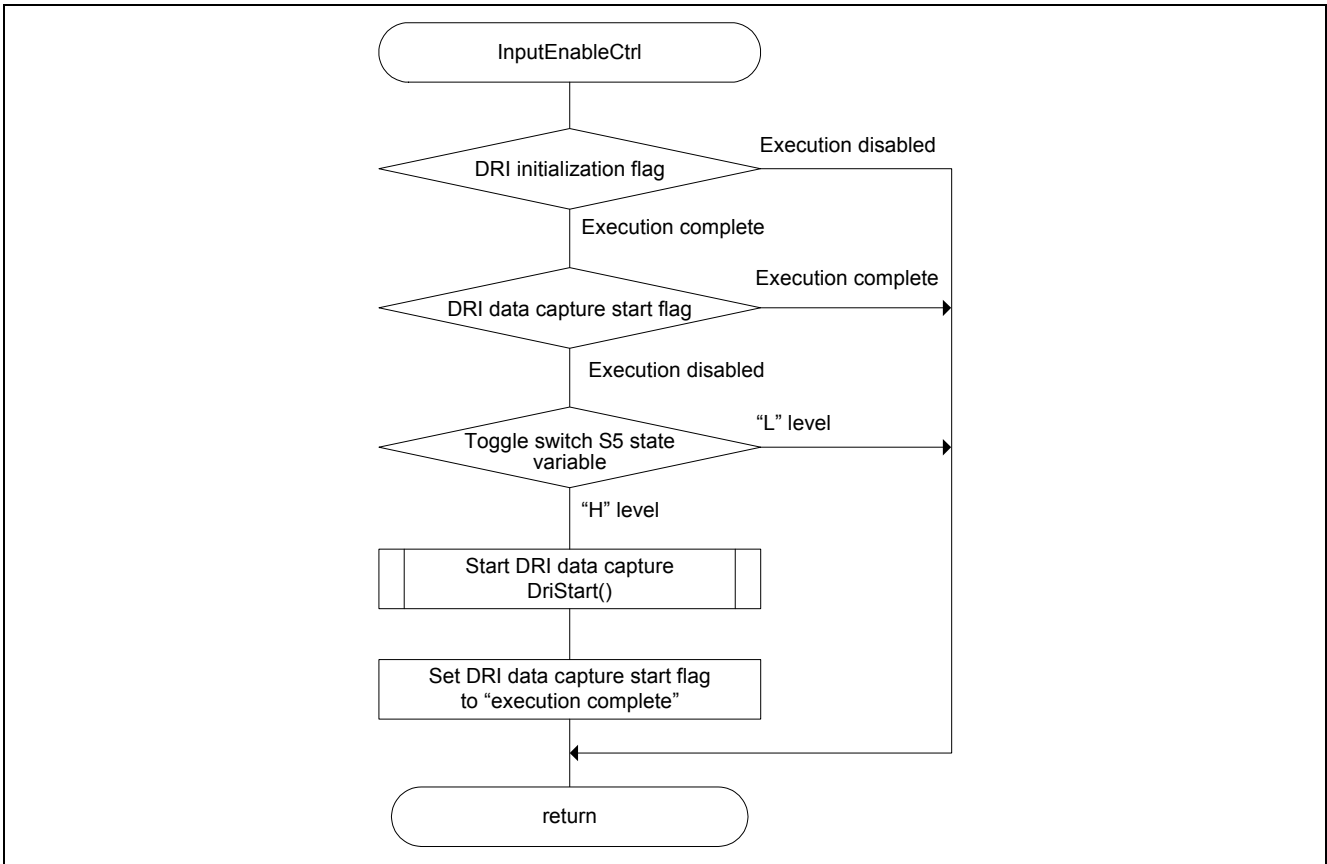


Figure 5.10 InputEnableCtrl Processing

5.8.8 ProcessingStatus Processing

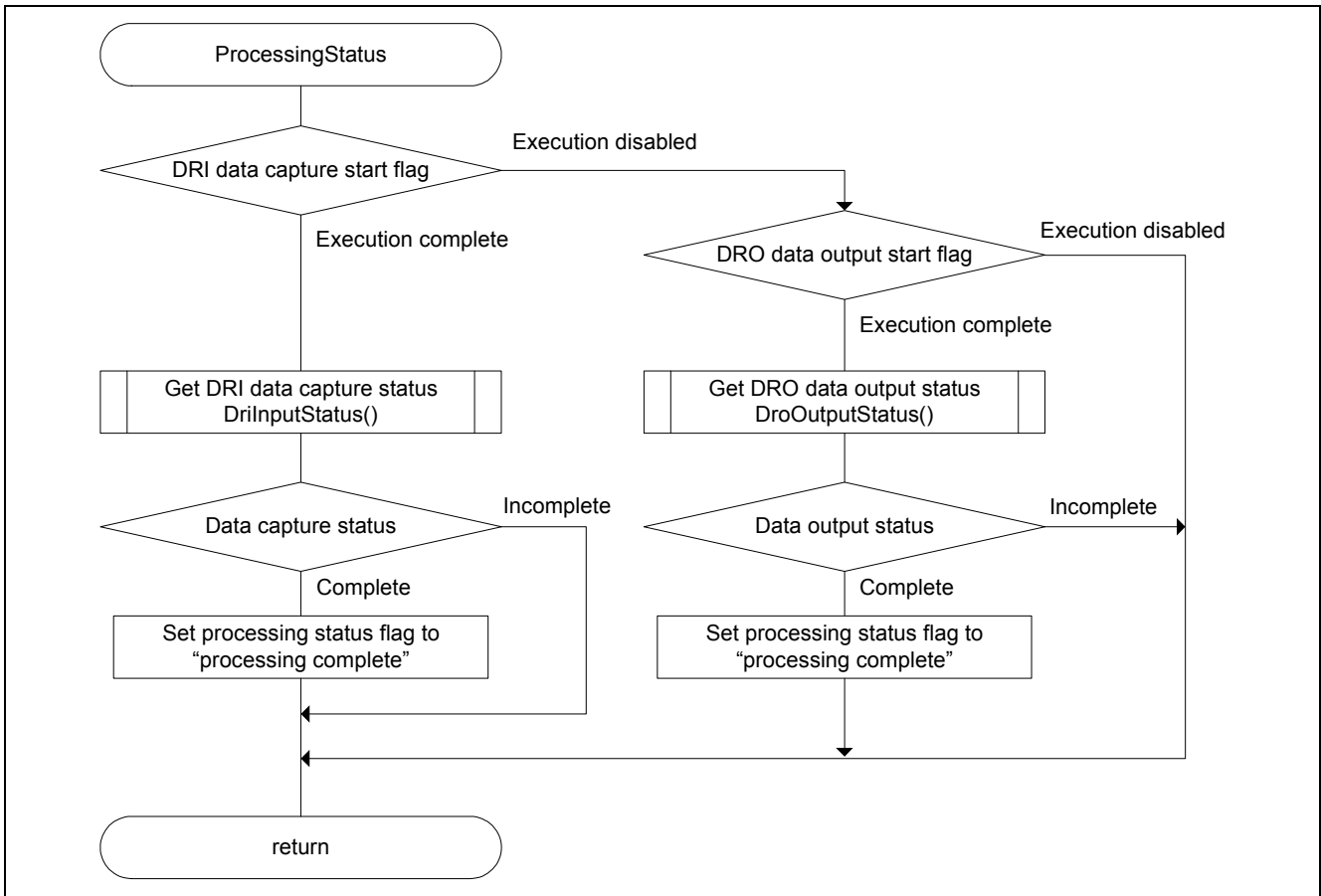


Figure 5.11 ProcessingStatus Processing

5.8.9 Drolnit Processing

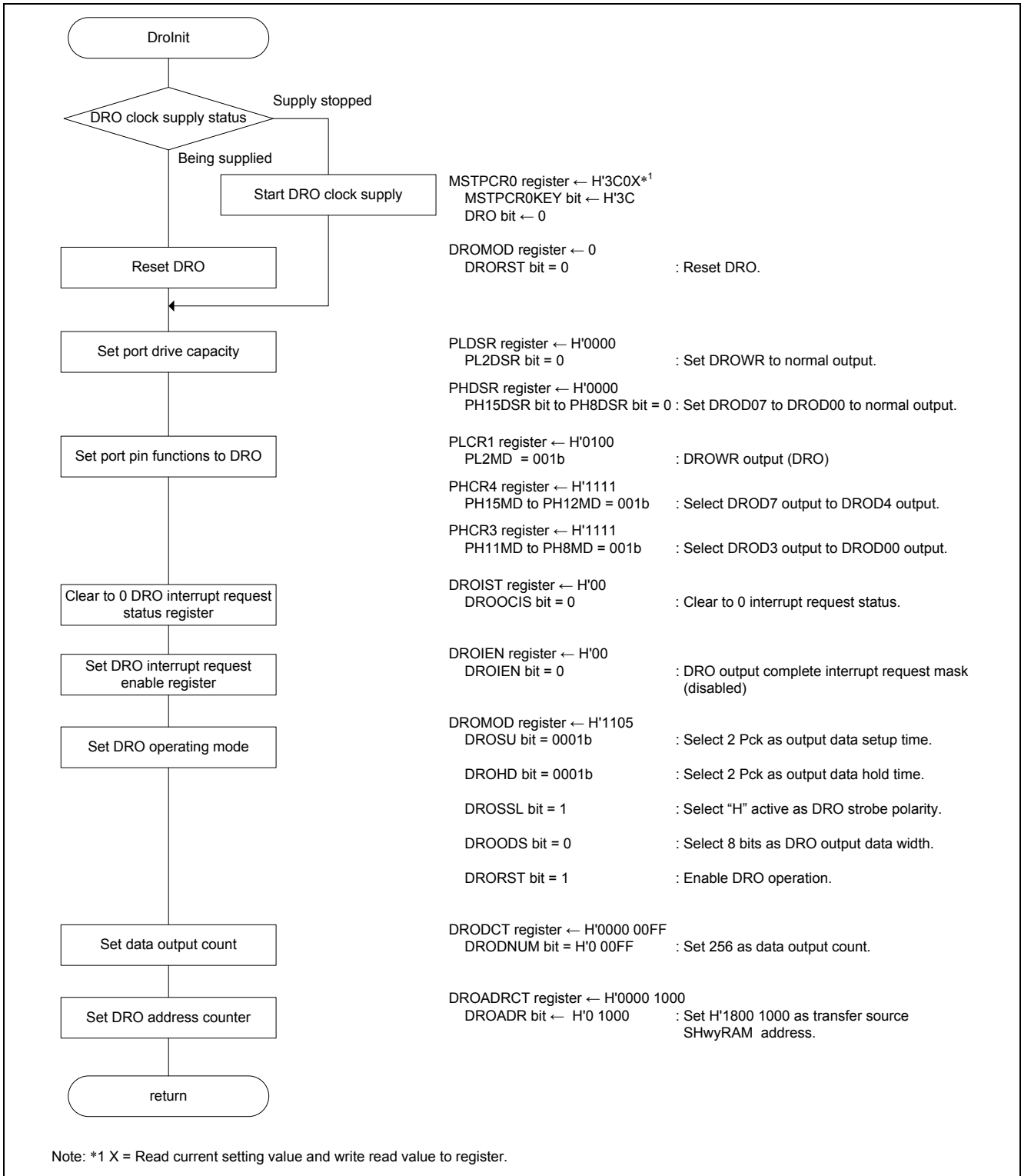


Figure 5.12 Drolnit Processing

5.8.10 DroStart Processing

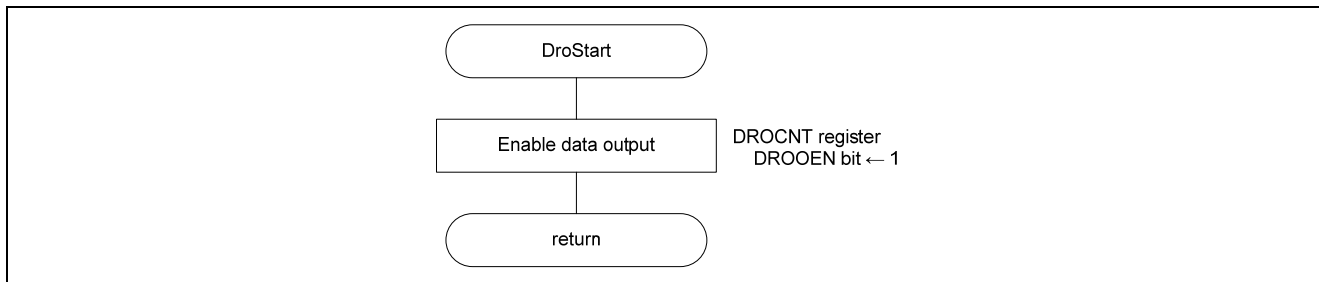


Figure 5.13 DroStart Processing

5.8.11 DroOutputStatus Processing

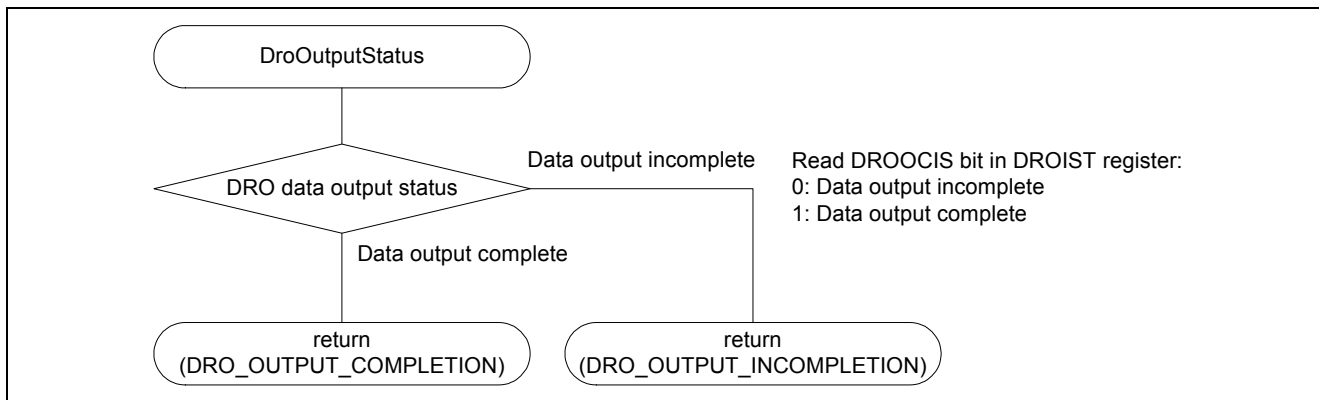


Figure 5.14 DroOutputStatus Processing

5.8.12 Drilnit Processing

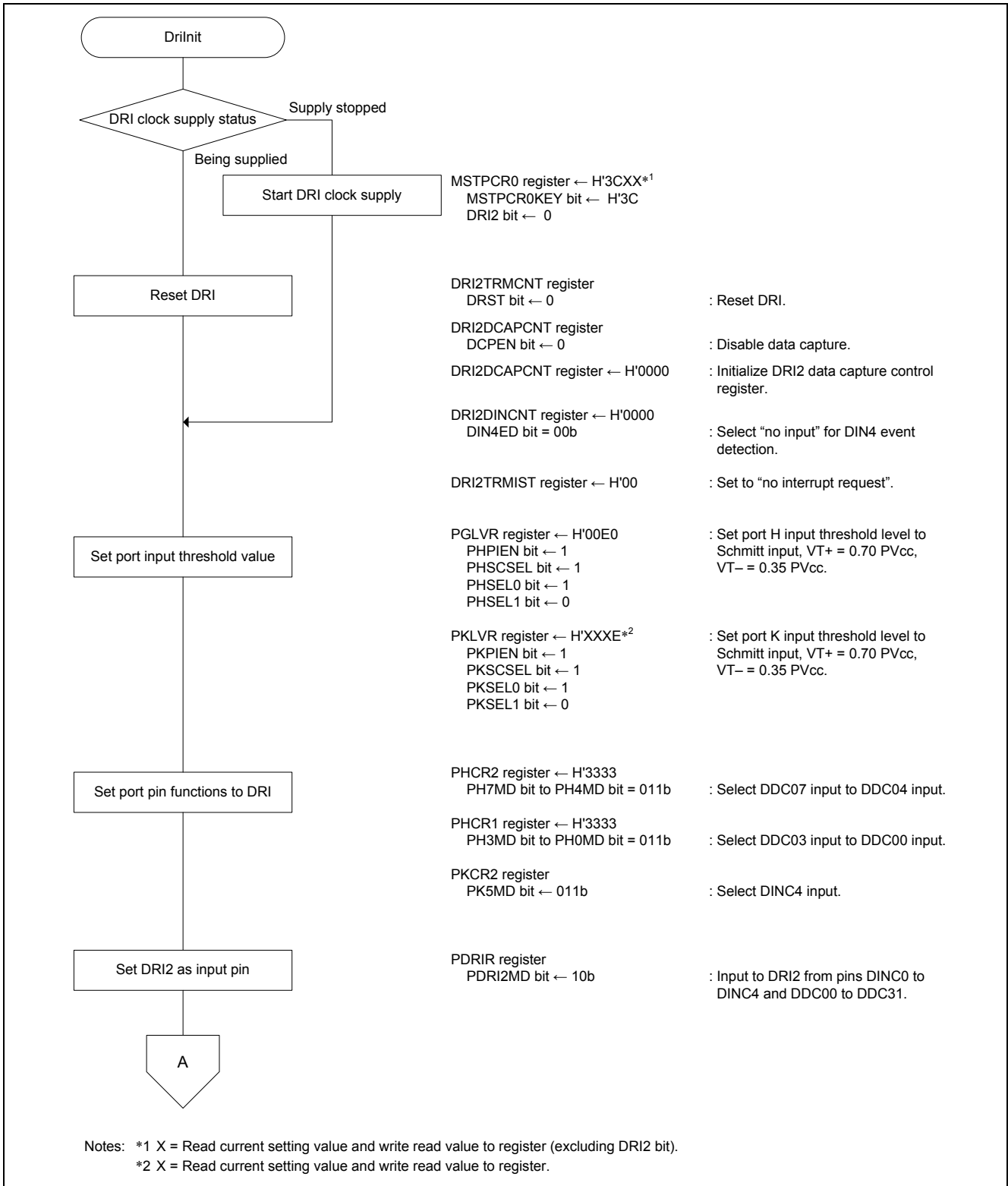


Figure 5.15 Drilnit Processing (1/2)

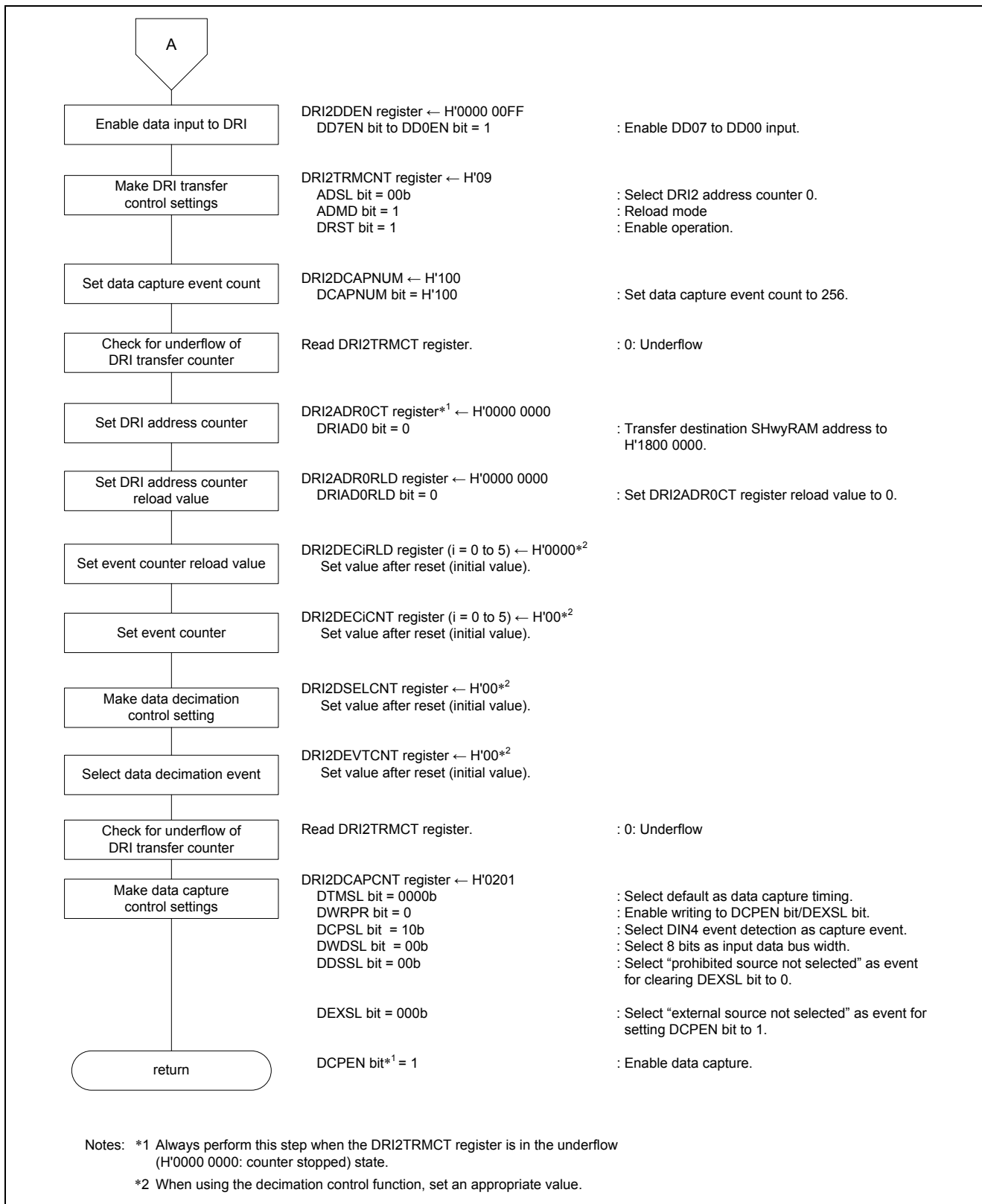


Figure 5.16 Drilnit Processing (2/2)

5.8.13 DriStart Processing

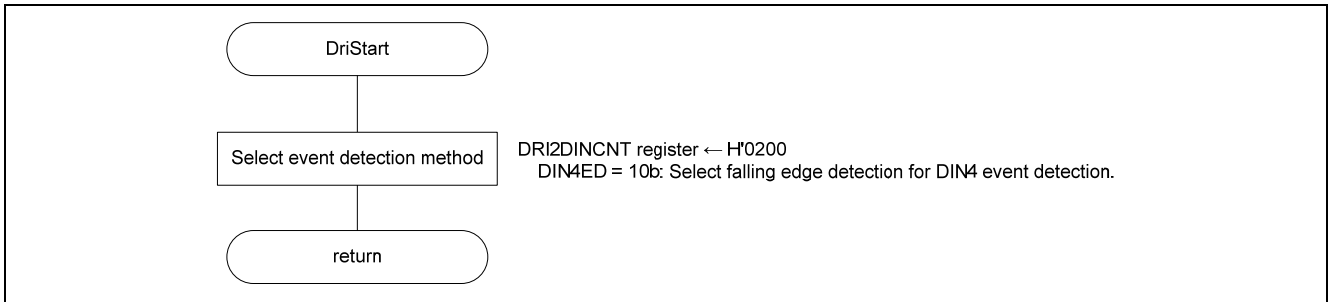


Figure 5.17 DriStart Processing

5.8.14 DriInputStatus Processing

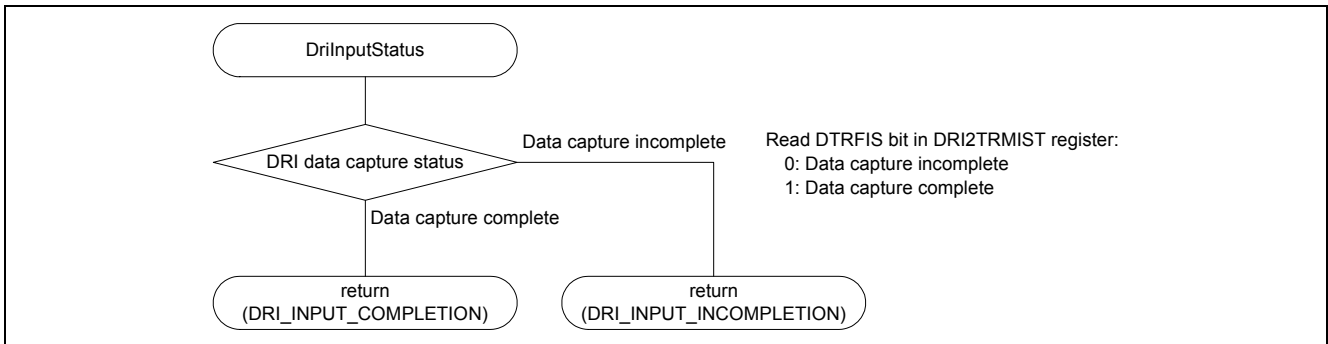


Figure 5.18 DriInputStatus Processing

6. Reference Documents

SH7450 Group, SH7451 Group User's Manual: Hardware, Rev.1.10 (R01UH0286EJ0110)
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	SH7450 Group, SH7451 Group Data Communication Using the DRO and DRI
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Rev.	Date	Description	
		Page	Summary
1.00	Nov. 2, 2011	—	First edition issued
1.01	Mar. 2, 2012	—	Template is changed

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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