# SH7262/SH7264 Group

## Video Display Controller 3 Video Recording Example

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### Summary

This application note describes the video recording example using the SH7262/SH7264 Microcomputers (MCUs) on-chip Video Display Controller 3 (VDC3).

### Target Device

SH7264 MCU.

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# 1. Introduction

## 1.1 Specifications

The SH7264 on-chip Video Display Controller 3 (VDC3) stores the input video in the BT.656 format in SDRAM.

## 1.2 Modules Used

- Video Display Controller 3 (VDC3)
- General-purpose I/O ports
- Interrupt Controller

## 1.3 Applicable Conditions

| | |
|---|---|
| MCU | SH7262/SH7264 |
| Operating Frequency | Internal clock: 144 MHz<br>Bus clock: 72 MHz<br>Peripheral clock: 36 MHz |
| Integrated Development Environment | Renesas Electronics Corporation<br>High-performance Embedded Workshop Ver.4.07.00 |
| C Compiler | Renesas Electronics SuperH RISC engine Family<br>C/C++ compiler package Ver.9.03 Release 00 |
| Compiler Options | Default setting in the High-performance Embedded Workshop<br>(-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0<br>-opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1) |

## 1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group SDRAM Interface Setting
- SH7262/SH7264 Group Video Display Controller 3 TFT-LCD Interfacing Example
- SH7262/SH7264 Group Video Display Controller 3 Video Display Example
- SH7262/SH7264 Group Video Display Controller 3 How to Use the α (Alpha) Blending Window Function

## 1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

# 2. Applications

This application note shows the pin connection example and configuration example to record the video by the VDC3.

## 2.1 VDC3 Operation

The VDC3 provides the video display function to display the video, and the video recording function to record the video. This application note describes the video recording function.

### 2.1.1 Overview

The VDC3 provides the following four functions. The function related to the video recording is the "video recording function". The video display function and video recording function cannot be used at the same time.

1. Video display function: Reduces the size of the input video, buffers the resultant video data in memory, and then displays the video on the panel
2. Video recording function: Stores a specified number of fields of the input video in SDRAM
3. Function for overlaying graphics images (two planes) on the input video
4. Function for outputting the control signals for the TFT-LCD panel

### 2.1.2 Features

The following table lists the VDC3 features.

**Table 1 VDC3 Features**

| Item | Description | Remarks |
|---|---|---|
| Operating frequency | Video input clock: 27 MHz<br>Panel clock: 4 to 36 MHz (depends on the panel specifications) | For video recording |
| Input video standard | 8-bit input compliant to the ITU-R BT.656 standard (27 MHz)<br>8-bit serial input compliant to the ITU-R BT.601 standard (27 MHz) | |
| Video recording function | Stores the video data in the RGB565 format at a rate of the 1/2 field (NTSC: 30 fps, PAL: 25 fps) | |
| Video scaling processing | Vertical: x 1/2, x 1/3, x 1/4<br>Horizontal: x 2/3, x 1/2, x 1/3x 1/4<br>Each scaled value can be further multiplied by 6/7 to support PAL. | |
| Interrupt output | Line interrupt output (this can be output on a desired line)<br>VSYNC cycle fluctuation detection signal for the BT.601, and BT.656<br>Field write completion signal<br>Overflow/underflow detection signal for the internal buffer | |
| Graphics images | Two planes (layers 1 and 2)<br>RGB565 progressive format<br>(α = none, R: 5 bits, G: 6 bits, B: 5 bits; 16 bits in total)<br>αRGB4444 progressive format<br>(α: 4 bits, R: 4 bits, G: 4 bits, B: 4 bits; 16 bits in total) | Other |
| Graphics functions | • α blending window function: Mixes the input video and layers 1 and 2 according to the transparency rate α in the specified region (fade-in and fade-out functions are available)<br>• Chroma-keying function: Mixes the images with applying the specified RGB color according to the transparency rate α.<br>• Dot α function: Mixes the images according to the transparency rate α when the target is a graphic image in α RGB4444 format.<br>• For each dot, the priority among the α values of the above functions is as follows:<br>• α blending window > chroma-keying > dot α | |
| Output video size | 640 pixels x 480 lines (VGA size)<br>480 pixels x 240 lines (WQVGA size)<br>320 pixels x 240 lines (QVGA , landscape-mode)<br>240 pixels x 320 lines (QVGA, portrait-mode)<br>Note: The maximum viewable area for the input image is 480 pixels x 240 lines (NTSC), and 480 pixels x 288 lines (PAL). | |
| Output video format | RGB565 progressive video output (16-bit parallel output) | |
| Sync signal output | Outputs the control signals for the TFT-LCD panel | |
| Video quality adjustment function | Contrast adjustment and brightness adjustment | |

### 2.1.3 I/O Pins

The following table shows the VDC3 I/O pins.

**Table 2 VDC3 I/O Pins**

| Symbol | I/O | Pin Name | Description | Remarks |
|---|---|---|---|---|
| DV_CLK | Input | Video input clock | BT.601, BT.656 clock input pin | For video recording |
| DV_VSYNC | Input | VSYNC input | BT.601 VSYNC signal input pin | |
| DV_HSYNC | Input | HSYNC input | BT.601 HSYNC signal input pin | |
| DV_DATA7 to 0 | Input | BT.601 or BT.656 input | BT.601 or BT.656 data signal input pins | |
| LCD_CLK | Output | Panel clock | Panel clock output pin | Other |
| LCD_EXTCLK | Input | Panel clock source | Panel clock source input pin | |
| LCD_VSYNC | Output | Panel VSYNC output | Vertical sync signal output pin for the panel | |
| LCD_HSYNC | Output | Panel HSYNC output | Horizontal sync signal output pin for the panel | |
| LCD_DE | Output | Panel data enable output | Data enable signal or data start position pulse signal output pin for the panel | |
| LCD_DATA15 to 0 | Output | Panel data output | Data output pins for the panel<br>MSB LSB MSB LSB<br>[15 : 11]: Red [4 : 0]<br>[10 : 5]: Green [5 : 0]<br>[4 : 0]: Blue [4 : 0] | |
| LCD_M_DISP | Output | Panel control signal | Alternating signal for the panel | |

### 2.1.4 Configuration

Figure 1 shows the VDC3 block diagram for the video displaying function. For details on the functional blocks for video recording, refer to Table 3.

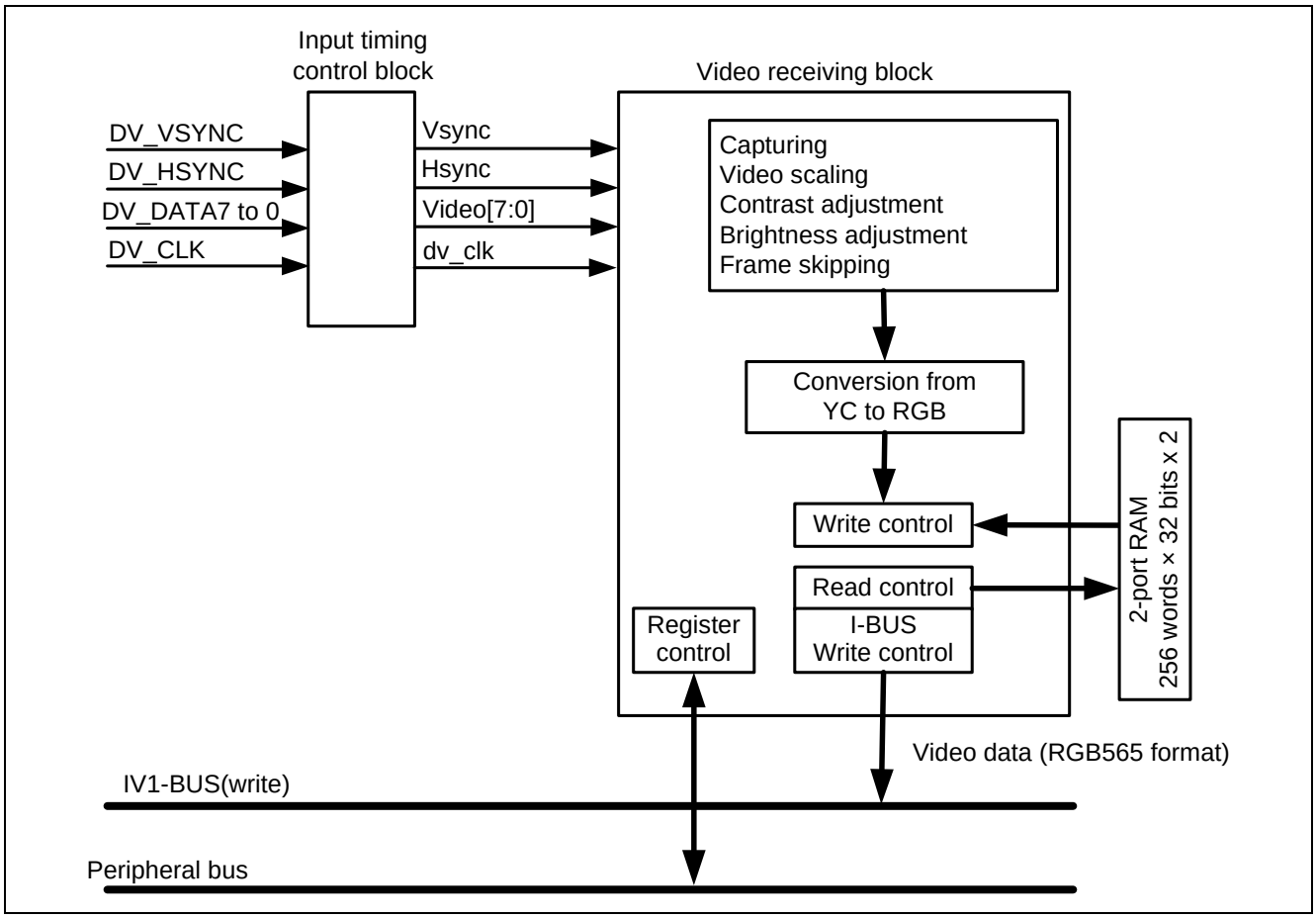



**Figure 1 VDC3 Block Diagram Related to the Video Recording Function**

**Table 3 VDC3 Functional Blocks**

| Block Name | Overview |
|---|---|
| Input timing control block | Controls the timing of the input sync signal clock rising or falling edge, and the sync polarity. It also controls the timing of the BT.601 and BT.656 video input signals clock rising or falling edge. |
| Video receiving block | (1) Captures the input video, scales, adjusts the contrast, and the brightness.<br>(2) Converts the YC format to the RGB565 format, and stores the data via the IV1-BUS.<br>(3) Skips the field, and stores the data in the RGB565 format via the IV1-BUS. |

### 2.1.5 Input Signals

The VDC3 has two options for the input video formats; BT.601 input or BT.656 input. This section describes the VDC3 input video formats in detail.

In addition, the VDC3 supports 525 lines (NTSC) and 625 lines (PAL) as the number of lines for the input video. This application is an example of 525 lines (NTSC).

(1) BT.601 Input

BT.601 is a standard for the NTSC and PAL, the analog television system, to specify the conversion and sampling frequency to digitize the analog video signal. The table below lists an overview of the BT.601. Refer to BT.601 specifications for detail.

**Table 4 BT.601 Overview (For NTSC)**

| Item | Description | |
|---|---|---|
| Scan Lines | 525 (2:1 interlace) | |
| Frame Rate | 60 fps | |
| Aspect Ratio | 4:3 or 16:9 | |
| Sample Structures | 4:2:2 | 4:4:4 |
| Color Format | Y, Cr, Cb | Y, Cr, Cb or R, G, B |
| Number of Samples per Total Line | 858 (Y), 429 (Cr, Cb) | 858 |
| Sampling Frequency | 13.5 MHz (Y), 6.75 MHz (Cr, Cb) | 13.5 MHz |
| Form of Coding | 8 or 10 bits/sample | |
| Number of Samples per Digital Active Line | 720 (Y), 360 (Cr, Cb) | 720 |
| Range of Data (8-bit coding) | 16 to 235 (Y), 16 to 240 (Cr, Cb) | 16 to 240 |

When selecting the BT.601 input, use DV_DATA7 to DV_DATA0 pins, DV_VSYNC pin, DV_HSYNC pin, and DV_CLK pin as the video input pins. Input the data signal to DV_DATA7 to DV_DATA0 pins, the vertical sync signal in DV_VSYNC pin, and the horizontal sync signal in DV_HSYNC pin.

Figure 2 shows the timing to capture video in the BT.601 input. Use the VIDEO_VSTART register to set the interval between the DV_VSYNC signal and the valid data area. For setting the interval between the DV_HSYNC signal and the valid data area, use the VIDEO_HSTART register. The polarity of the DV_VSYNC and DV_HSYNC signals can be changed by the VIDEO_TIM_CNT register.

As the input video is interlaced 2:1, Field 1 (TOP) and Field 2 (BOTTOM) of the data must be recognized. The VDC3 recognizes them by the value set in the FIELD_SKEW [9:0] bits in the VIDEO_TIM_CNT register. Figure 3 shows how to recognize fields in the BT.601. The data format for the input video is YC422. Figure 4 shows the data input format.

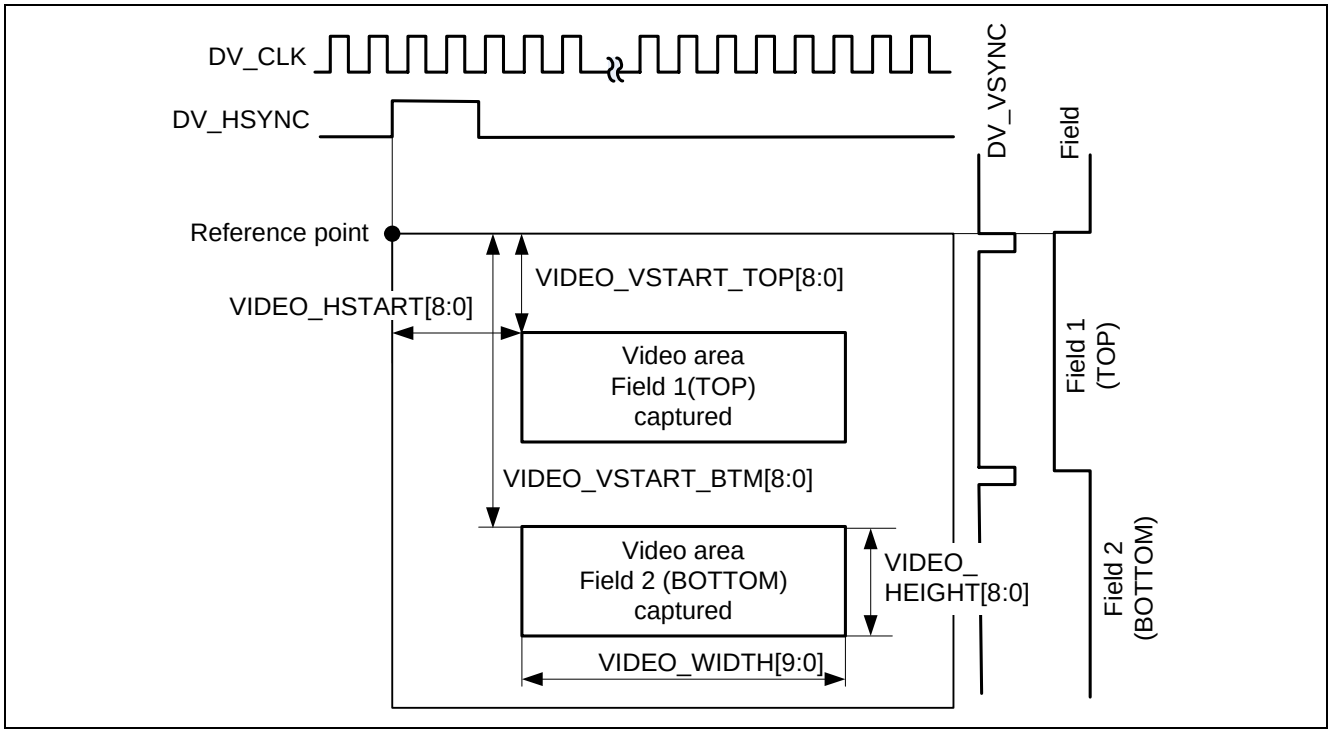



**Figure 2 Capture Timing in the BT.601 Input**

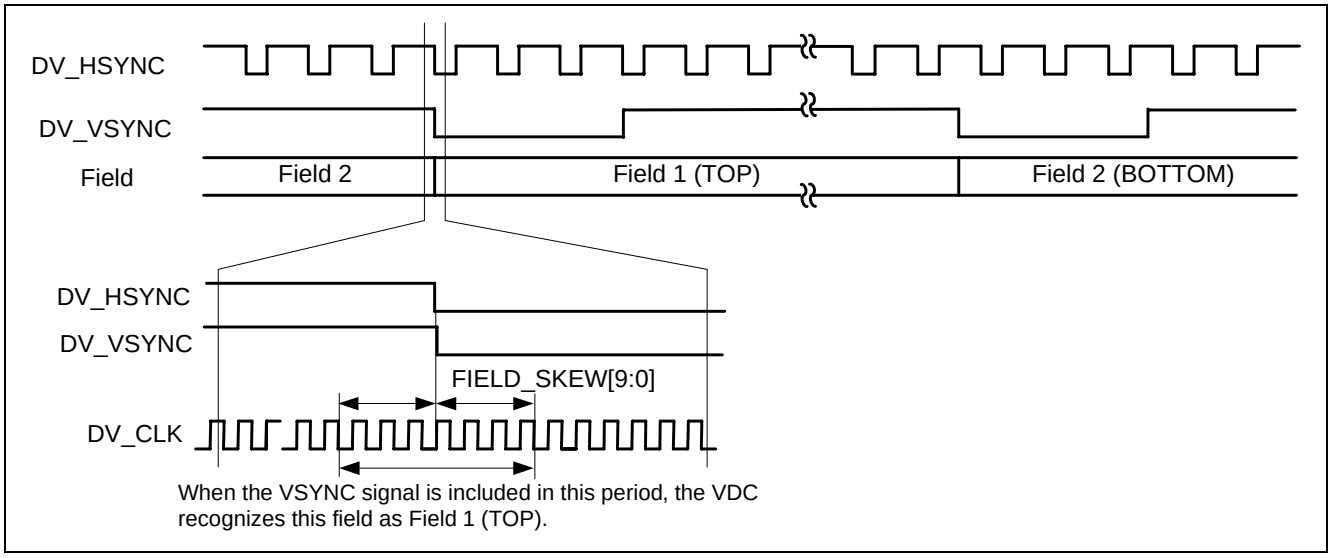



**Figure 3 How to Recognize the Fields in BT.601**

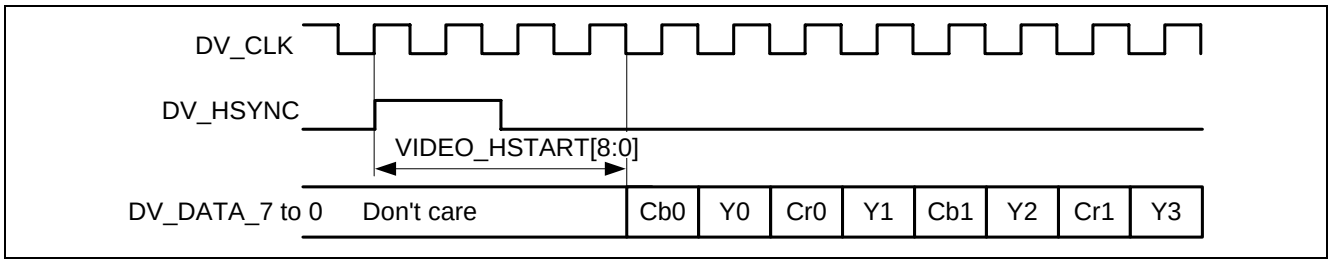



**Figure 4 Data Input Format for BT.601 input**

(2) BT.656 Input

BT.656 is a standard to specify the data structure of the digital video signals, which is defined in the BT.601. The structure of the data signals and the reference codes are specified in the BT.656. Replace the data output in the blanking interval with the reference codes to retrieve the Vsync and Hsync signals timing, and the field information. The following table lists the function of each bit in the reference codes.

**Table 5 Reference Codes (For 8-bit data)**

| Bit No. | The First Byte (H'FF) | The Second Byte (H'00) | The Third Byte (H'00) | The Fourth Byte (H'XX) |
|---|---|---|---|---|
| 7 | 1 | 0 | 0 | Fixed to 1 |
| 6 | | | | 0: field 1, 1: field 2 |
| 5 | | | | 1 during the vertical blanking interval, other, 0 |
| 4 | | | | 0: SAV (Start of Active Video)<br>1: EAV (End of Active Video) |
| 3 | | | | Protection bit (note) |
| 2 | | | | Protection bit (note) |
| 1 | | | | Protection bit (note) |
| 0 | | | | Protection bit (note) |

Note: Specific values for bits 6 to 4 are specified in BT.656.

When selecting the BT.656 input, use DV_DATA7 to DV_DATA0 pins only. As the vertical or horizontal sync information is retrieved by the reference code that is embedded in the data signal, input the data signals compliant to the BT.656.

The following figure shows the timing to capture video in the BT.656 input and the input data format.

| | | 1H cycle | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | EAV | | | | H blank | SAV | | | | Valid area | | | | | | |
| | | 1 | 2 | 3 | 4 | | 273 | 274 | 275 | 276 | 277 | 278 | 279 | 280 | | | 1716 |
| Field 2 BOTTOM | 1 | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | Blanking data area | | | | | | |
| | 2 | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | | | | | | | |
| | 3 | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | | | | | | | |
| Field 1 TOP | 4 | FF | 00 | 00 | B6 | | FF | 00 | 00 | AB | Blanking data area | | | | | | |
| | | FF | 00 | 00 | B6 | | FF | 00 | 00 | AB | | | | | | | |
| | 19 | FF | 00 | 00 | B6 | | FF | 00 | 00 | AB | | | | | | | |
| | 20 | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | Cb0 | Y0 | Cr0 | Y1 | | Cb359 Y718 Cr359 Y719 | |
| | | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | Valid pixel data area | | | | | | |
| | | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | | | | | | | |
| | | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | | | | | | | |
| | | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | | | | | | | |
| | 263 | FF | 00 | 00 | 9D | | FF | 00 | 00 | 80 | | | | | | | |
| | 264 | FF | 00 | 00 | B6 | | FF | 00 | 00 | AB | Blanking data area | | | | | | |
| | 265 | FF | 00 | 00 | B6 | | FF | 00 | 00 | AB | | | | | | | |
| Field 2 BOTTOM | 266 | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | Blanking data area | | | | | | |
| | | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | | | | | | | |
| | 282 | FF | 00 | 00 | F1 | | FF | 00 | 00 | EC | | | | | | | |
| | 283 | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | Cb0 | Y0 | Cr0 | Y1 | | Cb359 Y718 Cr359 Y719 | |
| | | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | Valid pixel data area | | | | | | |
| | | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | | | | | | | |
| | | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | | | | | | | |
| | | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | | | | | | | |
| | 525 | FF | 00 | 00 | DA | | FF | 00 | 00 | C7 | | | | | | | |

**Figure 5 Capture Timing in the BT.656 Input and the Data Input Format (For NTSC)**

### 2.1.6 Video Recording Image

The figure below shows the video recording image. The VDC3 captures only the TOP field of the input signal. Then, it scales down the captured video, adjusts the contrast and the brightness. Finally, it stores the video in the RGB565 format on internal RAM.

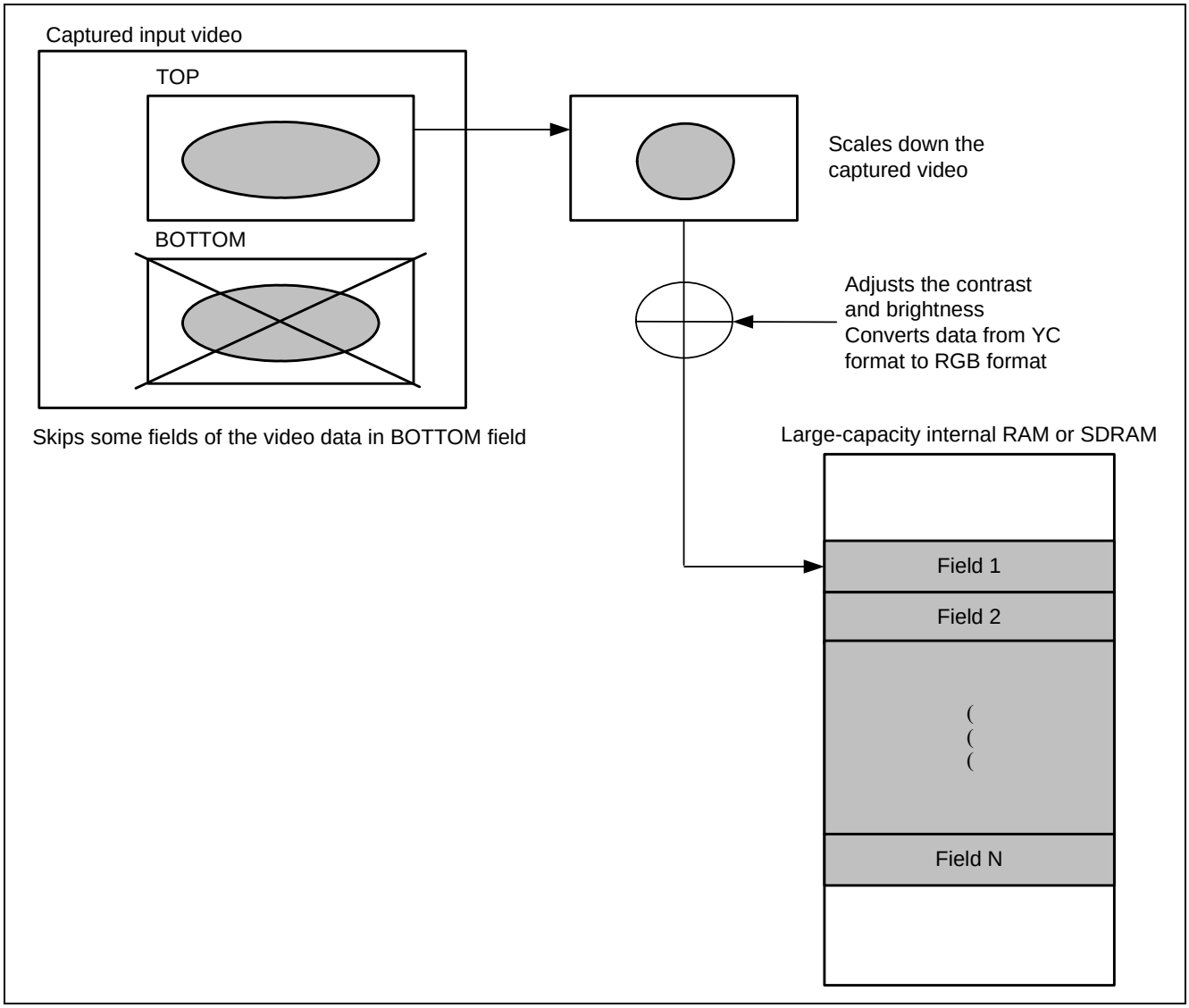



**Figure 6 Video Recording Image**

## 2.2 Video Recording Circuit Diagram

The figure below shows an example of the circuit diagram to record video. Use the digital video decoder to convert the video signal from analog to digital, and then input the video signal to the VDC3 through the DV_CLK, DV_VSYNC, DV_HSYNC, and DV_DATA7 to 0 pins. For interfacing SDRAM, refer to the application note "SH7262/SH7264 Group SDRAM Interface Setting".

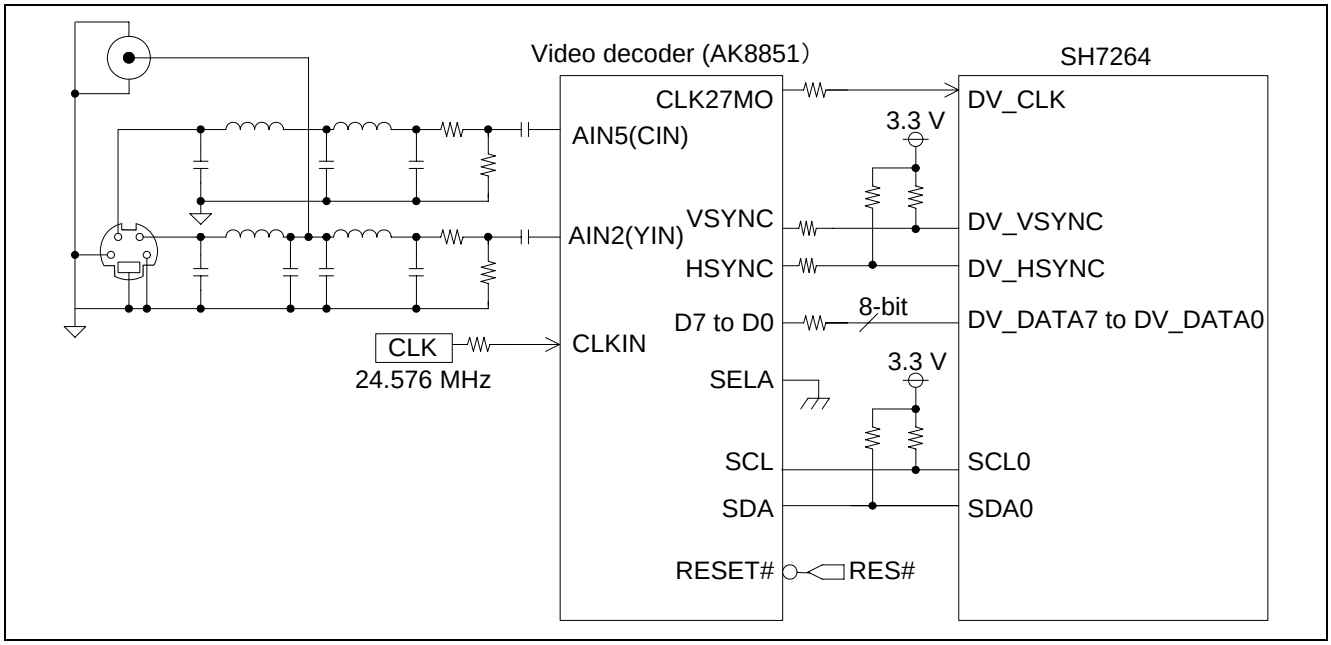



**Figure 7 Circuit Diagram**

## 2.3 Sample Program Specifications

This section describes the specifications of the sample program and shows the flow charts of each processing.

### 2.3.1 Specifications

- Stores the input video in the BT.656 format on SDRAM in the RGB565 format
- Scales down the video to 1/2 in both horizontal and vertical directions
- Stores 30 fields of video

### 2.3.2 Main Flow Chart of the Sample Program

Figure 8 shows the main flow chart of the sample program. The sample program executes a series of the processing as shown in Figure 9 to Figure 12 to store the input video on SDRAM.

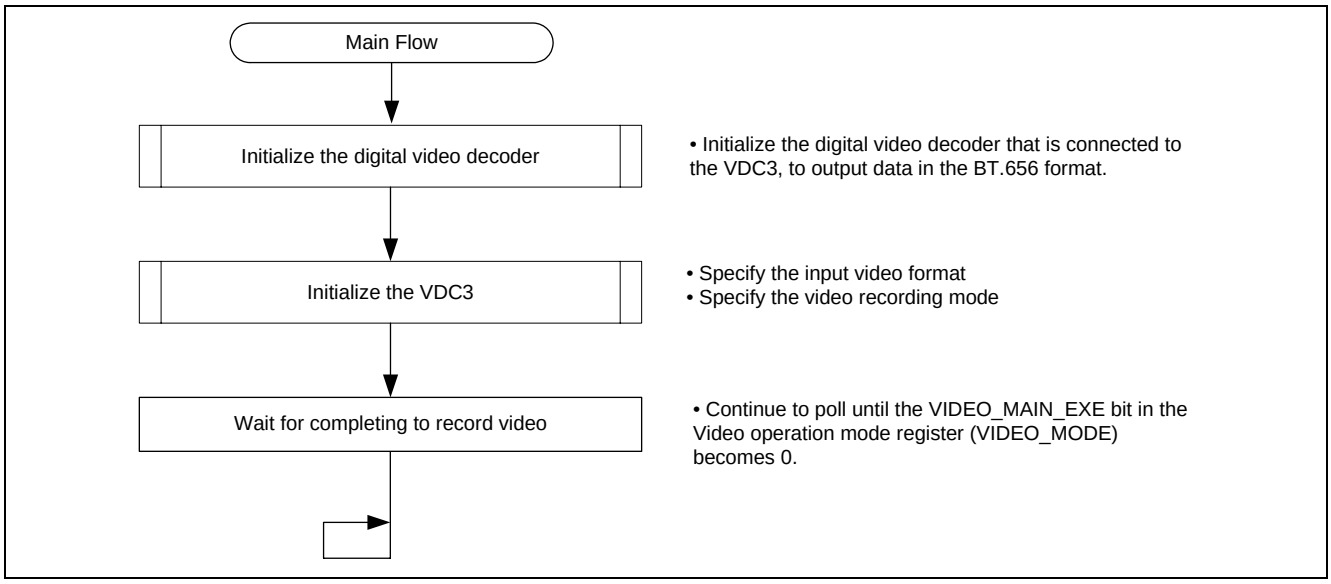



**Figure 8 Sample Program Main Flow Chart**

### 2.3.3 Flow Chart of Specifying Input Video Format

The figure below shows an example of specifying the input video format. The BT.656 input is specified in this application.

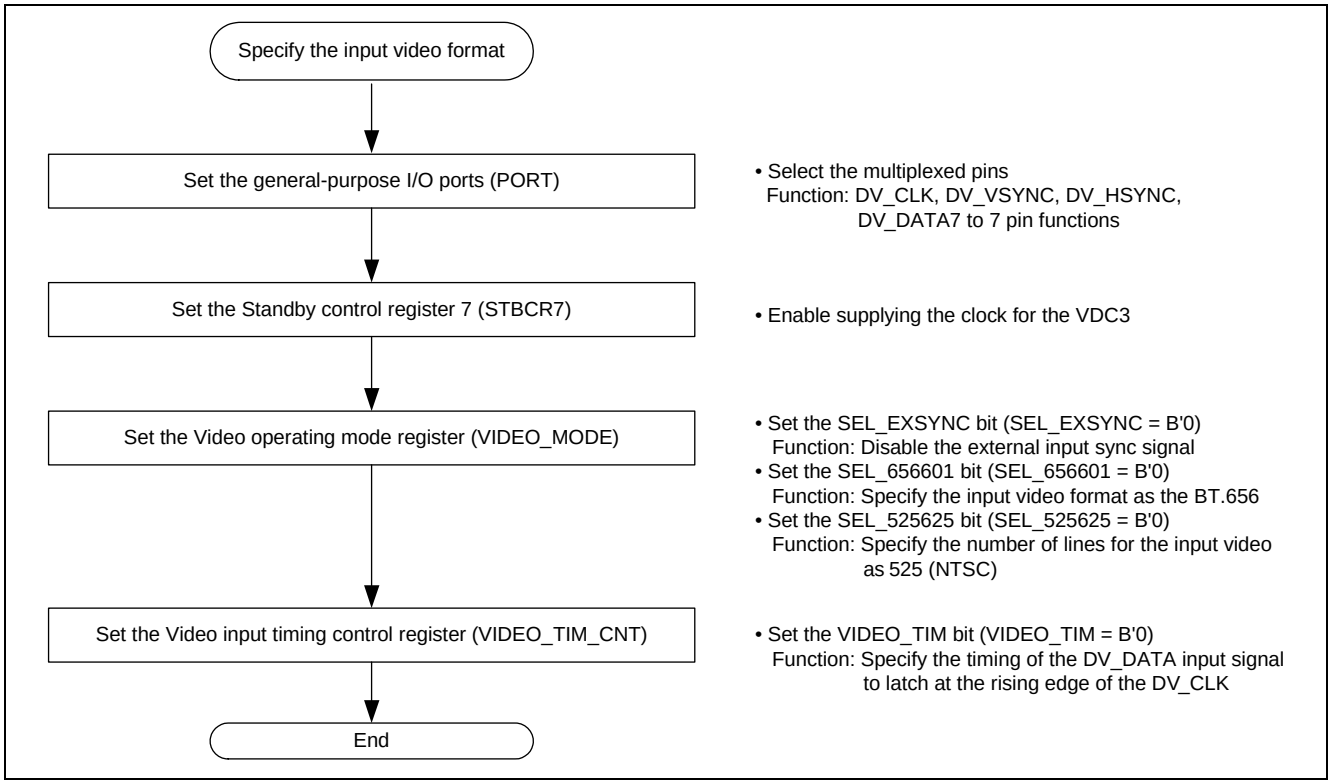
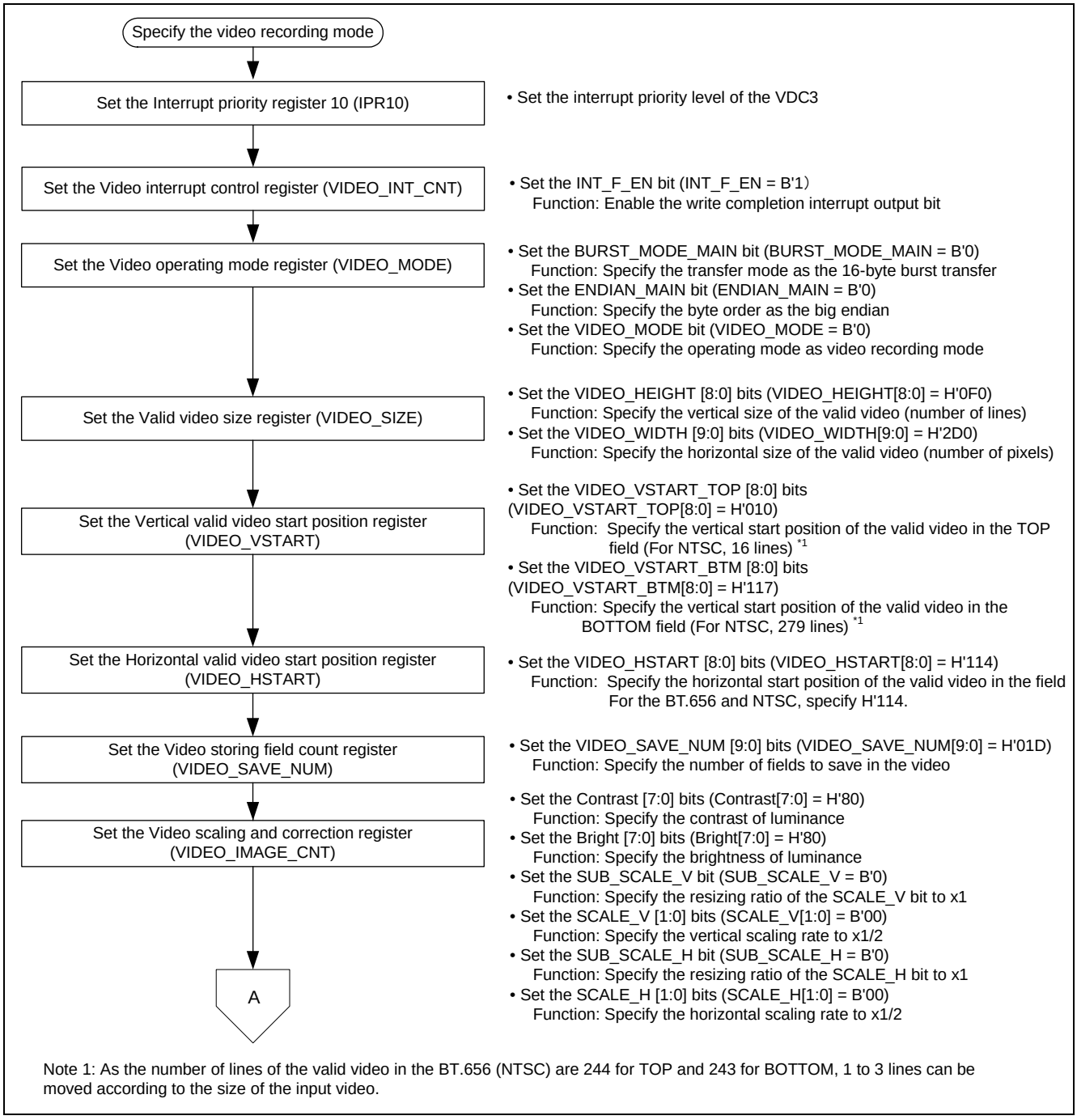



**Figure 9 Flow Chart of Specifying the Input Video Format**

### 2.3.4 Flow Chart of Specifying the Video Recording Mode

Figure 10 and Figure 11 show examples of specifying the video recording mode. This application scales down the captured input video at 1/2 both in the vertical and horizontal directions, and then stores the scaled video on SDRAM. The number of fields to store is 30.




Note 1: As the number of lines of the valid video in the BT.656 (NTSC) are 244 for TOP and 243 for BOTTOM, 1 to 3 lines can be moved according to the size of the input video.

**Figure 10 Setting Example of the Video Recording Mode (1/2)**

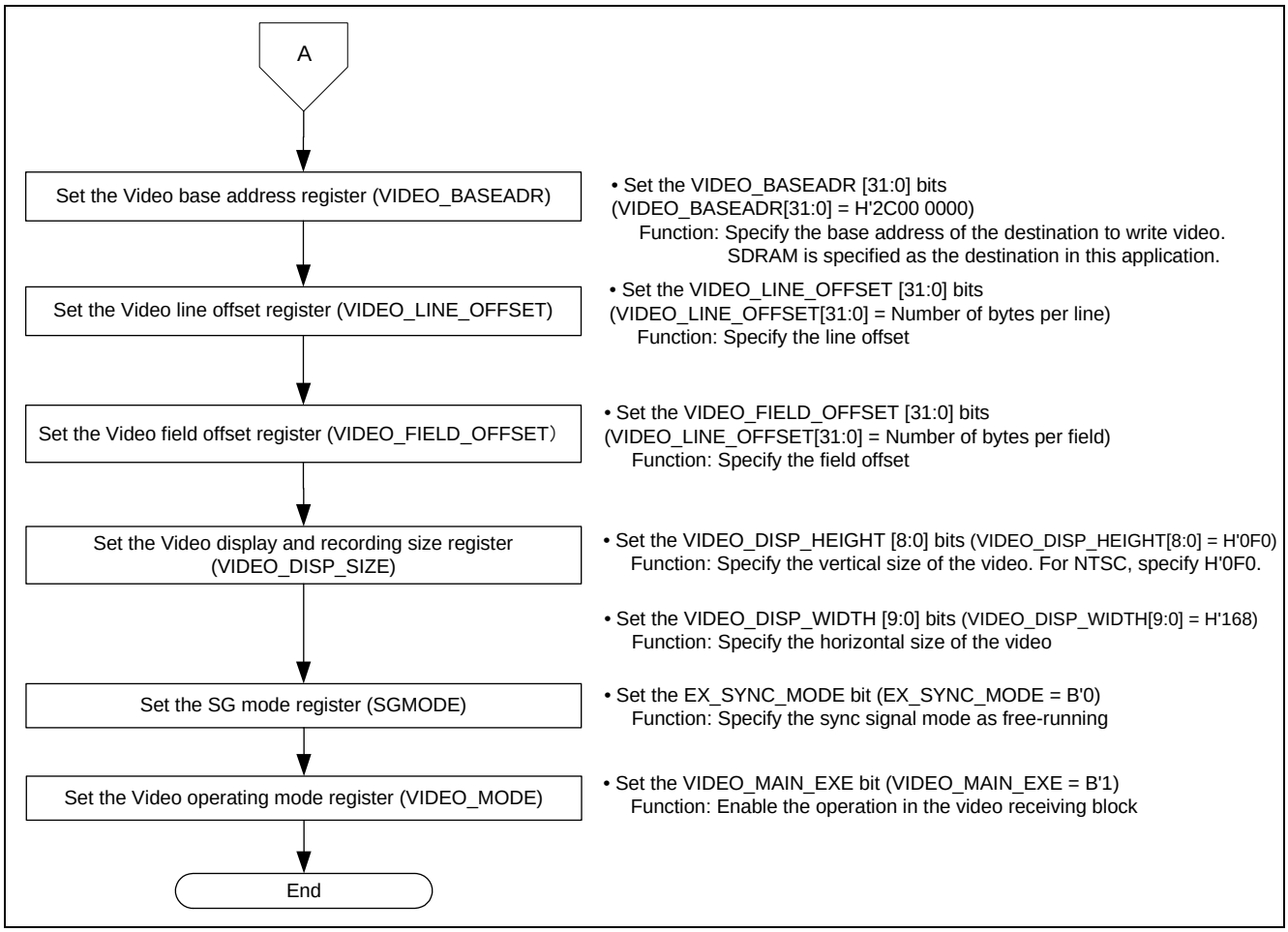



**Figure 11 Setting Example of the Video Recording Mode (2/2)**

### 2.3.5 Flow Chart of Interrupts

The figure below shows the flow chart of interrupts when writing one field of video is complete. The number of fields recorded is counted at every interrupt in this application. When the specified number of fields of recording is complete, it stops recording video.

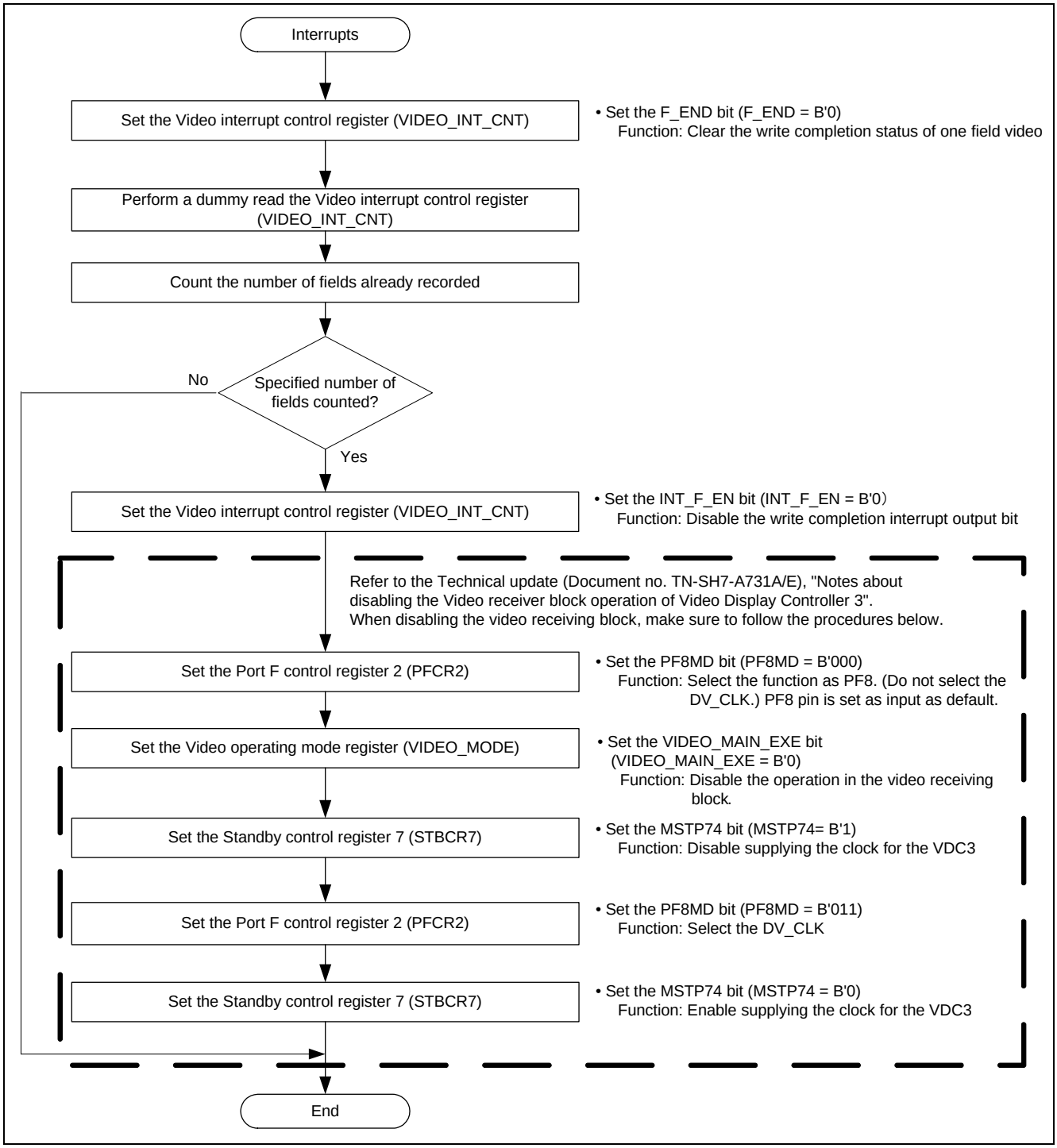



**Figure 12 Flow Chart of Interrupt (One Field of Video Writing is Complete)**

# 3. Sample Program Listing

## 3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

## 3.2 Sample Program Listing "main.c" (1/2)

```
1       /*********************************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Electronics Corporation and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Electronics Corporation and is protected under
8       *   all applicable laws, including copyright laws.
9       *
10      *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11      *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12      *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14      *   DISCLAIMED.
15      *
16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17      *   ELECTRONICS CORPORATION NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18      *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19      *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
20      *   AFFILIATES HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
21      *
22      *   Renesas reserves the right, without notice, to make changes to this
23      *   software and to discontinue the availability of this software.
24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      *********************************************************************************/
28      /* Copyright (C) 2009(2010,2011) Renesas Electronics Corporation. All Rights Reserved.*/
29      /*********************************************************************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : VDC3 Video recording example
33      *   Version     : 2.00.00
34      *   Device      : SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                               (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40      *   Description :
41      *********************************************************************************
42      *   History     : Jan.15,2009 Ver.1.00.00
43      *               : Jun.29,2009 Ver.1.01.00
44      *               : Feb.28,2011 Ver.2.00.00
45      *********************************************************************************/
46
47
```

## 3.3 Sample Program Listing "main.c" (2/2)

```
48    /***********************************************************************************
49    Includes  <System Includes> , "Project Includes"
50    ***********************************************************************************/
51    #include <stdio.h>
52    #include "iodefine.h"
53    #include "io_vdc3_video_rec.h"
54
55    /***********************************************************************************
56    Exported global variables and functions (to be accessed by other files)
57    ***********************************************************************************/
58    /* ==== Global functions ==== */
59    void main(void);
60
61    /***********************************************************************************
62     * ID           :
63     * Outline      : Video recording main
64     * Include      :
65     * Declaration  : void main(void);
66     * Description  : Records the video
67     * Argument     : void
68     * Return Value : void
69     ***********************************************************************************/
70    void main(void)
71    {
72      /* ==== Initializes the digital video decoder ==== */
73      init_video_decoder();
74
75      /* ==== Initializes the VDC3 ==== */
76      io_vdc3_init();
77
78      /* ==== Waits for completing to record video ==== */
79      while(1){
80        if( VDC3.VIDEO_MODE.BIT.VIDEO_MAIN_EXE == 0){
81            break;
82        }
83        }
84
85      while(1){
86        /* Loop */
87      }
88    }
89
90    /* End of File */
91
```

## 3.4 Sample Program Listing "io_vdc3_video_rec.c" (1/7)

```
1     /***********************************************************************
2     *   DISCLAIMER
3     *
4     *   This software is supplied by Renesas Electronics Corporation and is only
5     *   intended for use with Renesas products. No other uses are authorized.
6     *
7     *   This software is owned by Renesas Electronics Corporation and is protected under
8     *   all applicable laws, including copyright laws.
9     *
10    *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11    *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12    *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13    *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14    *   DISCLAIMED.
15    *
16    *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17    *   ELECTRONICS CORPORATION NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18    *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19    *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
20    *   AFFILIATES HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
21    *
22    *   Renesas reserves the right, without notice, to make changes to this
23    *   software and to discontinue the availability of this software.
24    *   By using this software, you agree to the additional terms and
25    *   conditions found by accessing the following link:
26    *   http://www.renesas.com/disclaimer
27    ***********************************************************************/
28    /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29    /***********************************************************************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : io_vdc3_video_rec.c
32    *   Abstract    : VDC3 Video recording example
33    *   Version     : 1.00.00
34    *   Device      : SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                              (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40    *   Description :
41    ************************************************************************
42    *   History     : Feb.28,2011 Ver.1.00.00
43    ***********************************************************************/
44
45
```

## 3.5 Sample Program Listing "io_vdc3_video_rec.c" (2/7)

```
46  /***********************************************************************
47  Includes  <System Includes> , "Project Includes"
48  ***********************************************************************/
49  #include "iodefine.h"
50  #include "io_vdc3_video_rec.h"
51
52  /***********************************************************************
53  Exported global variables and functions (to be accessed by other files)
54  ***********************************************************************/
55  /* ==== Global functions ==== */
56  void io_vdc3_init(void);
57  void io_int_vdc3_field_end(void);
58
59  /* ==== Global variables ==== */
60  #pragma section VREC_BUFF  /* Allocates the buffer at the 128-byte or 16-byte boundary
61                             in cache-disabled space */
62  unsigned short video_rec_buffer[VREC_FIELD_NUM][(VREC_FIELD_OFFSET / BYTES_PER_PIXEL)];
63  #pragma section
64
65  /***********************************************************************
66  Private global variables and functions
67  ***********************************************************************/
68  /* ==== Private fuctions ==== */
69  static void io_vdc3_init_video_in(void);
70  static void io_vdc3_init_video_rec(void);
71  static void io_vdc3_start(void);
72
73  /* ==== Private variables ==== */
74  static int saved_field_num;   /* Number of fields already recorded */
75
76  /***********************************************************************
77   * ID           :
78   * Outline      : Initializes the VDC3
79   * Include      :
80   * Declaration  : void io_vdc3_init(void);
81   * Description  : Uses the VDC3 video recording function for setting to store
82   *              : the video signal on SDRAM.
83   * Argument     : void
84   * Return Value : void
85   ***********************************************************************/
```

## 3.6 Sample Program Listing "io_vdc3_video_rec.c" (3/7)

```
86    void io_vdc3_init(void)
87    {
88      int i, j;
89
90      /* ==== Initializes the data ==== */
91      saved_field_num = 0;
92
93      /* ==== PORT ==== */
94      /* ---- Video (in) ---- */
95      PORT.PFCR1.BIT.PF7MD = 3;       /* DV_DATA7 */
96      PORT.PFCR1.BIT.PF6MD = 3;       /* DV_DATA6 */
97      PORT.PFCR1.BIT.PF5MD = 3;       /* DV_DATA5 */
98      PORT.PFCR1.BIT.PF4MD = 3;       /* DV_DATA4 */
99      PORT.PFCR0.BIT.PF3MD = 3;       /* DV_DATA3 */
100     PORT.PFCR0.BIT.PF2MD = 3;       /* DV_DATA2 */
101     PORT.PFCR0.BIT.PF1MD = 3;       /* DV_DATA1 */
102     PORT.PFCR0.BIT.PF0MD = 3;       /* DV_DATA0 */
103     PORT.PECR1.BIT.PE5MD = 3;       /* DV_HSYNC */
104     PORT.PECR1.BIT.PE4MD = 3;       /* DV_VSYNC */
105     PORT.PFCR2.BIT.PF8MD = 3;       /* DV_CLK */
106
107     /* ---- Display (out) ---- */
108     PORT.PGCR7.WORD = 0x5A01u;      /* LCD_DATA0 ( Bits 15 to 8 is H'5A. )*/
109     PORT.PGCR5.BIT.PG20MD= 1;       /* LCD_EXTCLK */
110     PORT.PGCR4.WORD = 0x1111u;      /* LCD_CLK, LCD_DE, LCD_HSYNC, LCD_VSYNC */
111     PORT.PGCR3.WORD = 0x1111u;      /* LCD_DATA15-12 */
112     PORT.PGCR2.WORD = 0x1111u;      /* LCD_DATA11-08 */
113     PORT.PGCR1.WORD = 0x1111u;      /* LCD_DATA07-04 */
114     PORT.PGCR0.BIT.PG3MD = 1;       /* LCD_DATA03 */
115     PORT.PGCR0.BIT.PG2MD = 1;       /* LCD_DATA02 */
116     PORT.PGCR0.BIT.PG1MD = 1;       /* LCD_DATA01 */
117
118     /* ==== CPG ==== */
119     CPG.STBCR7.BIT.MSTP74 = 0;      /* VDC3 */
120
121     /* ==== INTC ==== */
122     INTC.IPR10.BIT._VDC3 = 3;       /* Sets the interrupt priority level of VDC3 */
123
124     /* ==== VDC3 ==== */
125     /* ---- Initializes the video receiving block ---- */
126     io_vdc3_init_video_in();
127
128     /* ---- Initializes the video recording function ---- */
129     io_vdc3_init_video_rec();
130
131     /* ---- Enables the operation ---- */
132     io_vdc3_start();
133   }
134
```

## 3.7 Sample Program Listing "io_vdc3_video_rec.c" (4/7)

```
/*****************************************************************************
 * ID           :
 * Outline      : Interrupt at the writing complete
 * Include      : iodefine.h
 * Declaration  : void io_int_vdc3_field_end(void);
 * Description  : An interrupt handler when writing is complete in the video
 *              : recording mode. Counts the number of fields recorded when writing
 *              : a field is complete.
 *              : When the number of fields recorded is 30, it stops recording.
 * Argument     : void
 * Return Value : void
 *****************************************************************************/
void io_int_vdc3_field_end(void)
{
  volatile unsigned long dummy;

  VDC3.VIDEO_INT_CNT.BIT.F_END = 0;      /* Clears the write completion status of
                                         one field video */
  dummy = VDC3.VIDEO_INT_CNT.LONG;       /* Dummy read */
  saved_field_num++;                     /* Counts the number of fields already recorded
*/

  /* Stops when number of fields recorded reaches at the number of buffers */
  if(saved_field_num == VREC_FIELD_NUM){

    VDC3.VIDEO_INT_CNT.BIT.INT_F_EN   = 0;    /* Disables the write completion interrupt */

    /* ==== Notes about disabling the Video receiver block operation of VDC3
     [TN-SH7-A731A/E] ==== */
    /* (1) Do not select the DV_CLK function in multi-purpose I/O ports
     (PFCR2 register */
    PORT.PFCR2.BIT.PF8MD = 0;         /* Selects the PF8 pin  */

    /* (2) Sets the VIDEO_MAIN_EXE = 0 */
    VDC3.VIDEO_MODE.BIT.VIDEO_MAIN_EXE = 0;

    /* (3) Disables supplying the clock for the VDC3 (STBCR7) */
    CPG.STBCR7.BIT.MSTP74 = 1;

    /* (4) Selects the DV_CLK function in multi-purpose I/O ports (PFCR2 register) */
    PORT.PFCR2.BIT.PF8MD = 3;         /* Selects the DV_CLK */

    /* (5) Enables supplying the clock for the VDC3 */
    CPG.STBCR7.BIT.MSTP74 = 0;
  }
}
```

## 3.8 Sample Program Listing "io_vdc3_video_rec.c" (5/7)

```
182  /***********************************************************************************
183   * ID           :
184   * Outline      : Initializes the video receiving block
185   * Include      : iodefine.h
186   * Declaration  : static void io_vdc3_init_video_in(void);
187   * Description  : Initializes the video receiving block.
188   *              : BT.656 is used as the input video format.
189   * Argument     : void
190   * Return Value : void
191   ***********************************************************************************/
192  static void io_vdc3_init_video_in(void)
193  {
194    /* ----Input video format setting ---- */
195    VDC3.VIDEO_MODE.BIT.SEL_EXSYNC = 0;            /* Disables the external input
196                                                   sync signal */
197    VDC3.VIDEO_MODE.BIT.SEL_656601 = 0;            /* Specifies the BT.656 input */
198    VDC3.VIDEO_MODE.BIT.SEL_525625 = 0;            /* Number of lines for the
199                                                   input video: 525 (NTSC) */
200    VDC3.VIDEO_TIM_CNT.LONG    = 0x00000000ul; /* Latches the DV_DATA input
201                                                   signal at the rising edge */
202                                               /* Other control signals settings
203                                                   are not required for the BT656) */
204  }
```

## 3.9 Sample Program Listing "io_vdc3_video_rec.c" (6/7)

```
/*****************************************************************************
 * ID           :
 * Outline      : Initializes the video recording function
 * Include      : iodefine.h
 * Declaration  : static void io_vdc3_init_video_rec(void);
 * Description  : Uses the VDC3 video recording function for setting to store
 *              : the video signal on SDRAM.
 * Argument     : void
 * Return Value : void
 *****************************************************************************/
static void io_vdc3_init_video_rec(void)
{
  /* ---- Video recording function setting (BT.656, NTSC) ---- */
  VDC3.VIDEO_INT_CNT.BIT.INT_F_EN     = 1;    /* Enables the interrupt when writing
                                                 one field of data is completed */
  VDC3.VIDEO_MODE.BIT.BURST_MODE_MAIN = 0;    /* Bus in the video receiving block:
                                                 16-byte burst transfer */
  VDC3.VIDEO_MODE.BIT.ENDIAN_MAIN     = 0;    /* Bus in the video receiving block:
                                                 big endian */
  VDC3.VIDEO_MODE.BIT.VIDEO_MODE      = 0;    /* Video recording mode */
  VDC3.VIDEO_SIZE.BIT.VIDEO_HEIGHT    = VIN_INPUT_HEIGHT;    /* Number of lines */
  VDC3.VIDEO_SIZE.BIT.VIDEO_WIDTH     = VIN_INPUT_WIDTH; /* Number of pixels */
  VDC3.VIDEO_VSTART.BIT.VIDEO_VSTART_TOP = VIN_VSTART_VALIDDATA_TOP;
  VDC3.VIDEO_VSTART.BIT.VIDEO_VSTART_BTM = VIN_VSTART_VALIDDATA_BTM;
  VDC3.VIDEO_HSTART.BIT.VIDEO_HSTART     = VIN_HSTART_VALIDDATA;
  VDC3.VIDEO_SAVE_NUM.BIT.FIELD_SAVE_NUM = VREC_FIELD_NUM -1;
  VDC3.VIDEO_IMAGE_CNT.LONG = 0x80800300ul;  /* Adjusts the luminance contrast
                                                to default */
                                             /* Adjusts the luminance brightness
                                                to default */
                                             /* Luminance clipping is valid */
                                             /* Chrominance clipping is valid */
                                             /* Scales down vertically to 1/2 */
                                             /* Scales down horizontally to 1/2 */
  VDC3.VIDEO_BASEADR.LONG             = (unsigned long)video_rec_buffer;
  VDC3.VIDEO_LINE_OFFSET.LONG     = VREC_LINE_OFFSET;
  VDC3.VIDEO_FIELD_OFFSET.LONG        = VREC_FIELD_OFFSET;
  VDC3.VIDEO_DISP_SIZE.BIT.VIDEO_DISP_HEIGHT   = VREC_DISP_SZ_Y; /* Number of lines */
  VDC3.VIDEO_DISP_SIZE.BIT.VIDEO_DISP_WIDTH    = VREC_DISP_SZ_X; /* Number of pixels */
  VDC3.SGMODE.BIT.EX_SYNC_MODE    = 0;    /* Free-running mode */
}

```

## 3.10 Sample Program Listing "io_vdc3_video_rec.c" (7/7)

```
247   /*****************************************************************************
248    * ID           :
249    * Outline      : Enables the operation
250    * Include      : iodefine.h
251    * Declaration  : static void io_vdc3_start(void);
252    * Description  : Enables the operation.(Enabled from the next Vsync)
253    * Argument     : void
254    * Return Value : void
255    *****************************************************************************/
256   static void io_vdc3_start(void)
257   {
258     /*  ---- Enables the video receiving block  ---- */
259     VDC3.VIDEO_MODE.BIT.VIDEO_MAIN_EXE  = 1;
260   }
261   /* End of File */
262
```

## 3.11 Sample Program Listing "io_vdc3_video_rec.h" (1/2)

```
1     /***********************************************************************
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3     *
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6     *
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26    *   http://www.renesas.com/disclaimer
27    ***********************************************************************/
28    /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29    /***********************************************************************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : io_vdc3_video_rec.h
32    *   Abstract    : VDC3 Video recording example
33    *   Version     : 1.00.00
34    *   Device      : SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                              (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40    *   Description :
41    ************************************************************************
42    *   History     : Feb.28,2011 Ver.1.00.00
43    ***********************************************************************/
44
45
```

## 3.12 Sample Program Listing "io_vdc3_video_rec.h" (2/2)

```
46    /***************************************************************************
47    Macro definitions
48    ***************************************************************************/
49    #define BYTES_PER_PIXEL       2      /* Number of bytes per pixel */
50    #define RGB565_BLACK          0x0000u /* Black */
51    #define RGB565_WHITE          0xFFFFu /* White */
52    #define RGB565_GREEN          0x07E0u /* Green */
53    #define RGB565_BLUE           0x001Fu /* Blue */
54
55    /* ---- Video input parameters ---- */
56    #define VIN_VSTART_VALIDDATA_TOP 16   /* Vertical capture timing in the TOP field */
57    #define VIN_VSTART_VALIDDATA_BTM 279  /* Vertical capture timing in the BOTTOM field */
58    #define VIN_HSTART_VALIDDATA  276     /* Horizontal capture timing */
59    #define VIN_INPUT_HEIGHT      240     /* Number of lines of the input valid video */
60    #define VIN_INPUT_WIDTH       720     /* Number of pixels of the input valid video */
61
62    /* ---- Video recording parameters ---- */
63    #define VREC_DISP_SZ_Y        240     /* Video recording area height */
64    #define VREC_DISP_SZ_X        360     /* Video recording area width */
65    #define VREC_FIELD_NUM        30      /* Number of fields to record */
66    #define VREC_LINE_OFFSET      (((VREC_DISP_SZ_X * BYTES_PER_PIXEL) + 15 ) & 0xFFFFFFF0ul)
67                                         /* Number of bytes per line */
68    #define VREC_FIELD_OFFSET     (VREC_LINE_OFFSET * VREC_DISP_SZ_Y)
69                                        /* Number of bytes per field */
70
71    /***************************************************************************
72    Imported global variables and functions (from other files)
73    ***************************************************************************/
74    /* ==== Global functions ==== */
75    extern void io_vdc3_init(void);
76
77    /* ==== Global variables ==== */
78    extern unsigned short
      video_rec_buffer[VREC_FIELD_NUM][(VREC_FIELD_OFFSET/BYTES_PER_PIXEL)];
79
80    /* End of File */
81
```

## 4. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas Electronics website.

- Technical Update
  Notes about disabling the Video receiver block operation of Video Display Controller 3 (TN-SH7-A731A/E Rev. 1.00)
  The latest version of the technical update can be downloaded from the Renesas Electronics website.

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## Revision Record

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Apr.14.09 | — | First edition issued |
| 1.01 | Jul.31.09 | 12 | 2.3.1 Specifications, corrected |
| | | 14 to 15 | 2.3.4 Flow Chart of Specifying the Video Recording Mode, corrected |
| | | 16 | 2.3.5 Flow Chart of Interrupts, corrected |
| | | 17 to 23 | 3. Sample Program Listing, corrected |
| 1.02 | Mar.23.11 | 18 to 28 | Changed the configuration of the source code |

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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