SH7262/SH7264 Group

Video Display Controller 3 Video Display Example

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Summary

This application note describes the video display example using the SH7262/SH7264 Microcomputers (MCUs) on-chip Video Display Controller 3 (VDC3).

Target Device

SH7264 MCU

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1. Introduction

1.1 Specifications

The SH7264 MCU displays the input video on TFT-LCD panel.

Specifically, the digital video decoder decodes the NTSC video signal to input in the SH7264 MCU on-chip Video Display Controller (VDC3). The input video is displayed on the TFT-LCD panel connected with the VDC3.

1.2 Modules Used

- Video display controller (VDC3)
- General-purpose I/O ports
- I^2C bus Interface 3 (IIC3)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Video Display Controller 3 TFT-LCD Interfacing Example
- SH7262/SH7264 Group Video Display Controller 3 Video Recording Example
- SH7262/SH7264 Group Video Display Controller 3 How to Use the α (Alpha) Blending Window Function

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application note shows the pin connection example and configuration example to display the video by the VDC3.

2.1 VDC3 Operation

The VDC3 provides the video display function to display the video, and the video recording function to record the video. This application note describes the video display function.

2.1.1 Overview

The VDC3 provides the following four functions. The function related to the video display is the "video display function". The video display function and video recording function cannot be used at the same time.

1. Video display function: Reduces the size of the input video, buffers the resultant video data in memory, and then displays the video on the panel
2. Video recording function: Stores a specified number of fields of the input video in SDRAM
3. Function for overlaying graphic images (two planes) on the input video
4. Function for outputting the control signals for the TFT-LCD panel

2.1.2 Features

The following table lists the VDC3 features.

Table 1 VDC3 Features

Item	Description	Remarks
Operating frequency	Video input clock: 27 MHz Panel clock: 4 to 36 MHz (depends on the panel specifications)	For video input
Input video standard	8-bit input compliant to the ITU-R BT.656 standard (27 MHz) 8-bit serial input compliant to the ITU-R BT.601 standard (27 MHz)	
Video recording function	Stores the video data in the RGB565 format at a rate of the 1/2 field (NTSC: 30 fps; PAL: 25 fps)	
Video quality adjustment function	Contrast adjustment and brightness adjustment	
Video scaling processing	Vertical: x 1/2, x 1/3, x 1/4 Horizontal: x 2/3, x 1/2, x 1/3, x 1/4 Each scaled value can be further multiplied by 6/7 to support PAL.	
Output video size (note)	640 pixels x 480 lines (VGA size) 480 pixels x 240 lines (WQVGA size) 320 pixels x 240 lines (QVGA , landscape-mode) 240 pixels x 320 lines (QVGA, portrait-mode)	For output on panel
Output video format	RGB565 progressive video output (16-bit parallel output)	
Sync signal output	Outputs the control signals for the TFT-LCD panel	
Interrupt output	Line interrupt output (this can be output on a desired line) VSYNC cycle fluctuation detection signal for the BT.601 and BT.656 Field write completion signal Overflow/underflow detection signal for the internal buffer	Other
Graphics images	Two planes (layers 1 and 2) RGB565 progressive format (α = none, R: 5 bits, G: 6 bits, B: 5 bits; 16 bits in total) αRGB4444 progressive format (α: 4 bits, R: 4 bits, G: 4 bits, B: 4 bits; 16 bits in total)	
Graphics functions	• α blending window function: Mixes the input video and layers 1 and 2 according to the transparency rate α in the specified region (fade-in and fade-out functions are available) • Chroma-keying function: Mixes the images with applying the specified RGB color according to the transparency rate α. • Dot α function: Mixes the images according to the transparency rate α when the target is a graphic image in α RGB4444 format. For each dot, the priority among the α values of the above functions is as follows: α blending window > chroma-keying > dot α	

Note: The maximum viewable area for the input image is 480 pixels x 240 lines (NTSC), and 480 pixels x 288 lines (PAL).

2.1.3 I/O Pins

The following table lists the VDC3 I/O pins.

Table 2 VDC3 I/O Pins

Symbol	I/O	Pin Name	Description	Remarks
DV_CLK	Input	Video input clock	BT.601, BT.656 clock input pin	For video input
DV_VSYNC	Input	VSYNC input	BT.601 VSYNC signal input pin	
DV_HSYNC	Input	HSYNC input	BT.601 HSYNC signal input pin	
DV_DATA7 to 0	Input	BT.601 or BT.656 input	BT.601 or BT.656 data signal input pins	
LCD_CLK	Output	Panel clock	Panel clock output pin	For output on panel
LCD_EXCLK	Input	Panel clock source	Panel clock source input pin	
LCD_VSYNC	Output	Panel VSYNC output	Vertical sync signal output pin for the panel	
LCD_HSYNC	Output	Panel HSYNC output	Horizontal sync signal output pin for the panel	
LCD_DE	Output	Panel data enable output	Data enable signal or data start position pulse signal output pin for the panel	
LCD_DATA15 to 0	Output	Panel data output	Data output pins for the panel MSB LSB MSB LSB [15 : 11]: Red [4 : 0] [10 : 5]: Green [5 : 0] [4 : 0]: Blue [4 : 0]	
LCD_M_DISP	Output	Panel control signal	Alternating signal for the panel	

2.1.4 Configuration

Figure 1 shows the VDC3 block diagram. Refer to Table 3 for each block.

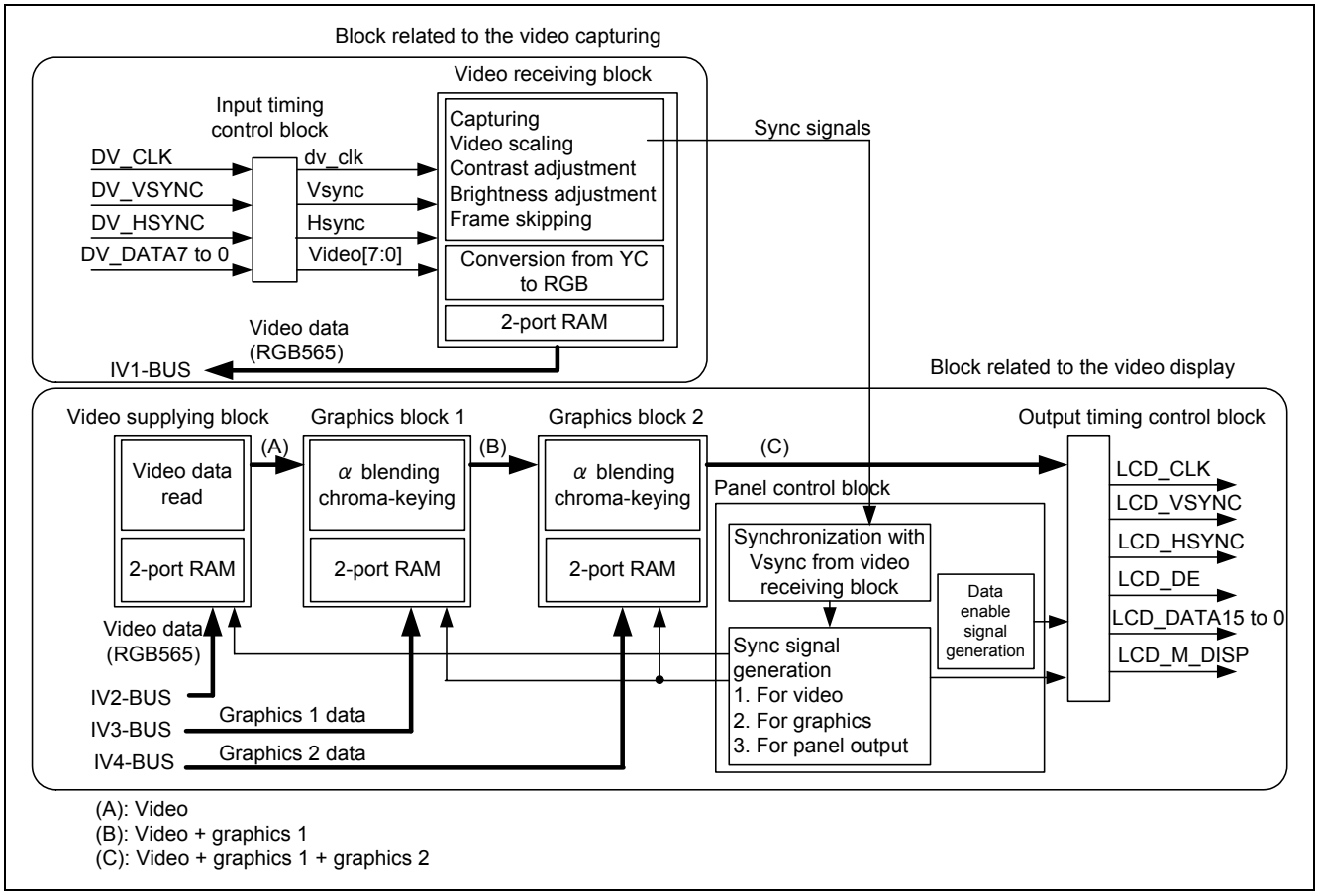


Figure 1 VDC3 Block Diagram

Table 3 VDC3 Functional Blocks

Block Name	Overview
Input timing control block	Controls the timing of the input sync signal clock rising or falling edge, and the sync polarity. It also controls the timing of the BT.601 and BT.656 video input signals clock rising or falling edge.
Video receiving block	(1) Captures the input video, scales, adjusts the contrast, and the brightness. (2) Converts the YC format to the RGB565 format, and stores the data via the IV1-BUS. (3) Skips the field, and stores the data in the RGB565 format via the IV1-BUS.
Video supplying block	Reads the video data via the IV2-BUS.
Graphics block 1	Reads a graphics image (layer 1) from the memory via the IV3-BUS, overlays it on the video sent from the video supplying block, and outputs the result to graphics block 2.
Graphics block 2	Reads a graphics image (layer 2) from the memory via the IV4-BUS, overlays it on the output from graphics block 1, and outputs the result to the output timing control block.
Panel control block	Generates the sync signals to output to the panel
Output timing control block	Controls the timing of the output sync signal clock rising or falling edge, and the sync signal polarity. It also controls the timing of the RGB565 video output signals clock rising or falling edge.

2.1.5 Input Video

The VDC3 has two options for the input video formats; BT.601 input or BT.656 input. This section describes the VDC3 input video formats in detail.

In addition, the VDC3 supports 525 lines (NTSC) and 625 lines (PAL) as the number of lines for the input video. This application is an example of 525 lines (NTSC).

(1) BT.601 Input

BT.601 is a standard for the NTSC and PAL, the analog television system, to specify the conversion and sampling frequency to digitize the analog video signal. The table below lists an overview of the BT.601. Refer to BT.601 specifications for detail.

Table 4 BT.601 Overview (For NTSC)

Item	Description	
Scan Lines	525 (2:1 interlace)	
Frame Rate	60 fps	
Aspect Ratio	4:3 or 16:9	
Sample Structures	4:2:2	4:4:4
Color Format	Y, Cr, Cb	Y, Cr, Cb or R, G, B
Number of Samples per Total Line	858 (Y), 429 (Cr, Cb)	858
Sampling Frequency	13.5 MHz (Y), 6.75 MHz (Cr, Cb)	13.5 MHz
Form of Coding	8 or 10 bits/sample	
Number of Samples per Digital Active Line	720 (Y), 360 (Cr, Cb)	720
Range of Data (8-bit coding)	16 to 235 (Y), 16 to 240 (Cr, Cb)	16 to 240

When selecting the BT.601 input, use DV_DATA7 to DV_DATA0 pins, DV_VSYNC pin, DV_HSYNC pin, and DV_CLK pin as the video input pins. Input the data signal to DV_DATA7 to DV_DATA0 pins, the vertical sync signal in DV_VSYNC pin, and the horizontal sync signal in DV_HSYNC pin.

Figure 2 shows the timing to capture video in the BT.601 input. Use the VIDEO_VSTART register to set the interval between the DV_VSYNC signal and the valid data area. The polarity of the DV_VSYNC and DV_HSYNC signals can be changed by the VIDEO_TIM_CNT register.

As the input video is interlaced 2:1, Field 1 (TOP) and Field 2 (BOTTOM) of the data must be recognized. The VDC3 recognizes them by the value set in the FIELD_SKEW [9:0] bits in the VIDEO_TIM_CNT register. Figure 3 shows how to recognize fields in the BT.601. The data format for the input video is YC422. Figure 4 shows the data input format.

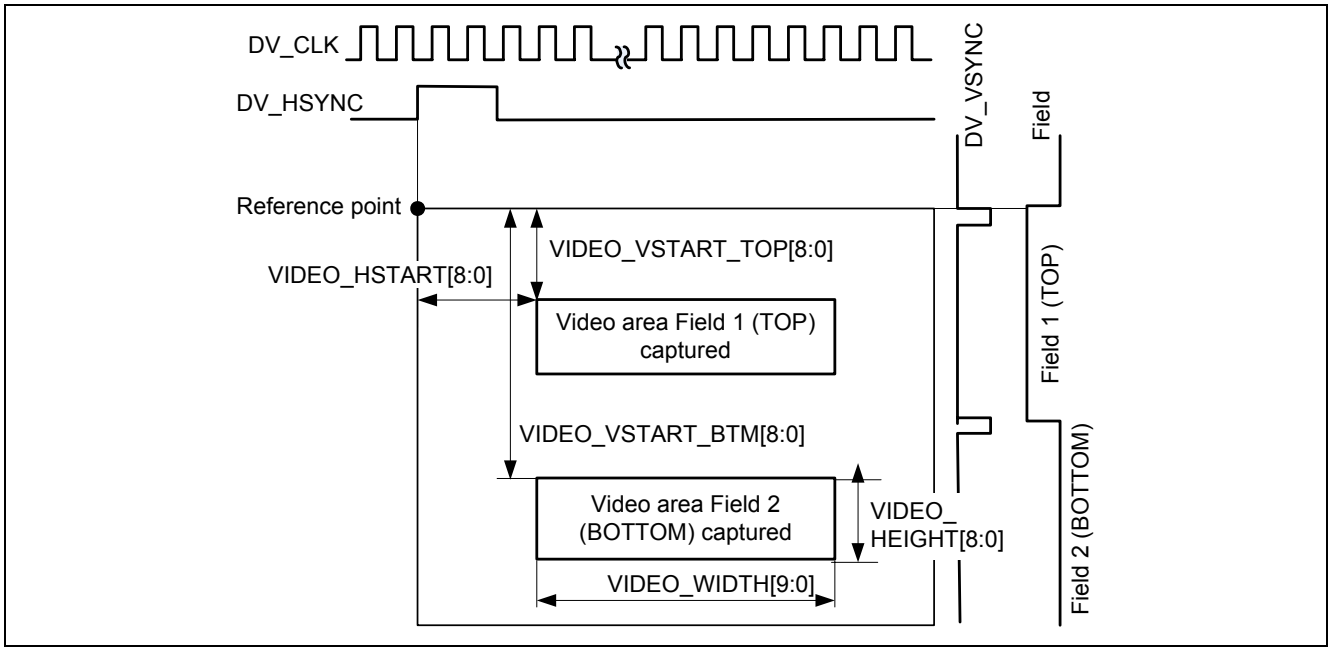


Figure 2 Capture Timing in the BT.601 Input

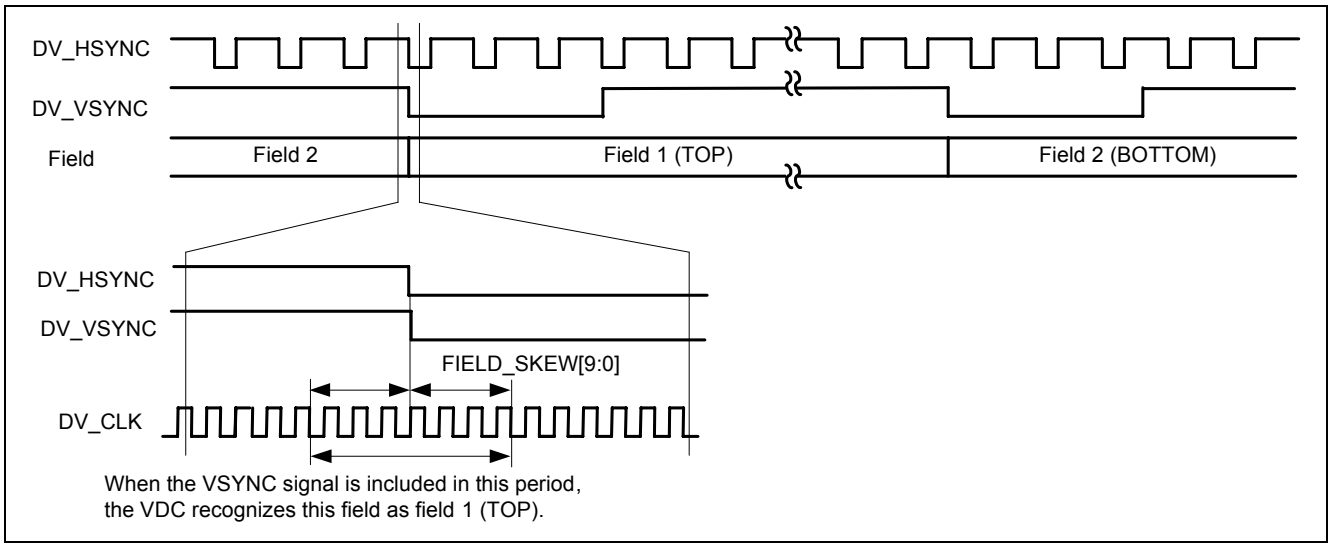


Figure 3 VDC3 Recognizing the Fields in BT.601

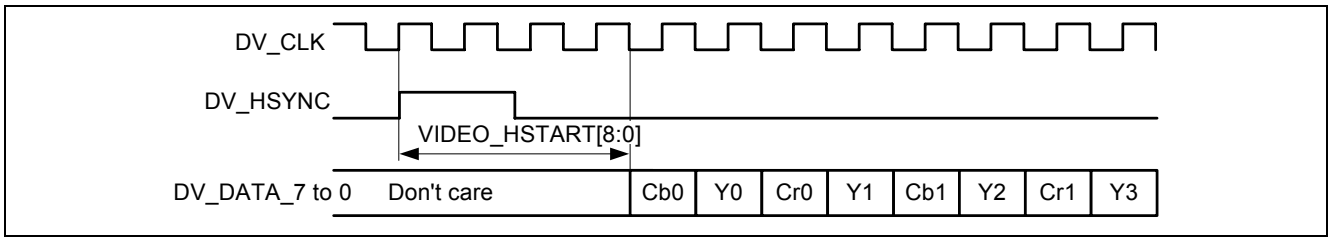


Figure 4 Data Input Format for BT.601 input

(2) BT.656 Input

BT.656 is a standard to specify the data structure of the digital video signals, which is defined in BT.601. The structure of the data signals and the reference codes are specified in BT.656. Replace the data output in the blanking interval with the reference codes to retrieve the Vsync and Hsync signals timing, and the field information. The following table lists the function of each bit in the reference codes.

Table 5 Reference Codes (For 8-bit data)

Bit No.	The First Byte (H'FF)	The Second Byte (H'00)	The Third Byte (H'00)	The Fourth Byte (H'XX)
7	1	0	0	Fixed to 1
6				0: field 1, 1: field 2
5				1 during the vertical blanking interval, other, 0
4				0: SAV (Start of Active Video) 1: EAV (End of Active Video)
3				Protection bit (note)
2				Protection bit (note)
1				Protection bit (note)
0				Protection bit (note)

Note: Specific values for bits 6 to 4 are specified in BT.656.

When selecting the BT.656 input, use DV_DATA7 to DV_DATA0 pins only. As the vertical or horizontal sync information is retrieved by the reference code that is embedded in the data signal, input the data signals compliant to BT.656.

The following figure shows the timing to capture video in the BT.656 input and the input data format.

		1H cycle									
		EAV				H blank	SAV				Valid area
		1	2	3	4		273	274	275	276	277 278 279 280 ... 1716
Field 2 (BOTTOM)	1	FF	00	00	F1		FF	00	00	EC	Blanking data area
	2	FF	00	00	F1		FF	00	00	EC	
	3	FF	00	00	F1		FF	00	00	EC	
Field 1 (TOP)	4	FF	00	00	B6		FF	00	00	AB	Blanking data area
		FF	00	00	B6		FF	00	00	AB	
	19	FF	00	00	B6		FF	00	00	AB	
	20	FF	00	00	9D		FF	00	00	80	Cb0 Y0 Cr0 Y1 ... Cb359 Y718 Cr359 Y719
		FF	00	00	9D		FF	00	00	80	
		FF	00	00	9D		FF	00	00	80	Valid pixel data area
		FF	00	00	9D		FF	00	00	80	
		FF	00	00	9D		FF	00	00	80	
	263	FF	00	00	9D		FF	00	00	80	
	264	FF	00	00	B6		FF	00	00	AB	Blanking data area
	265	FF	00	00	B6		FF	00	00	AB	
Field 2 (BOTTOM)	266	FF	00	00	F1		FF	00	00	EC	Blanking data area
		FF	00	00	F1		FF	00	00	EC	
	282	FF	00	00	F1		FF	00	00	EC	
	283	FF	00	00	DA		FF	00	00	C7	Cb0 Y0 Cr0 Y1 ... Cb359 Y718 Cr359 Y719
		FF	00	00	DA		FF	00	00	C7	
		FF	00	00	DA		FF	00	00	C7	Valid pixel data area
		FF	00	00	DA		FF	00	00	C7	
		FF	00	00	DA		FF	00	00	C7	
	525	FF	00	00	DA		FF	00	00	C7	

Figure 5 Capture Timing in the BT.656 Input and the Data Input Format (For NTSC)

2.1.6 Video Display Function

This section describes the procedure to display the captured video on the TFT-LCD panel.

The Video receiving block captures Field 1 or Field 2. Then, it scales down the captured video, adjusts the contrast and brightness. After converting the captured video from the YC format to the RGB 565 format, the Video receiving block temporarily stores the video data on RAM (line buffer). The Video supplying block reads the data stored in the line buffer regularly.

Next, the Video supplying block transfers the video data with the sync signals for video generated by the DC_CLK signal to Graphics block 1. Graphics block 1 transfers the video data to Graphics block 2. The graphics 1 data can be included with the video data. Similarly, the Graphics block 2 transfers the video data to the Output timing control block.

Finally, the Output timing control block outputs the video data and control signal to a TFT-LCD panel, synchronizing with the sync signals for panel output generated in the Panel control block.

The following figure shows an overview of the video and graphics image processing.

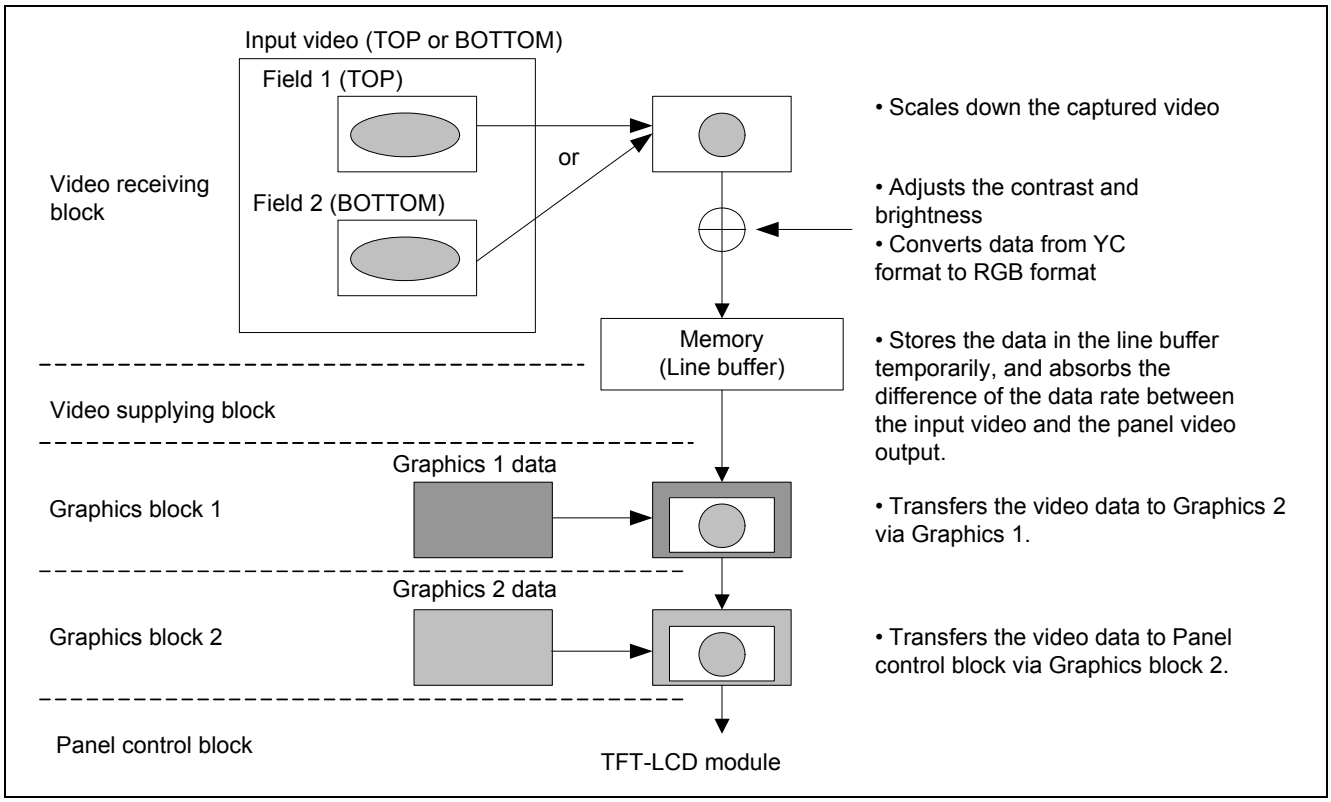


Figure 6 Video and Graphics Image Processing Overview

2.1.7 Adjusting the Data Rate between the Input Video and Display on the Panel

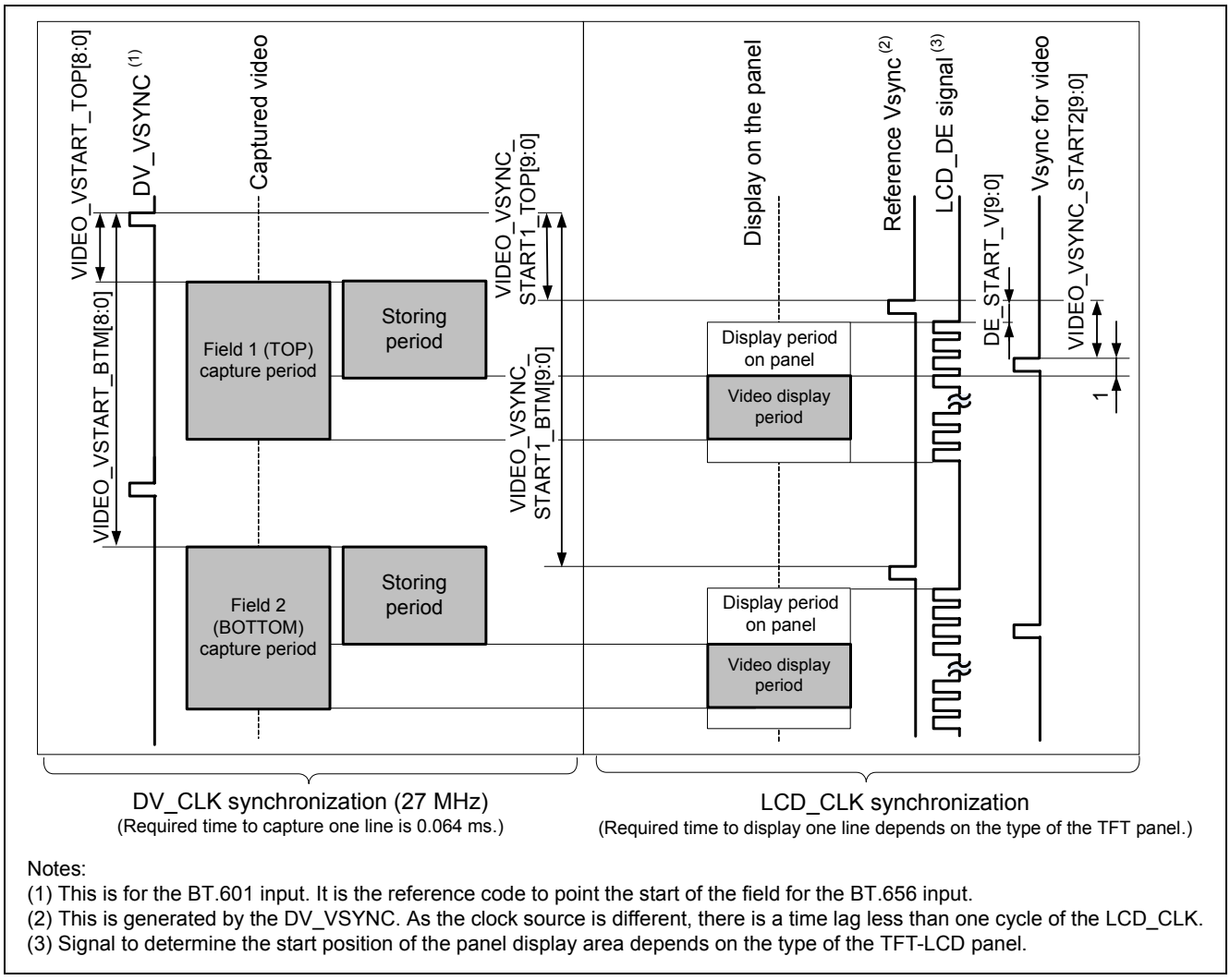
The VDC3 temporarily stores the video data in the line buffer using the video display function. This is to absorb the difference of the data rate between input video and output on the panel. This section explains how to adjust the data rates.

When setting the capacity of the line buffer is more than one field, adjusting the data rates is not required. When reducing the size of memory, calculate the capacity of the line buffer by the following steps.

The figure below shows an example of when the length of time to output data on panel is shorter than the length of time to capture the input video.

Firstly, determine the position of the reference Vsync. As the video can be displayed after it is captured, specify the timing for completing to display the video as same as when capturing the video is complete. Secondly, calculate the capacity of the line buffer. As the line buffer stores the input video that is captured until it starts to display the video, the "storing period" shown in the figure below is the capacity of the line buffer.

The capacity of the line buffer must take into account the margin values. Refer to formulae shown in Table 6 to Table 8.

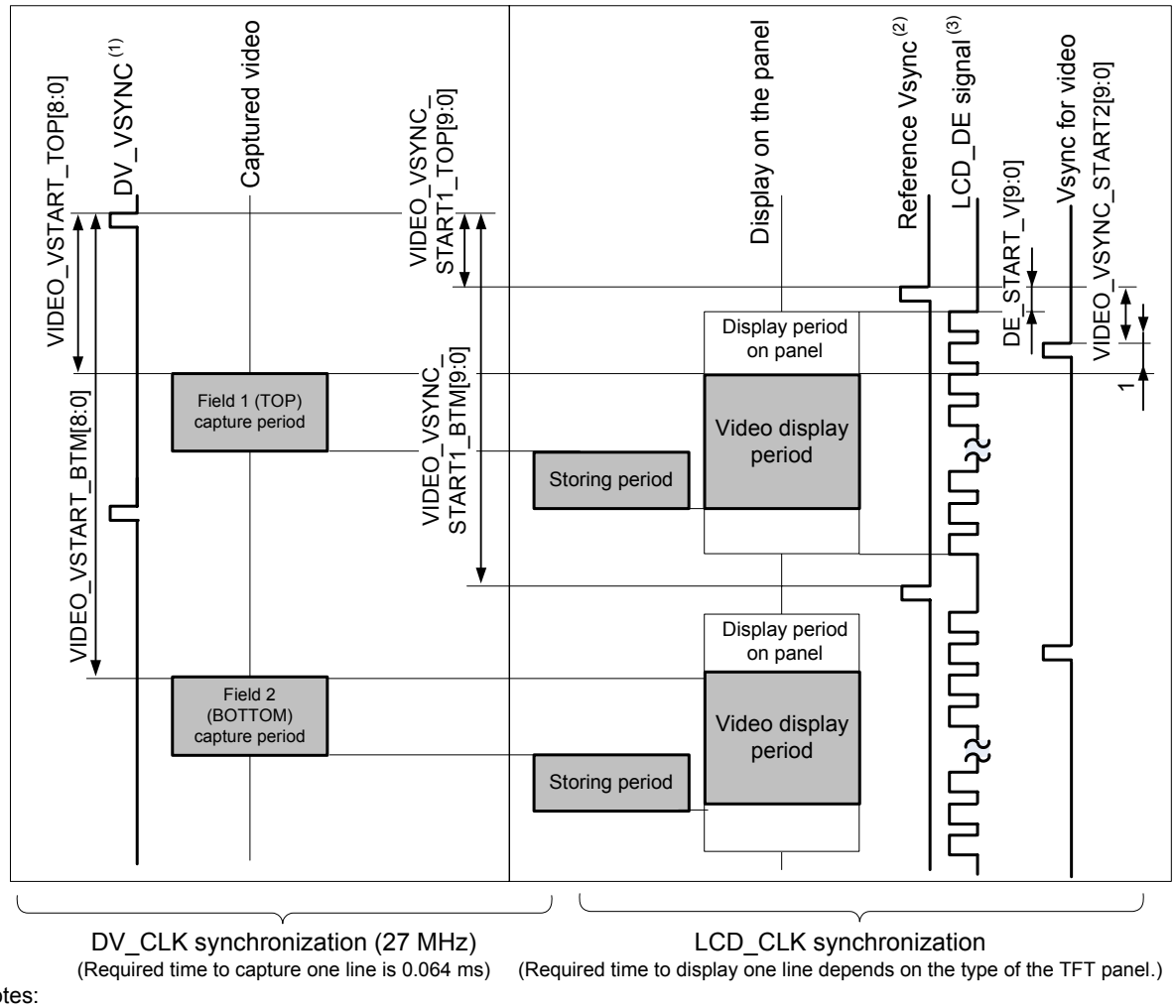


Notes:
(1) This is for the BT.601 input. It is the reference code to point the start of the field for the BT.656 input.
(2) This is generated by the DV_VSYNC. As the clock source is different, there is a time lag less than one cycle of the LCD_CLK.
(3) Signal to determine the start position of the panel display area depends on the type of the TFT-LCD panel.

Figure 7 Adjusting the Data Rates (Video display period on panel is shorter than capture period)

Figure 8 shows an example of when the length of time to output data on panel is longer than the length of time to capture the input video.

As well as the procedure shown in Figure 7, firstly determine the position of the reference Vsync. As the data does not result in underflow, specify the same timing to start capturing and displaying video. Secondly, calculate the capacity of the line buffer. As the line buffer stores the remaining display data when capturing is completed, the "storing period" shown in the figure below is the capacity of the line buffer. Refer to Table 6 to Table 8 for formulae.



Notes:
(1) This is for the BT.601 input. It is the reference code to point the start of the field for the BT.656 input.
(2) This is generated by the DV_VSYNC. As the clock source is different, the is a time lag less than one cycle of the LCD_CLK.
(3) Signal to determine the start position of the panel display area depends on the type of the TFT-LCD panel.

Figure 8 Adjusting the Data Rates (Video display period on panel is longer than capture period)

Table 6 Parameters for Adjusting the Data Rates

Parameters			
No.	**Description**	**Register Name/Value**	**Unit**
(1)	HSYNC cycle of the input video	0.064	ms
(2)	Vertical size of the valid video	VIDEO_SIZE register (VIDEO_HEIGHT [8:0] bits)	line
(3)	HSYNC cycle for the TFT-LCD panel	Depends on the type of the panel	ms
(4)	Vertical size of the video to display	VIDEO_DISP_SIZE register (VIDEO_DISP_HEIGHT [8:0] bits)	line
(5)	Line buffer margin	Specify 6 or greater	line
(6)	Vertical start position of the valid video in the TOP field	VIDEO_VSTART register (VIDEO_VSTART_TOP [8:0] bits)	line
(7)	Vertical start position of the valid video in the BOTTOM field	VIDEO_VSTART register (VIDEO_VSTART_BTM [8:0] bits)	line
(8)	Number of lines between the reference Vsync and display enable area	Depends on the type of the panel	line

Table 7 Formulae for Adjusting the Data Rates (to display at the top of the panel)

Formula			
No.	**Description**	**Register Name/Value**	**Unit**
(9)	VIDEO_VSYNC_TIM2 register (VIDEO_VSYNC_START2 [9:0] bits)	(8) - 1	line
(10)	Time lag between the input video and output on the panel (Storing period)	(1) x (2) - (3) x (4)	ms
(11)	Convert to the number of lines (the number of lines to store the data) Plus value: Storing period in Figure 7 Minus value: Storing period in Figure 8	When (10) is a plus value: (10)/(1) When (10) is an minus value: (10)/(3)	line
(12)	VIDEO_LINE_BUFF_NUM register Insert the margin	(11) + (5)	line
(13)	VIDEO_VSYNC_TIM1 register (VIDEO_VSYNC_START1_TOP [9:0] bits)	When (10) is a plus value: (6) + (11) - (8) + (5)/2 When (10) is an minus value: (6) - (8) + (5)/2	line
(14)	VIDEO_VSYNC_TIM1 register (VIDEO_VSYNC_START1_BTM [9:0] bits)	When (10) is a plus value: (7) + (11) - (8) + (5)/2 When (10) is an minus value: (7) - (8) + (5)/2	line

Table 8 Formulae to Change the Display Position

Formula			
No.	**Description**	**Register Name/Value**	**Unit**
(15)	VIDEO_VSYNC_TIM2 register	(9) + the line to start displaying	line
(16)	Convert to the number of lines of the input video	(3) x the line to start displaying/(1)	line
(17)	VIDEO_VSYNC_TIM1 register (VIDEO_VSYNC_START1_TOP [9:0] bits)	(13) - (16)	line
(18)	VIDEO_VSYNC_TIM1 register (VIDEO_VSYNC_START1_BTM [9:0] bits)	(14) - (16)	line

2.1.8 Panel Control Signal Output Timing

To display video on the TFT-LCD panel, specify the output timing for the panel control signal as same as that of the TFT-LCD panel. The figure below shows the timing for the panel control signal including the sync signal for video. For details, refer to the application note "SH7262/SH7264 Group Video Display Controller 3 TFT-LCD Interfacing Example".

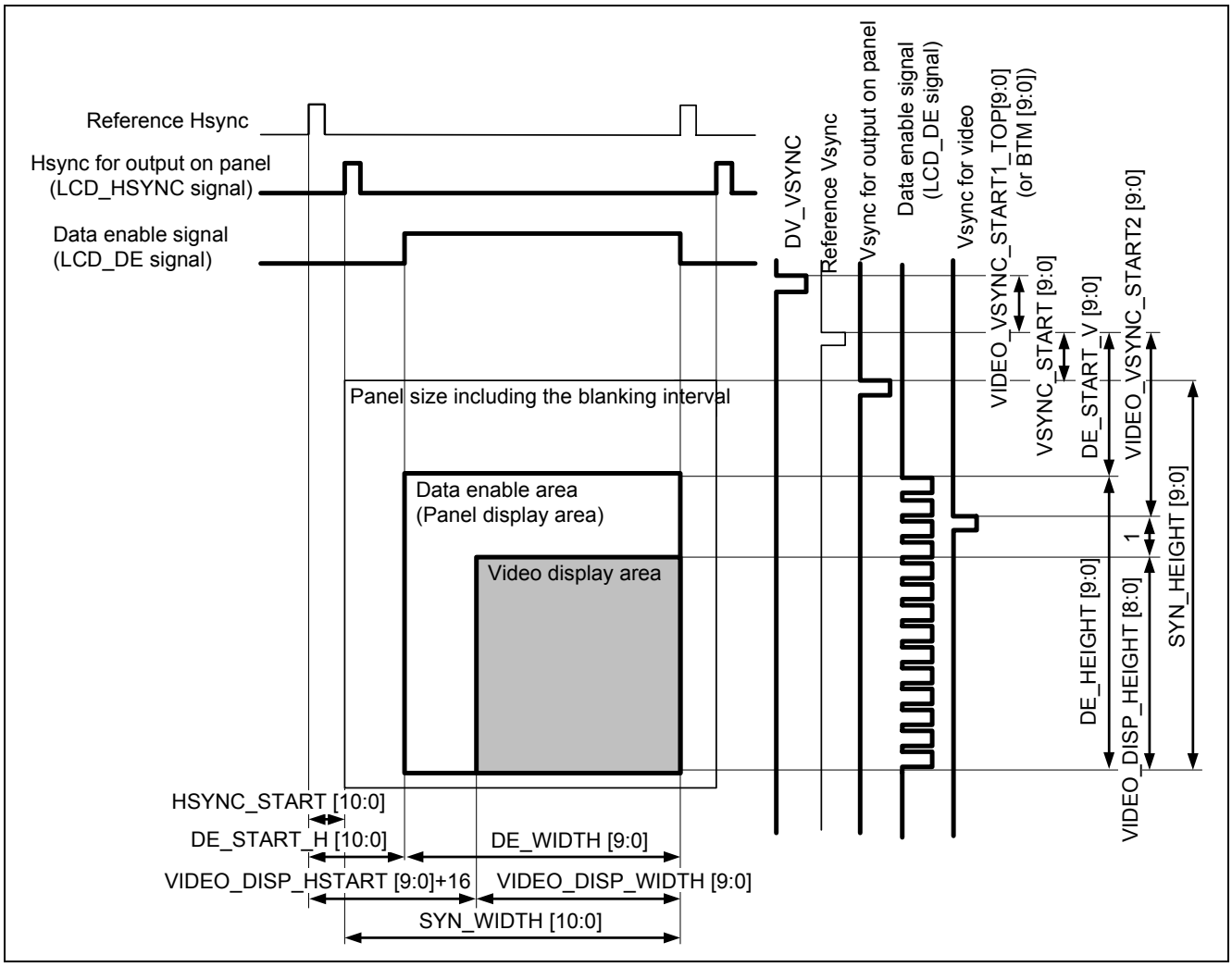


Figure 9 Synchronization Timing of the Panel Control Signal

2.2 Digital Video Decoder Specifications

When using the analog NTSC video signal, connect the digital video decoder as an extension to set it to output video in the input video format described in section 2.1.5.

This section describes the specifications of the digital video decoder (AK8851) used in this application.

2.2.1 Overview

The following table lists an overview of the digital video decoder used in this application.

Table 9 Digital Video Decoder Specifications

Item	Description
Input analog signal	NTSC, PAL, SECAM (Composite video signal) S-video signal (Component video signal)
Output digital signal	Y, Cb, Cr signals compliant to the ITU-R BT.601 and BT.656 specifications
Output clock	27 MHz
Analog input pin	6 channels
Output data bus width	8-bit parallel output (16-bit output is also possible)
Controlled by	I^2C control

2.2.2 Digital Video Decoder Circuit Example

The following figure shows an example of the digital video decoder circuit.

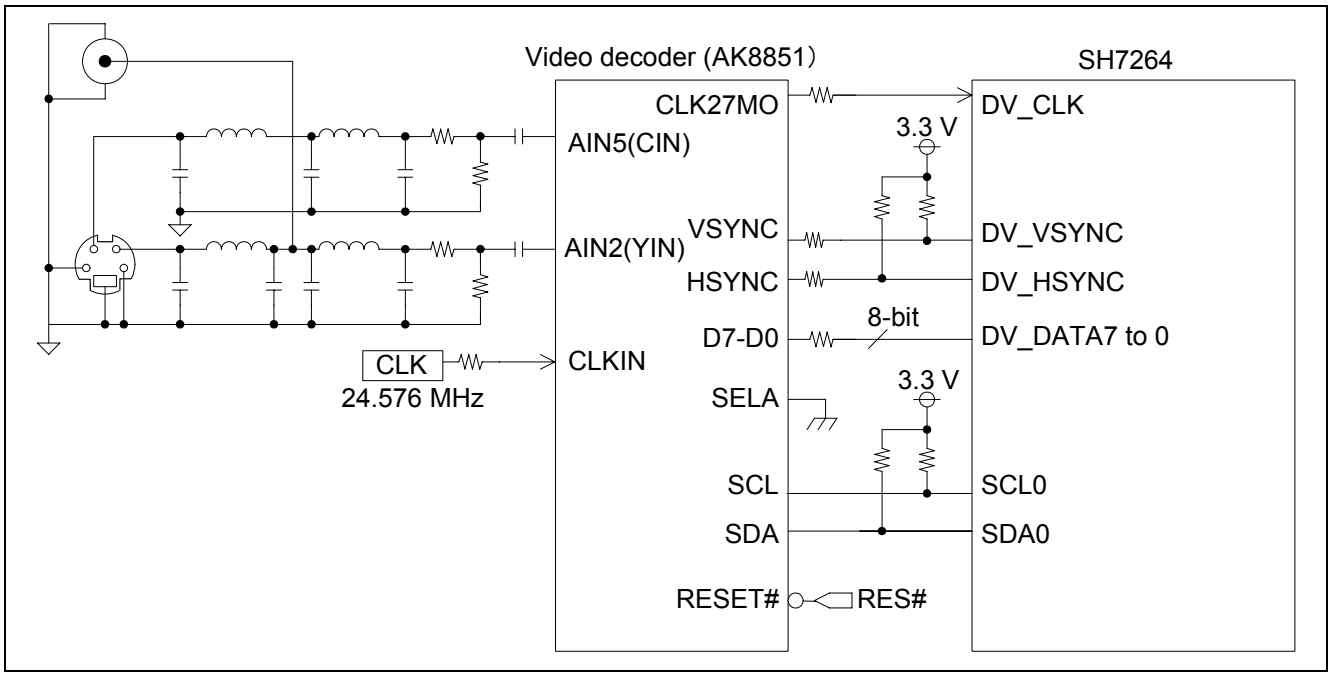


Figure 10 Example of the Digital Video Decoder Circuit

2.3 TFT-LCD Panel Specifications

For the specifications and circuit example of the TFT-LCD panel used in this application, refer to the application note "SH7262/7264 Group Video Display Controller 3 TFT-LCD Interfacing Example".

2.4 Sample Program Specifications

This section describes the specifications of the sample program and shows the flow charts of each processing.

2.4.1 Specifications

- Inputs the NTSC video to output on the QVGA size (V 320 x H 240) TFT-LCD panel
- Scales down the video to 1/3 (horizontal), 1/3 (vertical), to output the video in the center of the panel in V 160 x H 240
  (HSYNC cycle for the input video: 0.064 ms, HSYNC cycle for the TFT-LCD panel output: 0.045 ms)
- Uses the BT.656 as the input video format

2.4.2 Main Flow Chart of the Sample Program

Figure 11 shows the main flow chart of the sample program. The sample program executes a series of the initializing processing as shown in Figure 12 to Figure 16 to display the input video on the TFT-LCD panel.

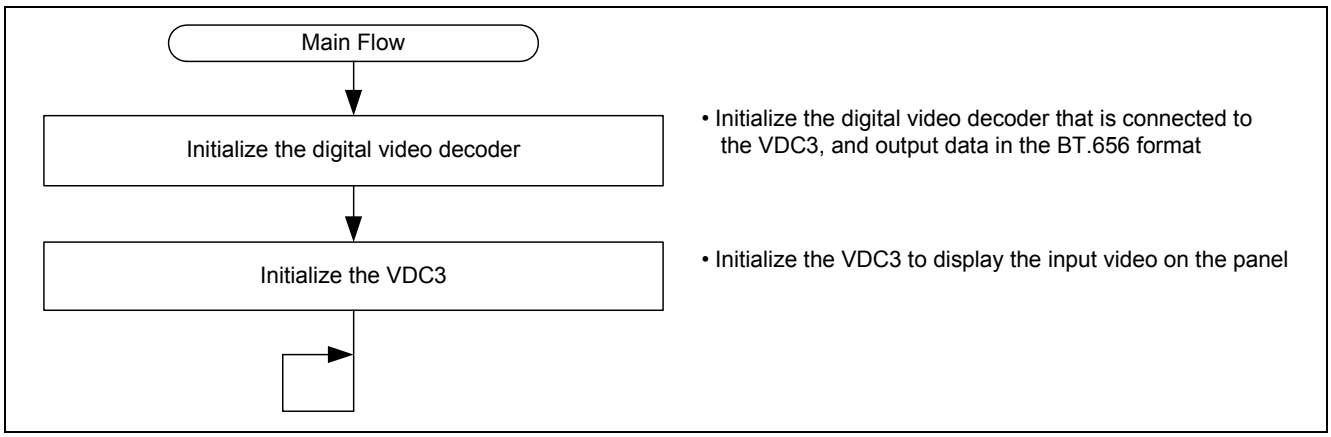


Figure 11 Sample Program Main Flow Chart

2.4.3 Flow Chart of Specifying Input Video Format

The figure below shows an example of specifying the input video format. BT.656 input is specified in this application.

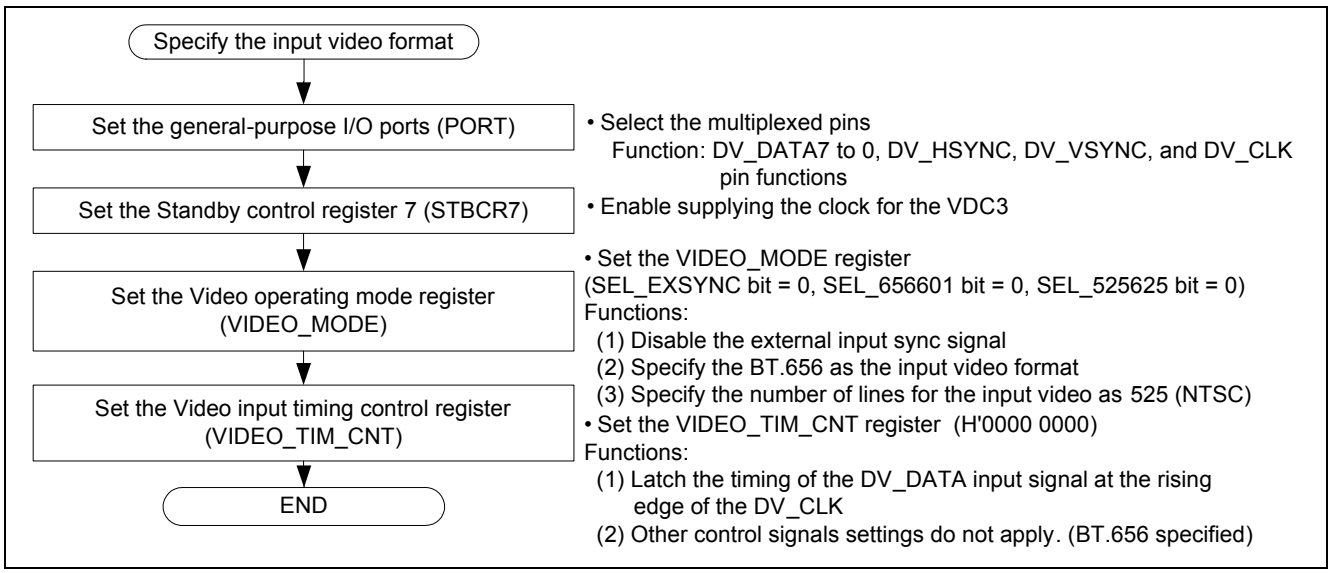


Figure 12 Flow Chart of Specifying the Input Video Format

2.4.4 Flow Chart of the Video Display Function Setting

Figure 13 and Figure 14 show examples of setting the video display function. This setting enables the VDC3 to transfer the captured video to the output timing control block.

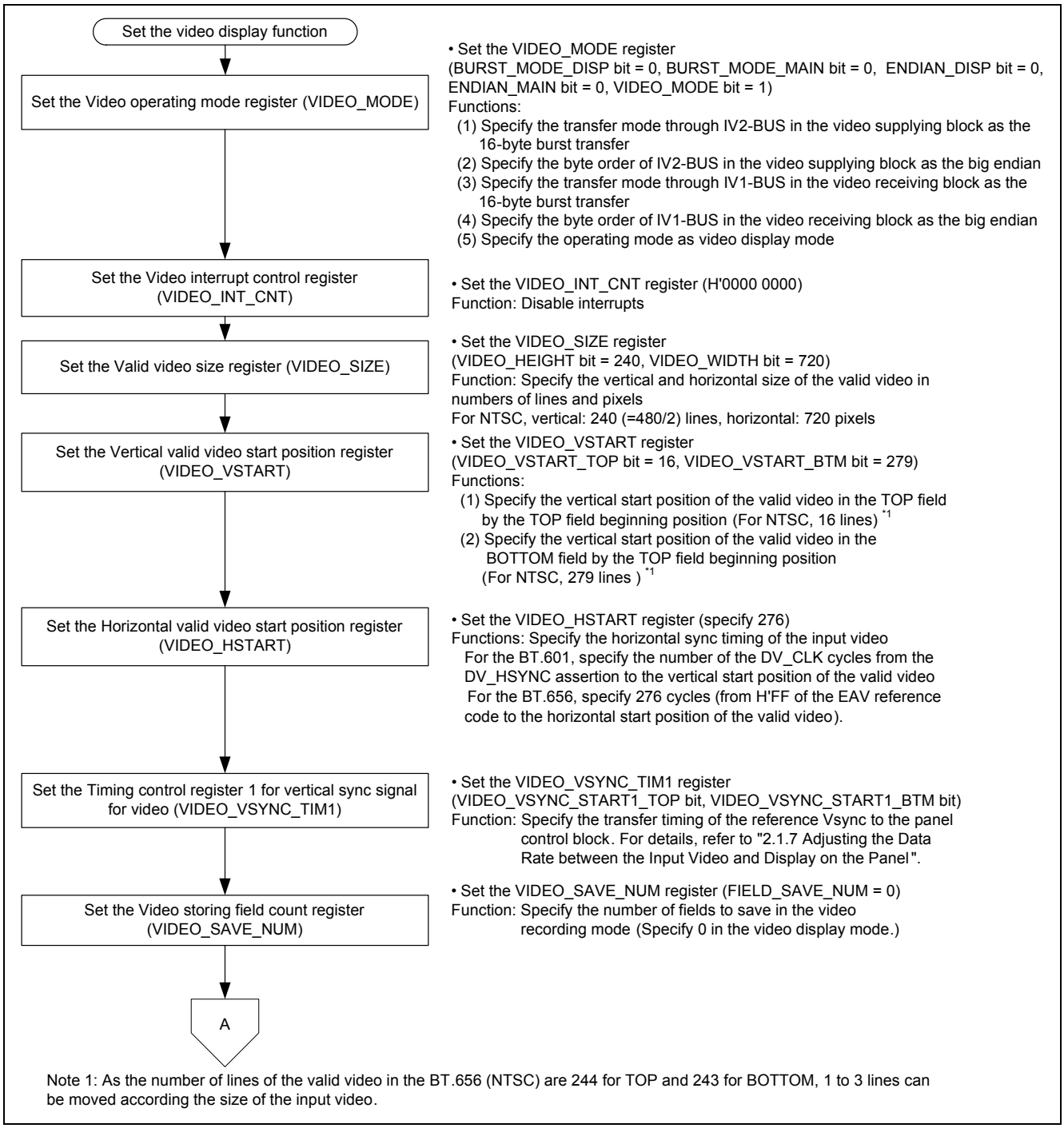


Figure 13 Setting Example of the Video Display Function (1/2)

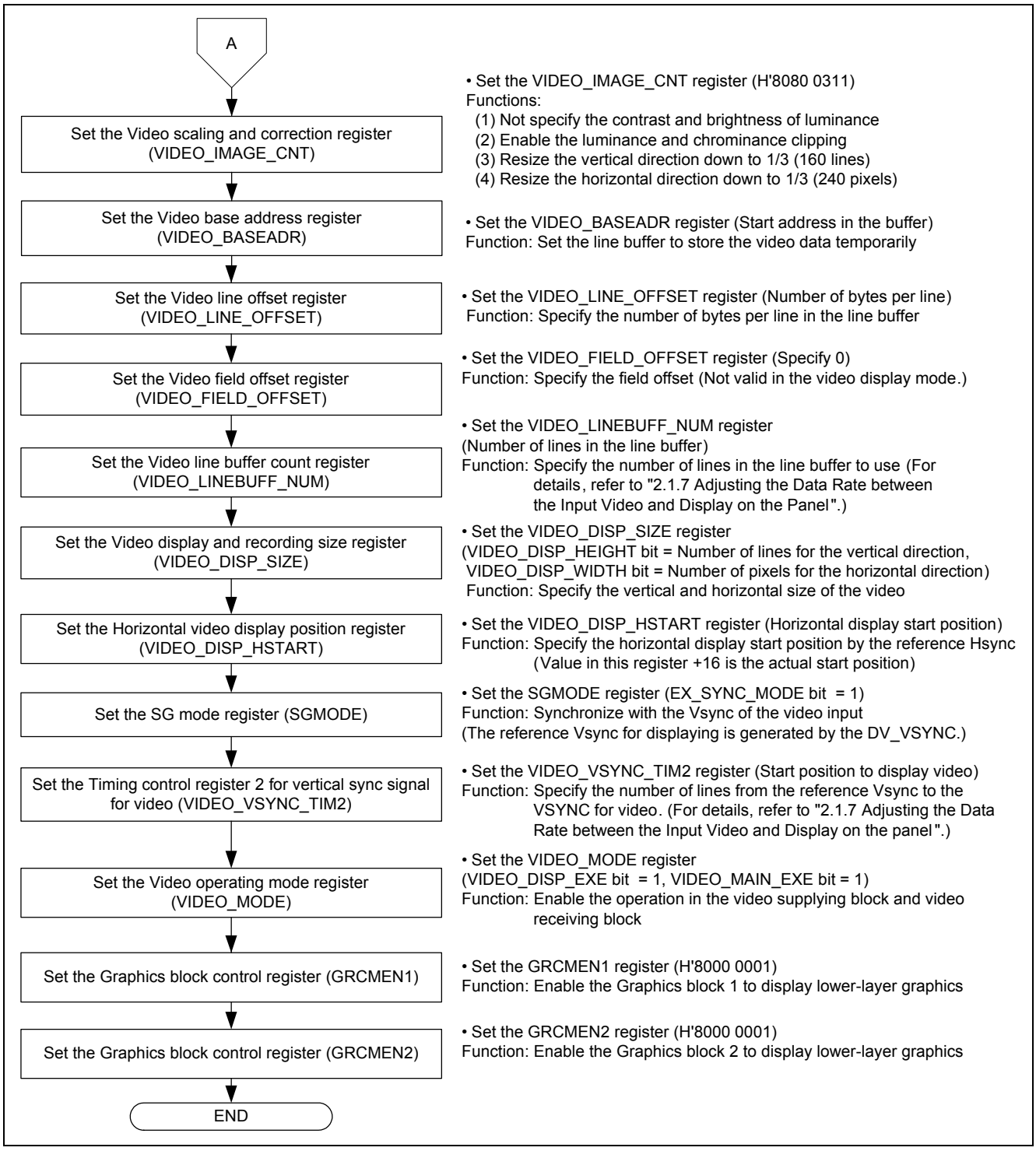


Figure 14 Setting Example of the Video Display Function (2/2)

2.4.5 Setting the Panel Control Signal Output

Figure 15 and Figure 16 show examples of setting the panel control signal output function. Follow these procedures in this section to set the control signal output on the TFT-LCD panel.

Values listed in Figure 15 and Figure 16 are set according to the specifications of the TFT-LCD panel used in this application. Alter the setting according to the type of the TFT-LCD panel.

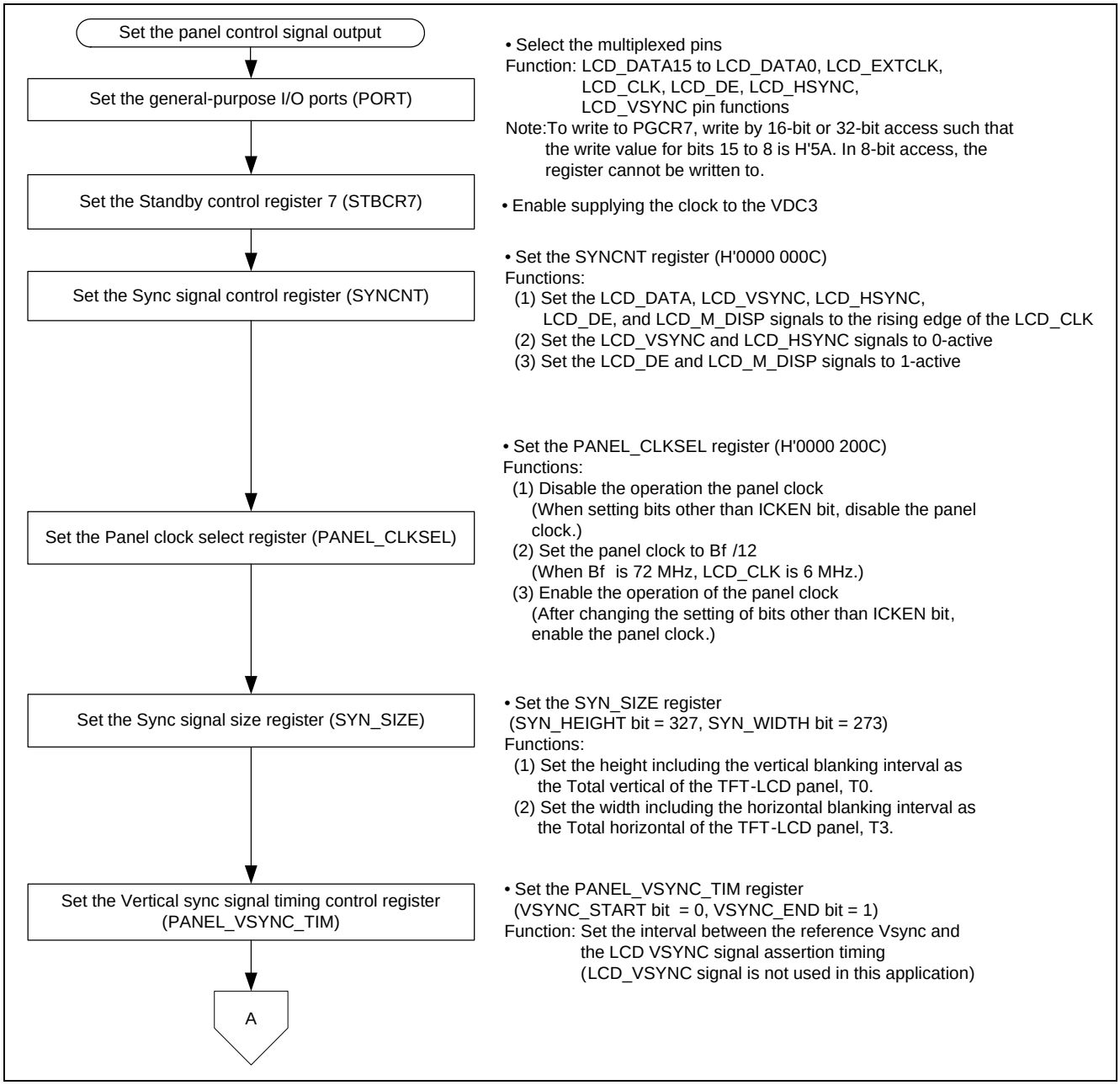


Figure 15 Panel Control Signal Output Setting (1/2)

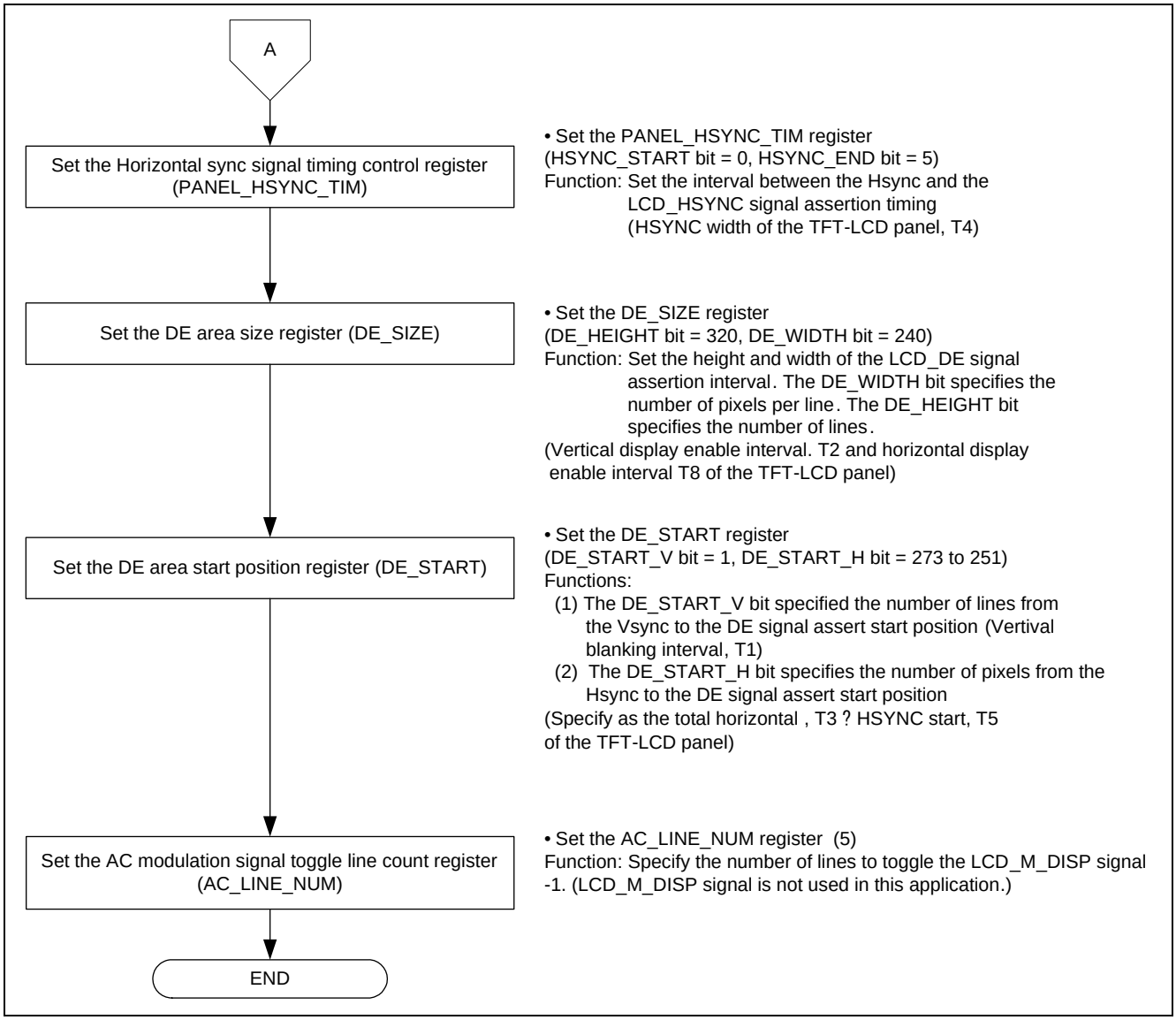


Figure 16 Panel Control Signal Output Setting (2/2)

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "main.c" (1/2)

```
1       /***********************************************************************
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13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
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15      *
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21      *
22      *   Renesas reserves the right, without notice, to make changes to this
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24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ***********************************************************************/
28      /* Copyright (C) 2009(2010,2011) Renesas Electronics Corporation. All Rights Reserved.*/
29      /***********************************************************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : VDC3 video display example
33      *   Version     : 2.00.00
34      *   Device      : SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                              (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40      *   Description :
41      ***********************************************************************
42      *   History     : Jan.30,2009 Ver.1.00.00
43      *               : Jan.14,2010 Ver.1.01.00
44      *               : Feb.28,2011 Ver.2.00.00
45      ***********************************************************************/
46
47
```

3.3 Sample Program Listing "main.c" (2/2)

```
48    /***********************************************************************************
49    Includes  <System Includes> , "Project Includes"
50    ***********************************************************************************/
51    #include <stdio.h>
52    #include "io_vdc3_video_disp.h"
53
54    /***********************************************************************************
55    Exported global variables and functions (to be accessed by other files)
56    ***********************************************************************************/
57    /* ==== Global functions ==== */
58    void main(void);
59
60    /***********************************************************************************
61     * ID           :
62     * Outline      : Video display main
63     * Include      :
64     * Declaration  : void main(void);
65     * Description  : Displays the video in the BT.656 input format on the TFT-LCD panel.
66     * Argument     : void
67     * Return Value : void
68     ***********************************************************************************/
69    void main(void)
70    {
71      /* ==== Initializes the digital video decoder ==== */
72      init_video_decoder();
73
74      /* ==== Initializes the VDC3 ==== */
75      io_vdc3_init();
76
77      while(1){
78        /* loop */
79        }
80
81    }
82
83    /* End of File */
```

3.4 Sample Program Listing "io_vdc3_video_disp.c" (1/7)

```
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9     *
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13    *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14    *   DISCLAIMED.
15    *
16    *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
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21    *
22    *   Renesas reserves the right, without notice, to make changes to this
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24    *   By using this software, you agree to the additional terms and
25    *   conditions found by accessing the following link:
26    *   http://www.renesas.com/disclaimer
27    ***********************************************************************/
28    /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29    /***********************************************************************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : io_vdc3_video_disp.c
32    *   Abstract    : VDC3 video display example
33    *   Version     : 1.00.00
34    *   Device      : SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                              (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40    *   Description :
41    ************************************************************************
42    *   History     : Feb.28,2011 Ver.1.00.00
43    ***********************************************************************/
44
45
```

3.5 Sample Program Listing "io_vdc3_video_disp.c" (2/7)

```
46  /***********************************************************************************
47  Includes  <System Includes> , "Project Includes"
48  ***********************************************************************************/
49  #include "iodefine.h"
50  #include "io_vdc3_video_disp.h"
51
52  /***********************************************************************************
53  Exported global variables and functions (to be accessed by other files)
54  ***********************************************************************************/
55  /* ==== Global functions ==== */
56  void io_vdc3_init(void);
57
58  /* ==== Global variables ==== */
59  #pragma section VLINE_BUFF /* Allocates the buffer at the 128-byte or 16-byte boundary
60                             in cache-disabled space */
61  unsigned short video_line_buffer[VOUT_LINEBUF_NUM][(VOUT_LINE_OFFSET / BYTES_PER_PIXEL)];
62  #pragma section
63
64  /***********************************************************************************
65  Private global variables and functions
66  ***********************************************************************************/
67  /* ==== Private fuctions ==== */
68  static void io_vdc3_init_video_in(void);
69  static void io_vdc3_init_video_out(void);
70  static void io_vdc3_init_disp(void);
71  static void io_vdc3_start(void);
72
```

3.6 Sample Program Listing "io_vdc3_video_disp.c" (3/7)

```
73    /***********************************************************************************
74     * ID           :
75     * Outline      : Initializes the VDC3
76     * Include      :
77     * Declaration  : void io_vdc3_init(void);
78     * Description  : Initializes the VDC3 to display the video.
79     * Argument     : void
80     * Return Value : void
81     ***********************************************************************************/
82    void io_vdc3_init(void)
83    {
84      /* ==== PORT ==== */
85      /* ---- Video (in) ---- */
86      PORT.PFCR1.BIT.PF7MD = 3;       /* DV_DATA7 */
87      PORT.PFCR1.BIT.PF6MD = 3;       /* DV_DATA6 */
88      PORT.PFCR1.BIT.PF5MD = 3;       /* DV_DATA5 */
89      PORT.PFCR1.BIT.PF4MD = 3;       /* DV_DATA4 */
90      PORT.PFCR0.BIT.PF3MD = 3;       /* DV_DATA3 */
91      PORT.PFCR0.BIT.PF2MD = 3;       /* DV_DATA2 */
92      PORT.PFCR0.BIT.PF1MD = 3;       /* DV_DATA1 */
93      PORT.PFCR0.BIT.PF0MD = 3;       /* DV_DATA0 */
94      PORT.PECR1.BIT.PE5MD = 3;       /* DV_HSYNC */
95      PORT.PECR1.BIT.PE4MD = 3;       /* DV_VSYNC */
96      PORT.PFCR2.BIT.PF8MD = 3;       /* DV_CLK */
97
98      /* ---- Display (out) ---- */
99      PORT.PGCR7.WORD = 0x5A01u;      /* LCD_DATA0 ( Bits 15 to 8 is H'5A. )*/
100     PORT.PGCR5.BIT.PG20MD= 1;       /* LCD_EXTCLK */
101     PORT.PGCR4.WORD = 0x1111u;      /* LCD_CLK, LCD_DE, LCD_HSYNC, LCD_VSYNC */
102     PORT.PGCR3.WORD = 0x1111u;      /* LCD_DATA15-12 */
103     PORT.PGCR2.WORD = 0x1111u;      /* LCD_DATA11-08 */
104     PORT.PGCR1.WORD = 0x1111u;      /* LCD_DATA07-04 */
105     PORT.PGCR0.BIT.PG3MD = 1;       /* LCD_DATA03 */
106     PORT.PGCR0.BIT.PG2MD = 1;       /* LCD_DATA02 */
107     PORT.PGCR0.BIT.PG1MD = 1;       /* LCD_DATA01 */
108
109     /* ==== CPG ==== */
110     CPG.STBCR7.BIT.MSTP74 = 0;      /* VDC3 */
111
112     /* ==== VDC3 ==== */
113     /* ---- Initializes the video receiving block ---- */
114     io_vdc3_init_video_in();
115
116     /* ---- Initializes the video supplying block ---- */
117     io_vdc3_init_video_out();
118
119     /* ---- Initializes the panel control block and output timing control block ---- */
120     io_vdc3_init_disp();
121
122     /* ---- Enables the operation ---- */
123     io_vdc3_start();
124   }
```

3.7 Sample Program Listing "io_vdc3_video_disp.c" (4/7)

```
125
126  /***********************************************************************************
127   * ID           :
128   * Outline      : Initializes the video receiving block
129   * Include      : iodefine.h
130   * Declaration  : static void io_vdc3_init_video_in(void);
131   * Description  : Initializes the video receiving block.
132   *              : BT.656 is used as the input video format.
133   * Argument     : void
134   * Return Value : void
135   ***********************************************************************************/
136  static void io_vdc3_init_video_in(void)
137  {
138    /* ----Input video format setting ---- */
139    VDC3.VIDEO_MODE.BIT.SEL_EXSYNC = 0;            /* Disables the external input
140                                                      sync signal */
141    VDC3.VIDEO_MODE.BIT.SEL_656601 = 0;            /* Specifies the BT.656 input */
142    VDC3.VIDEO_MODE.BIT.SEL_525625 = 0;            /* Number of lines for the
143                                                      input video: 525 (NTSC) */
144    VDC3.VIDEO_TIM_CNT.LONG    = 0x00000000ul; /* Latches the DV_DATA input
145                                                      signal at the rising edge */
146                                              /* Other control signals settings
147                                                      are not required for the BT656) */
148  }
149
150  /***********************************************************************************
151   * ID           :
152   * Outline      : Initializes the video supplying block
153   * Include      : iodefine.h
154   * Declaration  : static void io_vdc3_init_video_out(void);
155   * Description  : Initializes the video supplying block.
156   *              : BT.656 is used as the input video format.
157   * Argument     : void
158   * Return Value : void
159   ***********************************************************************************/
160  static void io_vdc3_init_video_out(void)
161  {
162    /* ---- Video display function setting (NTSC, BT.656) ---- */
163    VDC3.VIDEO_MODE.BIT.BURST_MODE_DISP = 0;       /* Bus in the video supplying block:
164                                                      16-byte burst transfer */
165    VDC3.VIDEO_MODE.BIT.BURST_MODE_MAIN = 0;       /* Bus in the video receiving block:
166                                                      16-byte burst transfer */
167    VDC3.VIDEO_MODE.BIT.ENDIAN_DISP     = 0;       /* Bus in the video supplying block:
168                                                      big endian */
169    VDC3.VIDEO_MODE.BIT.ENDIAN_MAIN     = 0;       /* Bus in the video receiving block:
170                                                      big endian */
171    VDC3.VIDEO_MODE.BIT.VIDEO_MODE      = 1;       /* Specifies the video display function */
172    VDC3.VIDEO_INT_CNT.LONG             = 0x00000000ul;/* Disables video interrupts */
173    VDC3.VIDEO_SIZE.BIT.VIDEO_HEIGHT    = VIN_INPUT_HEIGHT;
174    VDC3.VIDEO_SIZE.BIT.VIDEO_WIDTH     = VIN_INPUT_WIDTH;
175                                            /* Specifies the number of lines
176                                                      and pixels of the valid video */
```

3.8 Sample Program Listing "io_vdc3_video_disp.c" (5/7)

```
177     VDC3.VIDEO_VSTART.BIT.VIDEO_VSTART_TOP = VIN_VSTART_VALIDDATA_TOP;
178     VDC3.VIDEO_VSTART.BIT.VIDEO_VSTART_BTM = VIN_VSTART_VALIDDATA_BTM;
179     VDC3.VIDEO_HSTART.BIT.VIDEO_HSTART     = VIN_HSTART_VALIDDATA;
180                                             /* Vertical start position of the
181                                                valid video in the TOP field
182                                                Vertical start position of the
183                                                valid video in the BOTTOM field
184                                                Horizontal start position of the
185                                                valid video */
186     VDC3.VIDEO_VSYNC_TIM1.BIT.VIDEO_VSYNC_START1_TOP
187      = VIN_VSTART_VALIDDATA_TOP+VOUT_IO_DFLINE-TFT_DE_START_V+(VOUT_BUF_MARGIN/2)-
    VOUT_DISP_POS_IO_DF;
188     VDC3.VIDEO_VSYNC_TIM1.BIT.VIDEO_VSYNC_START1_BTM
        = VIN_VSTART_VALIDDATA_BTM+VOUT_IO_DFLINE-TFT_DE_START_V+(VOUT_BUF_MARGIN/2)-
189   VOUT_DISP_POS_IO_DF;
190                                             /* Specifies the reference Vsync position
191                                                in the TOP field and BOTTOM field */
192     VDC3.VIDEO_SAVE_NUM.BIT.FIELD_SAVE_NUM  = 0;    /* Number of fields to store (Set to 0
193                                                in the video display function)*/
194     VDC3.VIDEO_IMAGE_CNT.LONG = 0x80800311ul;       /* Luminance contrast not adjusted */
195                                             /* Luminance brightness not adjusted */
196                                             /* Luminance clipping is valid */
197                                             /* Chrominance clipping is valid */
198                                             /* Scales down vertically to 1/3 */
199                                             /* Scales down horizontally to 1/3 */
200     VDC3.VIDEO_BASEADR.LONG         = (unsigned long)video_line_buffer;
201     VDC3.VIDEO_LINE_OFFSET.LONG     = VOUT_LINE_OFFSET;
202     VDC3.VIDEO_FIELD_OFFSET.LONG        = 0;        /* Field offset (Disabled in the video
203                                                disable function) */
204     VDC3.VIDEO_LINEBUFF_NUM.BIT.VIDEO_LINEBUFF_NUM = VOUT_LINEBUF_NUM;
205                                             /* Specifies the line buffer address,
206                                                line offset (Number of bytes per line),
207                                                and the number of lines to use */
208     VDC3.VIDEO_DISP_SIZE.BIT.VIDEO_DISP_HEIGHT   = VOUT_DISP_SZ_Y;
209     VDC3.VIDEO_DISP_SIZE.BIT.VIDEO_DISP_WIDTH    = VOUT_DISP_SZ_X;
210     VDC3.VIDEO_DISP_HSTART.BIT.VIDEO_DISP_HSTART = (TFT_DE_START_H-16);
211                                             /* Specifies the vertical and
212                                                horizontal size, horizontal start
213                                                position of the video */
214     VDC3.SGMODE.BIT.EX_SYNC_MODE= 1;            /* Synchronizes the reference Vsync
215                                                with the Vsync for video input */
216     VDC3.VIDEO_VSYNC_TIM2.LONG      = (TFT_DE_START_V + VOUT_DISP_POS_Y - 1);
217                                             /* Specifies the timing of the Vsync
218                                                for video display */
219   }
220
```

3.9 Sample Program Listing "io_vdc3_video_disp.c" (6/7)

```
/*****************************************************************************
 * ID           :
 * Outline      : Initializes the panel control block and output timing control block
 * Include      : iodefine.h
 * Declaration  : static void io_vdc3_init_disp(void);
 * Description  : Initializes the panel control block and output timing control block.
 * Argument     : void
 * Return Value : void
 *****************************************************************************/
static void io_vdc3_init_disp(void)
{
  /* ---- TFT-LCD panel control signal output setting ---- */
  VDC3.SYNCNT.LONG = 0x0000000Cul;               /* Outputs all signals at the
                                                    rising edge */
                                                /* LCD_VSYNC/LCD_HSYNC signal:
                                                    output is inverted */
  VDC3.PANEL_CLKSEL.BIT.ICKEN = 0;              /* Disables the operation of
                                                    the panel clock */
  VDC3.PANEL_CLKSEL.LONG      = 0x0000200Cul;   /* Clock source: Bφ (72 MHz) */
                                                /* Clock frequency: 6 MHz */
  VDC3.PANEL_CLKSEL.BIT.ICKEN = 1;              /* Enables the operation of
                                                    the panel clock */
  VDC3.SYN_SIZE.BIT.SYN_HEIGHT= TFT_TOTAL_SZ_V; /* Number of lines including the
                                                    vertical blanking interval */
  VDC3.SYN_SIZE.BIT.SYN_WIDTH = TFT_TOTAL_SZ_H; /* Number of pixels including the
                                                    horizontal blanking interval */
  VDC3.PANEL_VSYNC_TIM.LONG   = TFT_VSYNC_WDTH; /* Sets the timing for the
                                                    panel output VSYNC */
  VDC3.PANEL_HSYNC_TIM.LONG   = TFT_HSYNC_WDTH; /* Sets the timing for the
                                                    panel output HSYNC */
  VDC3.DE_SIZE.BIT.DE_HEIGHT  = TFT_DISP_SZ_V;  /* Number of lines for the DE area */
  VDC3.DE_SIZE.BIT.DE_WIDTH   = TFT_DISP_SZ_H;  /* Number of pixels for the DE area */
  VDC3.DE_START.BIT.DE_START_V= TFT_DE_START_V; /* DE area start position in
                                                    the vertical direction */
  VDC3.DE_START.BIT.DE_START_H= TFT_DE_START_H; /* DE area start position in
                                                    the horizontal direction */
}

```

3.10 Sample Program Listing "io_vdc3_video_disp.c" (7/7)

```
/*****************************************************************************
 * ID           :
 * Outline      : Enables the operation
 * Include      : iodefine.h
 * Declaration  : static void io_vdc3_start(void);
 * Description  : Enables the operation.(Enabled from the next Vsync)
 * Argument     : void
 * Return Value : void
 *****************************************************************************/
static void io_vdc3_start(void)
{
  /*  ---- Enables the video receiving block  ---- */
  VDC3.VIDEO_MODE.BIT.VIDEO_MAIN_EXE  = 1;

  /*  ---- Enables the video supplying block  ---- */
  VDC3.VIDEO_MODE.BIT.VIDEO_DISP_EXE  = 1;

  /*  ---- Enables the graphics block 2  ---- */
  VDC3.GRCMEN2.LONG = 0x80000001ul;   /* Disables to display the current graphics,
                                         enables to display the lower-layer graphics */

  /*  ---- Enables the graphics block 1  ---- */
  VDC3.GRCMEN1.LONG = 0x80000001ul;   /* Disables to display the current graphics,
                                         enables to display the lower-layer graphics */

}
/* End of File */
```

3.11 Sample Program Listing "io_vdc3_video_disp.h" (1/3)

```
1     /***********************************************************************
2     *   DISCLAIMER
3     *
4     *   This software is supplied by Renesas Electronics Corporation and is only
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6     *
7     *   This software is owned by Renesas Electronics Corporation and is protected under
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9     *
10    *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
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12    *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13    *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
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15    *
16    *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
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24    *   By using this software, you agree to the additional terms and
25    *   conditions found by accessing the following link:
26    *   http://www.renesas.com/disclaimer
27    ***********************************************************************/
28    /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29    /***********************************************************************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : io_vdc3_video_disp.h
32    *   Abstract    : VDC3 video display example
33    *   Version     : 1.00.00
34    *   Device      : SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                              (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40    *   Description :
41    ************************************************************************
42    *   History     : Feb.28,2011 Ver.1.00.00
43    ***********************************************************************/
44
45
```

3.12 Sample Program Listing "io_vdc3_video_disp.c" (2/3)

```
46  /***********************************************************************************
47  Macro definitions
48  ***********************************************************************************/
49  #define BYTES_PER_PIXEL       2       /* Number of bytes per pixel */
50  #define RGB565_BLACK          0x0000u /* Black */
51  #define RGB565_WHITE          0xFFFFu /* White */
52  #define RGB565_GREEN          0x07E0u /* Green */
53  #define RGB565_BLUE           0x001Fu /* Blue */
54
55  /* ---- Video input parameters ---- */
56  #define VIN_VSTART_VALIDDATA_TOP 16       /* Vertical capture timing in the TOP field */
57  #define VIN_VSTART_VALIDDATA_BTM 279  /* Vertical capture timing in the BOTTOM field */
58  #define VIN_HSTART_VALIDDATA  276     /* Horizontal capture timing */
59  #define VIN_INPUT_HEIGHT      240     /* Number of lines of the input valid video */
60  #define VIN_INPUT_WIDTH       720     /* Number of pixels of the input valid video */
61
62  /* ---- Video output parameters ---- */
63  #define VOUT_DISP_SZ_Y        160     /* Video display area height */
64  #define VOUT_DISP_SZ_X        240     /* Video display area width */
65  #define VOUT_BUF_MARGIN       6       /* Line buffer margin (specify 6 or greater) */
66  #define VOUT_IO_DFLINE        127     /* Difference in number of lines between
67                                           the input cycle and display cycle */
68                                        /*  = VIN_INPUT_HEIGHT -(VOUT_DISP_SZ_Y *
69  (0.045/0.064))*/
70  #define VOUT_LINEBUF_NUM      (VOUT_IO_DFLINE + VOUT_BUF_MARGIN)
71                                        /* Number of lines of line buffer */
72  #define VOUT_LINE_OFFSET      (((VOUT_DISP_SZ_X * BYTES_PER_PIXEL) + 15 ) & 0xFFFFFFF0ul)
73                                        /* Number of bytes per line */
74  #define VOUT_DISP_POS_Y       80      /* Vertical start position of the video
75                                        (from the top of the panel) */
76  #define VOUT_DISP_POS_X       0       /* Horizontal start position of the video
77                                            (from the leftmost of the panel) */
78  #define VOUT_DISP_POS_IO_DF   56      /* Converted value of the VD_DISP_POS_Y
79                                            to the number of lines of the input video */
80                                        /*  = VOUT_DISP_POS_Y * (0.045/0.064) */
81
82  /* ---- TFT-LCD panel parameters ---- */
83  #define TFT_TOTAL_SZ_V        327     /* Number of lines including the vertical
84                                            blanking interval */
85  #define TFT_TOTAL_SZ_H        273     /* Number of pixels including the horizontal
86                                            blanking interval */
87  #define TFT_DISP_SZ_V         320     /* Vertical display enable interval */
88  #define TFT_DISP_SZ_H         240     /* Horizontal display enable interval */
89  #define TFT_VSYNC_WDTH        1       /* LCD_VSYNC pulse width (number of lines) */
90  #define TFT_HSYNC_WDTH        5       /* LCD_HSYNC pulse width (number of pixels) */
91  #define TFT_DE_START_V        1       /* Number of lines between the reference Vsync
92                                            and the enable interval */
93  #define TFT_DE_START_H        (TFT_TOTAL_SZ_H - 251)
94                                        /* Number of pixels between the reference
95                                            Hsync and the enable interval */
```

3.13 Sample Program Listing "io_vdc3_video_disp.c" (3/3)

```
96    /***********************************************************************************
97    Imported global variables and functions (from other files)
98    ***********************************************************************************/
99    /* ==== Global functions ==== */
100   extern void io_vdc3_init(void);
101
102   /* ==== Global variables ==== */
103   extern unsigned short video_line_buffer[VOUT_LINEBUF_NUM][(VOUT_LINE_OFFSET /
104   BYTES_PER_PIXEL)];
105
106   /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev.3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware manual Rev.2.00
  The latest version of the hardware manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.14.09	—	First edition issued
1.01	Jan.19.10	21	Figure 15, Note added
		23	Supplement to the sample program added for 640-KB RAM
		28	Writing procedure to the PGCR7 updated
		24 to 31	Format for header comments updated
1.02	Mar.23.11	19 to 35	Changed the configuration of the source code

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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