SH7262/SH7264 Group

SDRAM Interface Setting

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Summary

This application note describes how to connect the SH7264 microcomputers (MCUs) to SDRAM using Bus State Controller SDRAM interface.

Target Device

SH7262/7264 MCU (In this document, SH7262/SH7264 are described as SH7264.)

Contents

1. Introduction

1.1 Specifications

- Uses a 16-MB (8 Mwords × 16 bits) SDRAM to connect with the SH7264 in 16-bit bus wide
- Configures theSH7264 Bus State Controller to access SDRAM, and initializes the SDRAM using the SH7264 Bus State Controller SDRAM Interface

1.2 Modules Used

- Bus State Controller

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequencies	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Electronics Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug-gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

- SH7262/SH7264 Group Example of Initialization

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application uses the SH7264 Bus State Controller to configure the SH7264 to control an external SDRAM.

2.1 Bus State Controller Operation

The SH7264 Bus State Controller outputs control signals to memory devices and other external devices connected to external address space, which allows the MCU to connect external memory devices such as SRAM, SDRAM, and other external devices directly.

Table 1 lists the features of the Bus State Controller. Table 2 lists the features of the Bus State Controller SDRAM interface.

Table 1 Bus State Controller Features

Item	Description
Target space	Supports seven spaces from CS0 to CS6, up to 64 MB per space
Memory options	Following memory spaces can be specified: • Normal space interface • SRAM interface with byte selection • Burst ROM (clock synchronous or asynchronous) • MPX-I/O • SDRAM interface • PCMCIA interface
Data bus width	Specify CS0 space data bus in 16-bit wide. 8- or 16- bit can be specified per space for CS1 to CS6 spaces
Wait control	Controls to insert wait state cycles per space
Idle control	Specifies idle cycles independently during the sequential access: • In read-write in the same space • In read-write in different spaces • In read-read in the same space • In read-read in different spaces, or • When the first cycle is the write cycle

Table 2 SDRAM Interface Features

Item	Description
Target space	SDRAM can be specified in up to two spaces (CS2 and CS3 spaces) Use CS3 space when connecting SDRAM to one space
Address output	Supports address multiplexing (row address and column address) Row address: 11 to 13 bits, column address: 8 to 10 bits
Burst length	Fixed to 1 When accessing data larger than the SDRAM data bus width sequentially, access the data in burst length of 1 as many times as needed
Precharge control	Supports auto-precharge mode, and bank active mode (note)
Refresh control	Supports auto-refresh, and self-refresh
Other	Supports low frequency mode, power-down mode Supports to issue commands MRS and EMRS

Note: Bank active mode is available in CS3 space only.

Figure 1 shows the block diagram of the Bus State Controller.

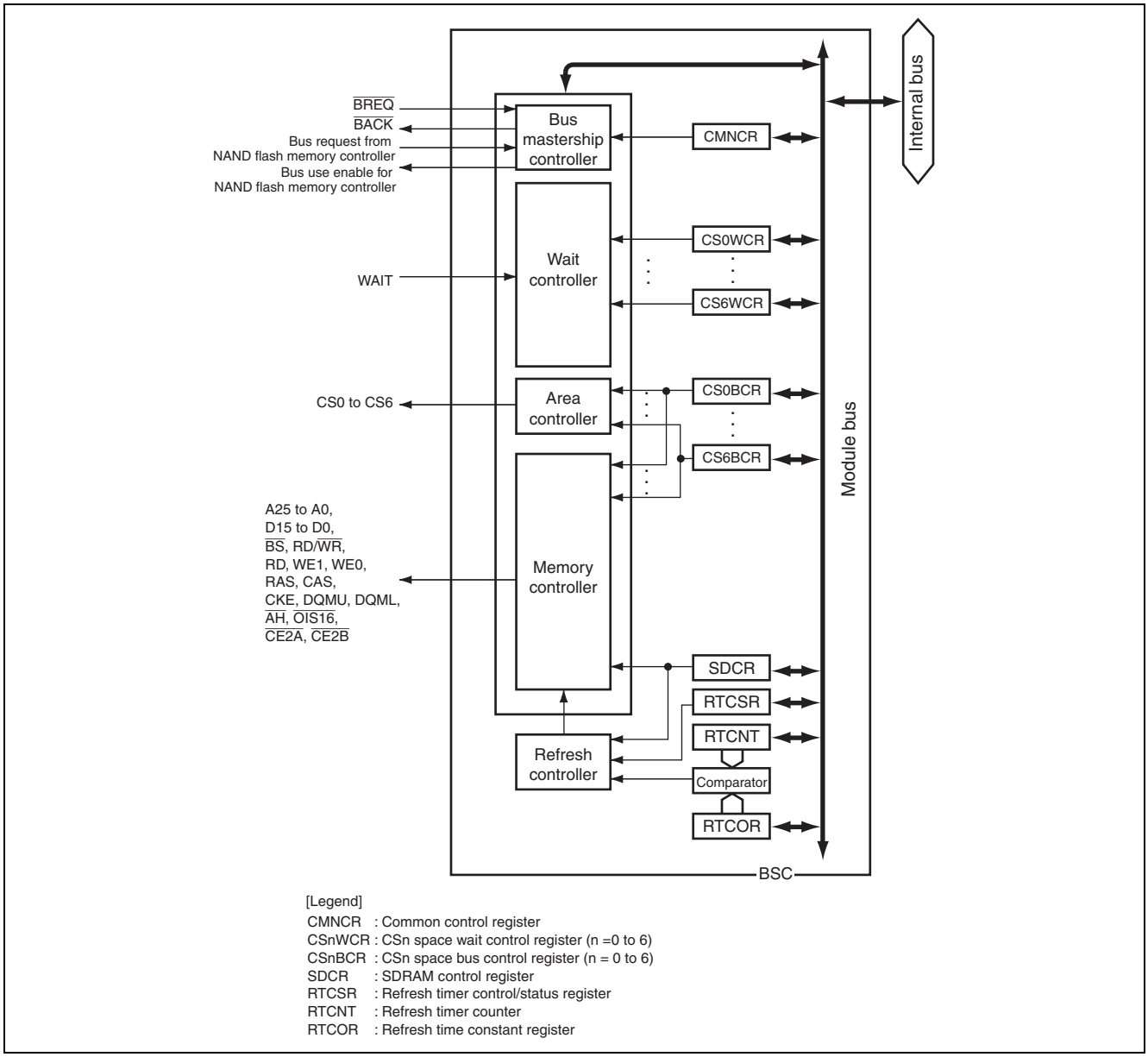


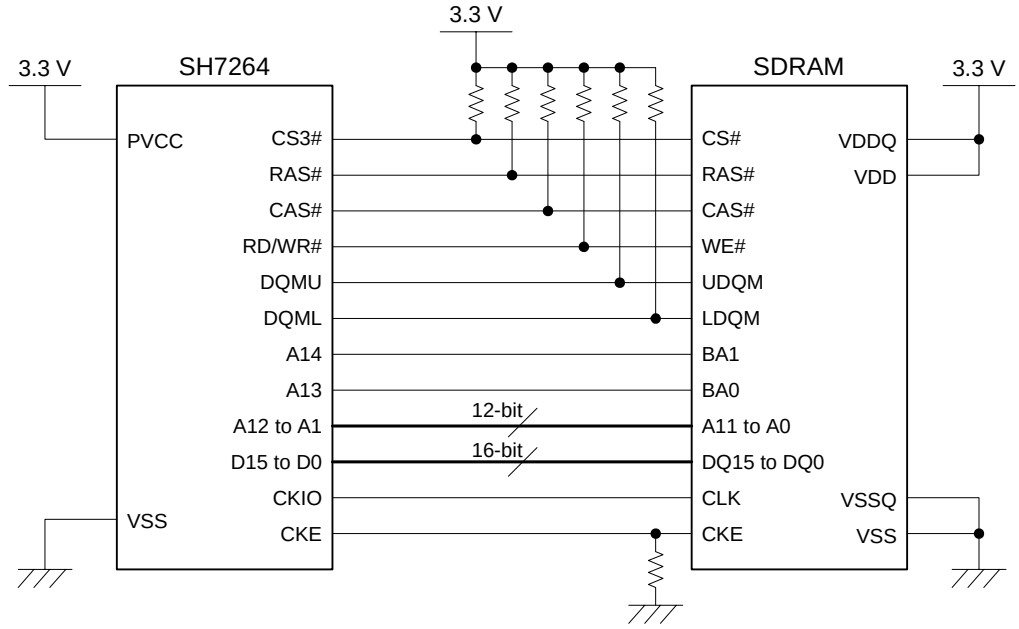
Figure 1 Bus State Controller Block Diagram

2.2 Interfacing Example

Table 3 lists the specifications of the SDRAM used in this application. Figure 2 shows the connection between the SDRAM and the SH7264. Figure 3 shows memory map related to the SDRAM.

Table 3 SDRAM Specifications

Item	Description
Part number	EDS1216AHTA-75E
Density, organization	128 Mbits (2 Mwords × 16 bits × 4 banks): 1
Data bus width	16-bit
Address configuration	Bank address: 2-bit, row address: 12-bit, column address: 9-bit
Refresh cycle	4096 cycles every 64 ms
CAS latency	2 or 3
Operating voltage	3.3 V ± 0.3 V



Note: Damping resistors on signals lines are not included. Install them according to the system configuration.

Figure 2 SDRAM Connection

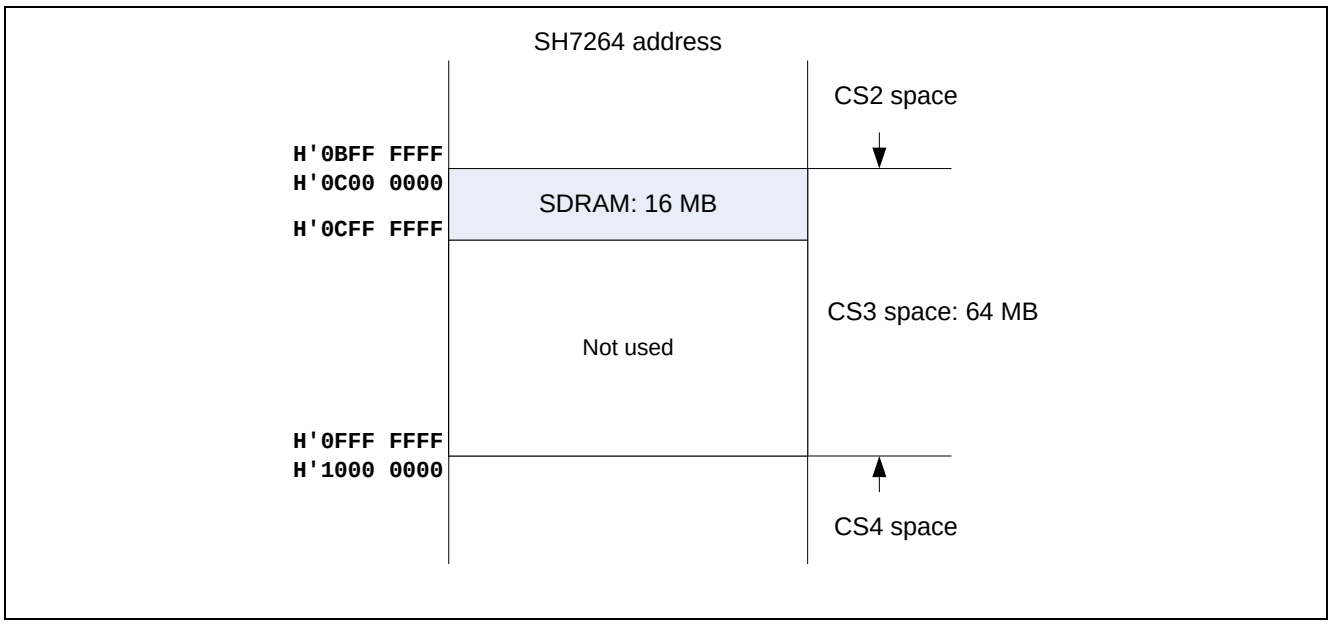


Figure 3 Memory Map associated with the SDRAM

Note: Pull up or pull down the control signal pins using the external resistors

Pins CKE, CS3#, RAS#, CAS#, RD/WR#, DQMU, and DQML are configured as I/O ports as default, change the pin functions by the general-purpose I/O ports.

As the SH7264 I/O ports are configured as input as default, its state is undefined. Pull-up or pull-down is recommended to avoid improper operation of the SDRAM.

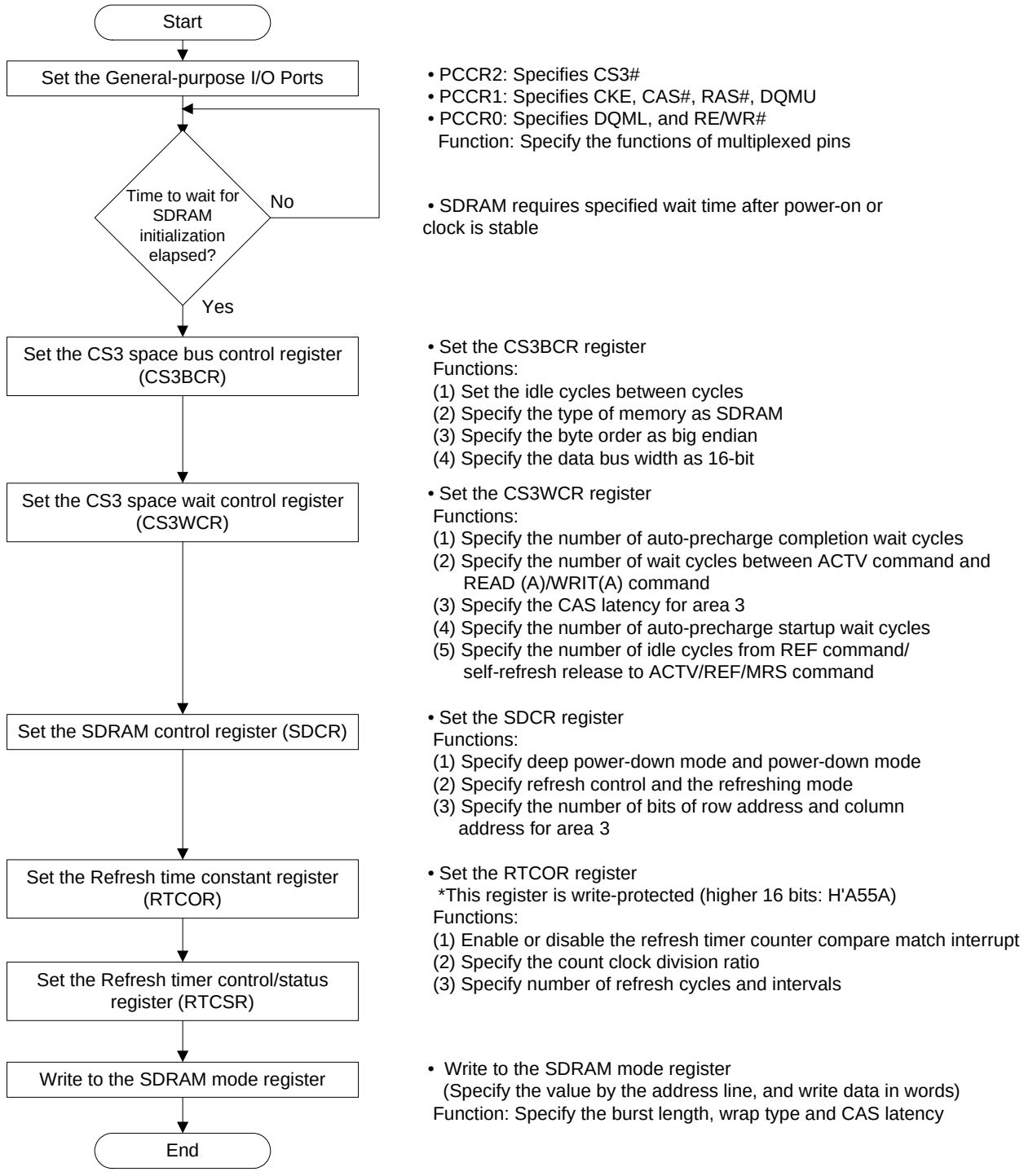
In general, control signals will be undefined during the RESET period before the BSC is initialized, so to get more stable memory operation, pull up pins CS3#, RAS#, CAS#, RD/WR#, DQMU, and DQML to high level using external resistors.

Pull-down is also recommended on the CKE pin using an external resistor, supposing that the SDRAM continues to self-refreshing to save data after the signal from the MCU is stopped.

How to configure SDRAM pins depends on the type of the SDRAM. For more information, refer to the SDRAM datasheet provided by the manufacturer.

2.3 Setting Procedure

Figure 4 shows the initializing procedure when connecting SDRAM with the SH7264 CS3 space.



Note: Do not acess SDRAM before setting the BSC is completed.

Figure 4 Bus State Controller and General-purpose I/O Port Setting Procedure (CS3 Space)

2.3.1 AC Characteristics Switching Procedure

To connect the SDRAM to the SH7264 MCU, use the AC characteristics switching function by specifying the AC characteristics switching register (ACSWR) and AC characteristics switching key register (ACKEYR).

Figure 5 shows the setting example of the AC characteristics switching register (ACSWR). Make sure to specify this register on the internal RAM.

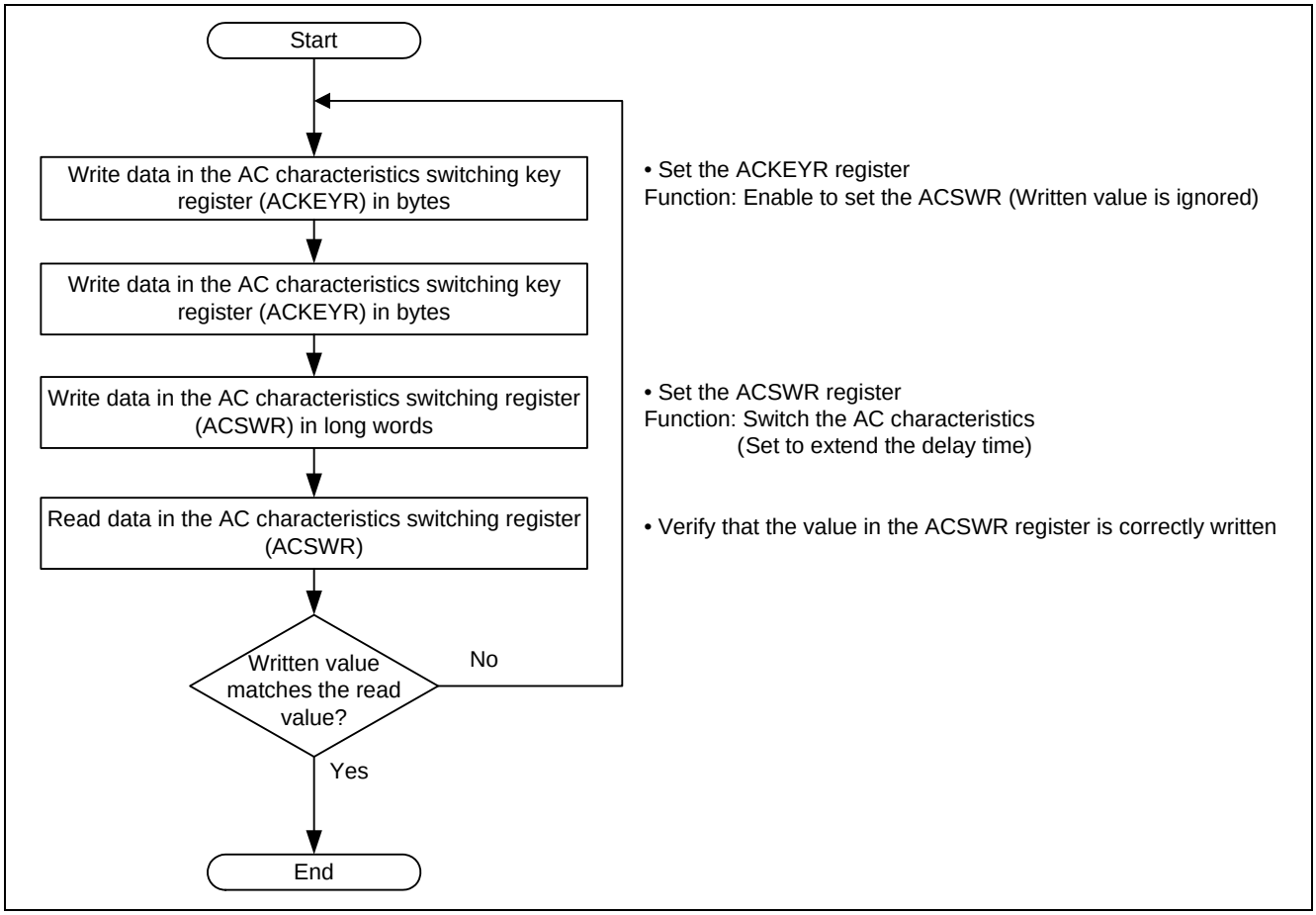


Figure 5 Example of the AC Characteristics Switching Procedure

2.3.2 Power-on Sequence

To initialize the SDRAM, set the BSC (Bus State Controller) registers and then write to the SDRAM mode register.

SDRAM requires a certain period of idle time after power on. This application sets at least 200-µs idle time by software. As the required idle time depends on the type of the SDRAM, refer to the SDRAM datasheet.

When writing to the SDRAM mode register, issue the mode register set command (MRS) by combination of CS3#, RAS#, CAS#, and RD/WR# to use its address as the input data to SDRAM. Table 4 lists access address when writing to the SDRAM mode register in CS3 space.

Table 4 Access Address When Writing to the SDRAM Mode Register (CS3 Space)

Data bus width	CAS latency	Burst read/ single write (Burst length is 1)		Burst read/ burst write (Burst length is 1)	
		Access address	External address pin	Access address	External address pin
16-bit	2	H'FFFC 5440	H'0000 0440	H'FFFC 5040	H'0000 0040
	3	H'FFFC 5460	H'0000 0460	H'FFFC 5060	H'0000 0060

This application set the SDRAM mode registers as follows;

- Burst length: burst read/single write (burst length: 1)
- Wrap type: sequential
- CAS latency: 2 cycles

As listed in Table 4, write desired data in words to the address H'FFFC 5040 to set the SDRAM mode register. (The write data is ignored). This operation issues the following commands to the SDRAM sequentially.

1. Issue the all bank pre-charge command (PALL)
   The PALL command is issued to insert the number of idle cycles (Tpw) specified by WTRP [1:0] bits in the CS3WCR between the PALL and the first REF.
2. Issue eight auto refresh commands (REF)
   The REF command is issued to insert the number of idle cycles (Trc) specified by WTRC [1:0] bits in the CS3WCR between (a) the REF and the REF, and (b) the REF and the MRS. Repeat to issue the REF command for eight times.
3. Issue the mode register set command (MRS)

2.4 Bus State Controller and General-purpose I/O Ports Setting

Table 5 lists an example to set the Bus State Controller. Table 6 lists an example to set the General-purpose I/O ports (related setting to the SDRAM connection). For details on registers, refer to Chapter 9 Bus State Controller (BSC) and Chapter 32 General-purpose I/O Ports in the SH7262 Group, SH7264 Group Hardware Manual.

Table 5 BSC Setting

Register Name	Address	Value	Description
CS3 space bus control register (CS3BCR)	H'FFFC 0010	H'0000 4400	• IWW [2:0] = "B'000" No idle cycles between Write-Read cycles and Write-Write cycles • IWRWD [2:0], IWRWS [2:0] = "B'000" No idle cycles between Read-Write cycles • IWRRD [2:0], IWRRS[2:0] = "B'000": No idle cycles between Read-Read cycles • TYPE [2:0] = "B'100": SDRAM • ENDIAN = "0": Big endian • BSZ [1:0] = "B'10": 16-bit data bus wide
CS3 space wait control register (CS3WCR)	H'FFFC 0034	H'0000 288A	• WTRP [1:0] = "B'01": Number of Auto-precharge completion wait cycles: 1 • WTRCD [1:0] = "B'10": Number of wait cycles between ACTV command and READ(A)/WRIT(A) command: 2 • A3CL [1:0] = "B'01": CAS latency for Area 3: 2 • TRWL [1:0] = "B'01": Number of Auto-precharge startup wait cycles: 1 • WTRC[1:0] = "B'10": Number of idle cycles from REF command/self-refresh release to ACTV/REF/MRS command: 5
SDRAM control register (SDCR)	H'FFFC 004C	H'0000 0809	• RFSH = "1": Refresh the SDRAM • RMODE = "0": Auto-refresh the SDRAM • BACTV = "0": Bank active mode: Auto-precharge mode • A3ROW [1:0] = "B'01": Number of bits of row address for Area 3: 12 • A3COL [1:0]="B'01": Number of bits of column address: 9
Refresh timer control/status register (RTCSR)	H'FFFC 0050	H'A55A 0010	• CMIE = "0": Compare match interrupt enable: Disable request to interrupt by the CMF • CKS [2:0] = "B'010": Clock select: Bφ/16 • RRC [2:0] = "B'000": Number of refresh cycles: 1
Refresh time constant register (RTCOR)	H'FFFC 0058	H'A55A 0046	• SDRAM refresh request interval is as follows; 1 cycle: 222 ns (72 MHz/16 = 4.5 MHz) Request interval: 15.625 µs/time (4096 refresh cycles every 64 ms) 15.625 µs ÷ 222 ns = 70 cycles (0×46)

Table 6 General-purpose I/O Ports Setting (Items Related to the SDRAM Connection)

Register Name	Address	Setting	Description
Port C control register 2 (PCCR2)	H'FFFE 384A	H'0001	• PC8MD [1:0] = "B'01": Specify PC8 pin as CS3#
Port C control register 1 (PCCR1)	H'FFFE 384C	H'1111	• PC7MD [1:0] = "B'01": Specify PC7 pin as CKE • PC6MD [1:0] = "B'01": Specify PC6 pin as CAS# • PC5MD [1:0] = "B'01": Specify PC5 pin as RAS# • PC4MD = "1": Specify PC4 pin as DQMU
Port C control register 0 (PCCR0)	H'FFFE 384E	H'1111	• PC3MD = "1": Specify PC3 pin as DQML • PC2MD = "1": Specify PC2 pin as RD/WR#

2.5 SDRAM Timing Setting Example

When connecting an SDRAM, set the access speed to SDRAM (CAS latency), wait cycles depending on the AC characteristics, and SDRAM refresh cycles to the SH7264. This section describes key points to set wait cycles and refresh cycles.

The SH7264 operates at bus clock 50 MHz (tcyc = 20 ns), and uses auto-precharge mode to access SDRAM.

For AC characteristics of the SH7264 and SDRAM, refer to the datasheet. The SDRAM operates at the rising edge of the CKIO.

2.5.1 Access Wait Cycle

(1) Specify the wait cycle (Trw) between cycles Tr and Tc in WTRCD [1:0] bits in the CS3WCR register.
(2) Specify the wait cycle (Tcw) between cycles Tc and Td in A3CL [1:0] bits in the CS3WCR register. The number of the Tcw cycle is equal to the number of the CAS latency cycle −1.
(3) Specify the wait cycle (Tap/Tpw) until the precharge is completed in WTRP [1:0] bits in the CS3WCR register.
(4) Specify the wait cycle (Trwl) before the auto-precharge is activated in TRWL [1:0] bits in the CS3WCR register.
Make sure that the above settings satisfy the bus timings both for the SH7264 and SDRAM.
Tr, Tcn (n = 1 to 8), Tdn (n = 1 to 8), and Tde used in the following formula equal "tcyc".

- SDRAM tRC (Ref/Active to Ref/Active command period, read cycle)
  tRC (min.) ≤ (tcyc × Trw) + (Tc1) + (tcyc × Tcw) + (Td1) + (Tde) + (tcyc × Tap) + (Tr) .....Figure 6

Note: Tr = Tc = Tdn = Tde = tcyc

- SDRAM tRC (Ref/Active to Ref/Active command period, write cycle)
  tRC (min.) ≤ (tcyc × Trw) + (Tc1) + (tcyc × Trwl) + (tcyc × Tap) + (Tr) .....Figure 8

- SDRAM tRAS (Active to Precharge command period)
  tRAS (min.) ≤ (tcyc × Trw) + (Tc1) + (tcyc × Tcw) .....Figure 6

- SDRAM tRCD (Active command to column command)
  tRCD (min.) ≤ (tcyc × Trw) + (Tc1) .....Figure 6

- SDRAM tRP (Precharge to active command period, read cycle)
  tRP (min.) ≤ (tcyc × (Tcw − 1)) + (Td1) + (Tde) + (tcyc × Tap) + (Tr) .....Figure 6

- SDRAM tRP (Precharge to active command period, write cycle)
  tRP(min) ≤ (tcyc × Tap) + (Tr) .....Figure 8

- SDRAM tDAL (Last data into active latency)
  tDAL (min.) ≤ (tcyc ×Trwl) + (tcyc × Tap) + (Tr) .....Figure 8

- SDRAM tRP (Precharge to active command period, auto-refresh)
  tRP (min.) ≤ (tcyc × Tpw) + (Trr) .....Figure 10

Note: Tpw = Tap

2.5.2 Refresh Cycle

(1) Specify the period to refresh the SDRAM (tREF) in registers RTCSR and RTCOR.
(2) Specify the wait cycle for the auto-refresh cycle in WTRC [1:0] bits in the CS3WCR register.
Make sure that the above settings satisfy the bus timing both for the SH7264 and SDRAM.

- SDRAM tREF (Refresh period)
  tREF (max.) ≥ tcyc × CKS × RTCOR × Ref_Cyc

Note: The Ref_Cyc in the above formula indicates the number of refresh cycles, which is 4096 in this example. tcyc × CKS indicates the clock frequency of the refresh counter. "tcyc × CKS" multiplied by the RTCOR value is the interval between SDRAM refresh cycles.

Reference:

Assume that tcyc = 13.9 ns, CKS = 16, RTCOR = 70, and Ref_Cyc = 4096,

- Refresh counter clock frequency: tcyc × CKS = 222 (ns)
- Interval between SDRAM refresh cycles: tcyc × CKS × RTCOR = 15.54 (µs)
- Refresh period for 4096 refresh cycles: tcyc × CKS × RTCOR × Ref_Cyc = 63.65 (ms)

- SDRAM tRC (Refresh cycle)
  tRC (min.) ≤ (tcyc × Trc) (Tr) .....Figure 9

Note: Tr = tcyc

Figure 6 shows the SDRAM single read timing example. Figure 7 shows the SDRAM burst read timing example. Figure 8 shows the SDRAM single write timing example. Figure 9 shows the SDRAM burst write timing example. Figure 10 shows the SDRAM auto-refresh timing example. These examples set bits WTRP [1:0] as B'00, WTRCD [1:0] as B'01, A3CL [1:0] as B'01, TRWL [1:0] as B'10, and WTRC [1:0] as B'01 in the CS3WCR register.

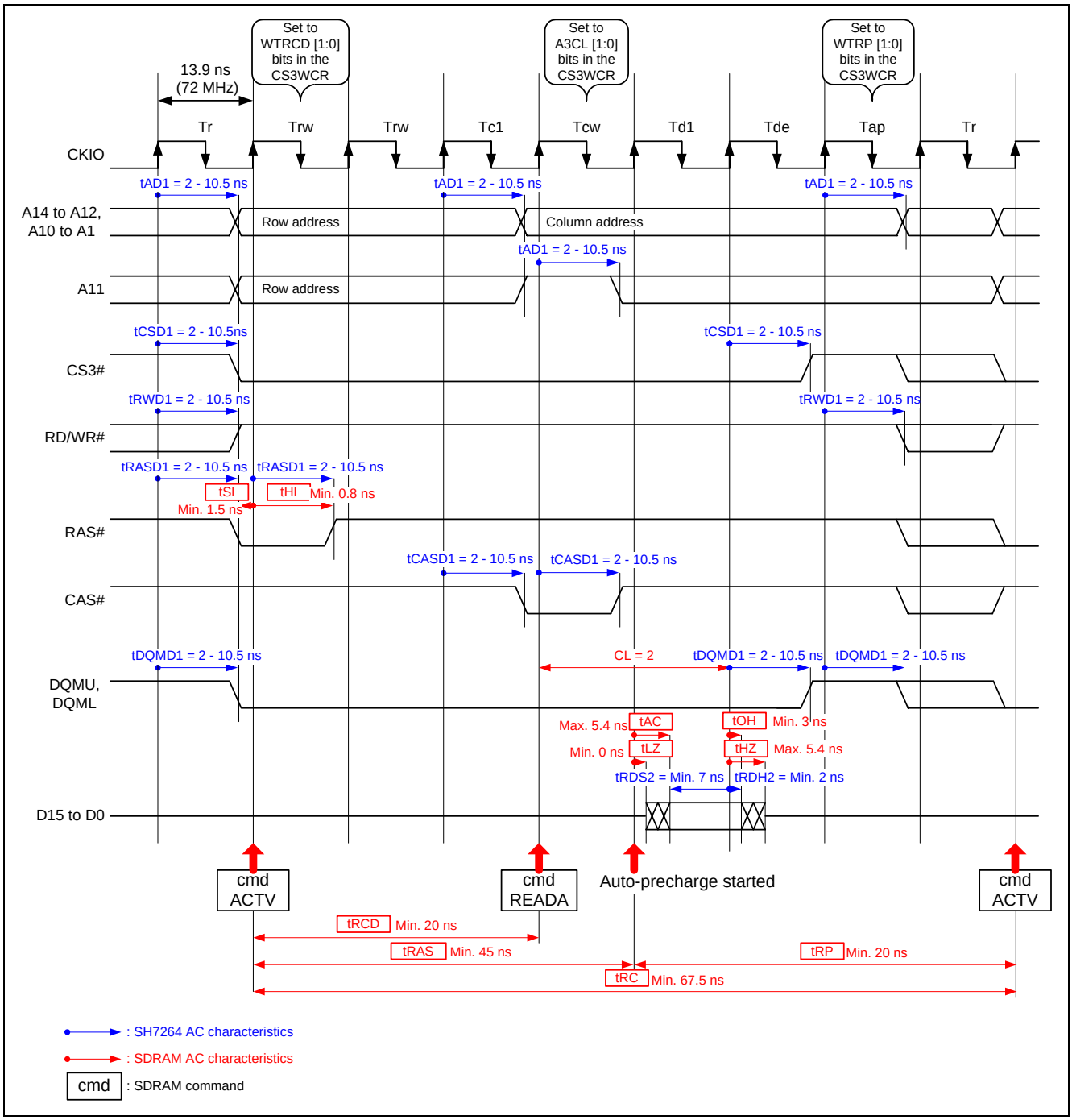


Figure 6 SDRAM Single Read Timing Example

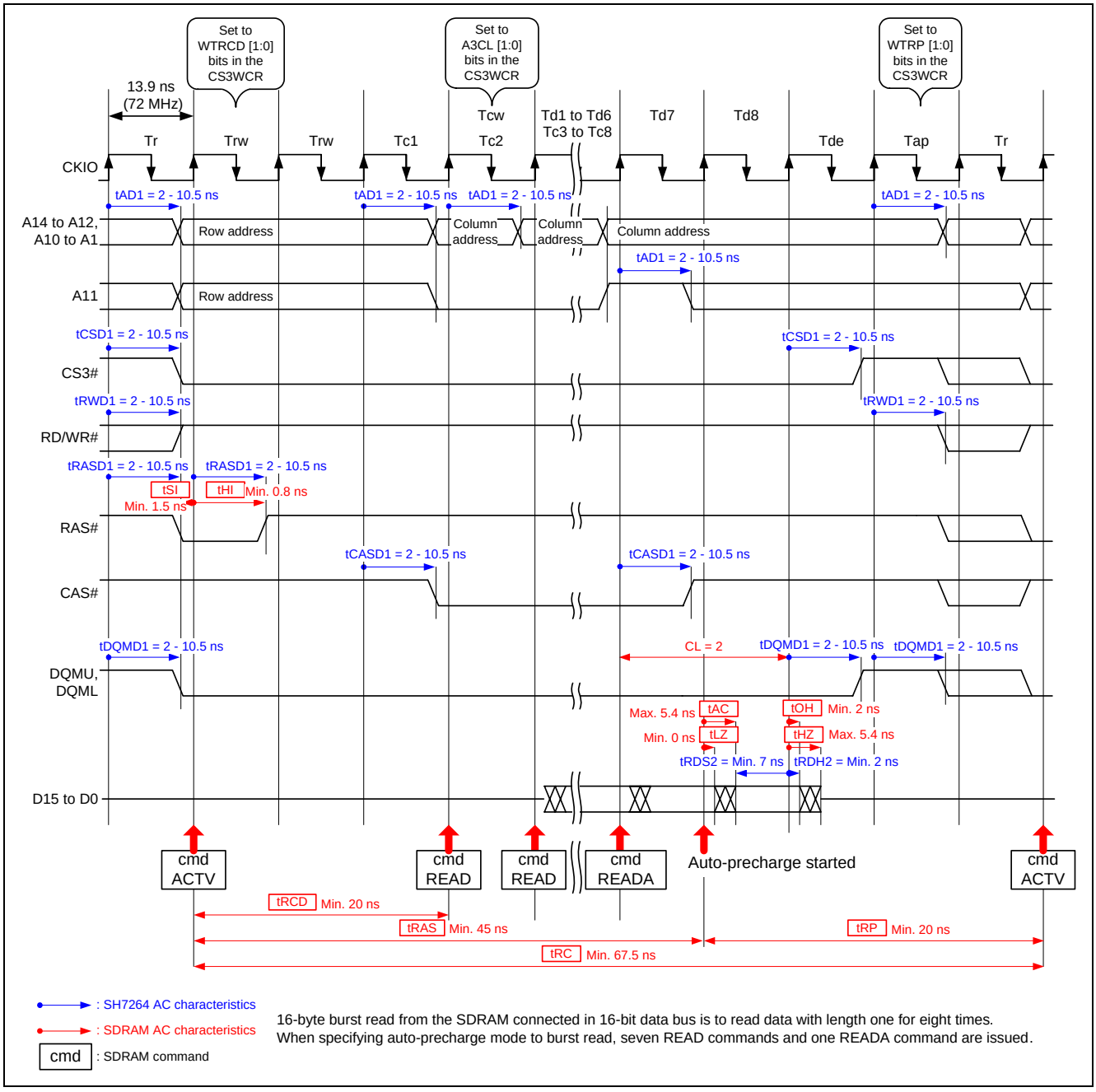


Figure 7 SDRAM Burst Read Timing

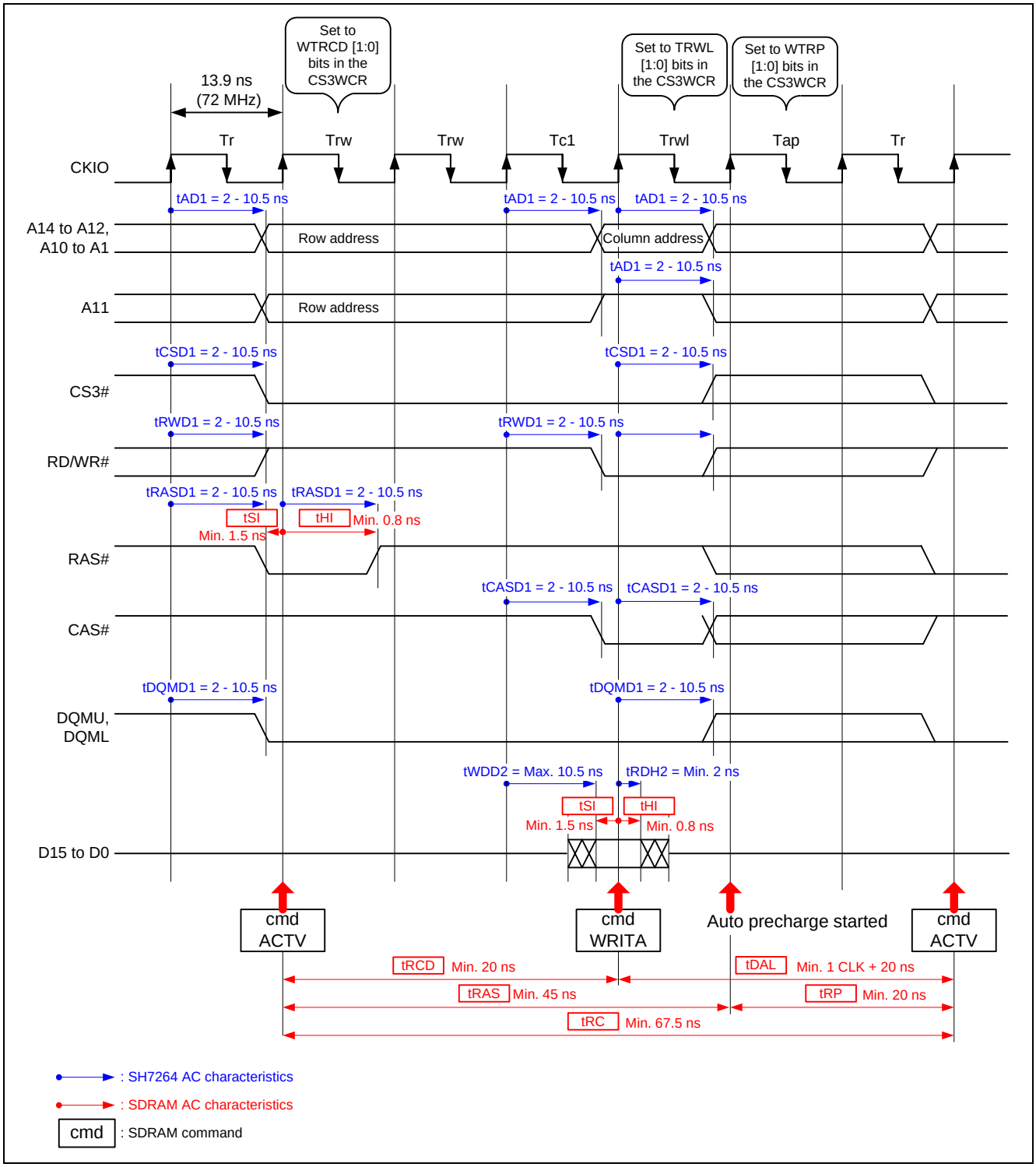


Figure 8 SDRAM Single Write Timing Example

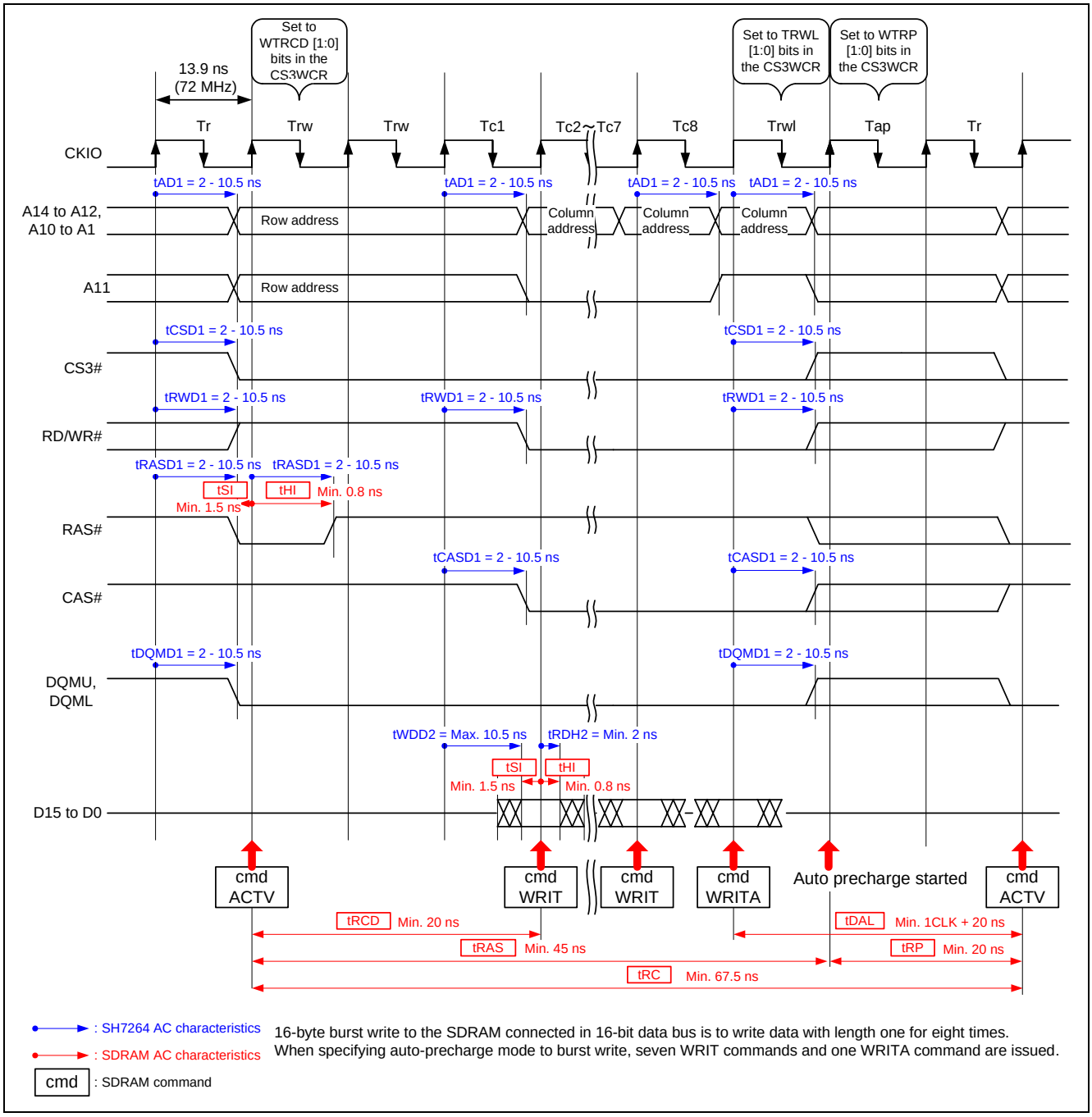


Figure 9 SDRAM Burst Write Timing Example

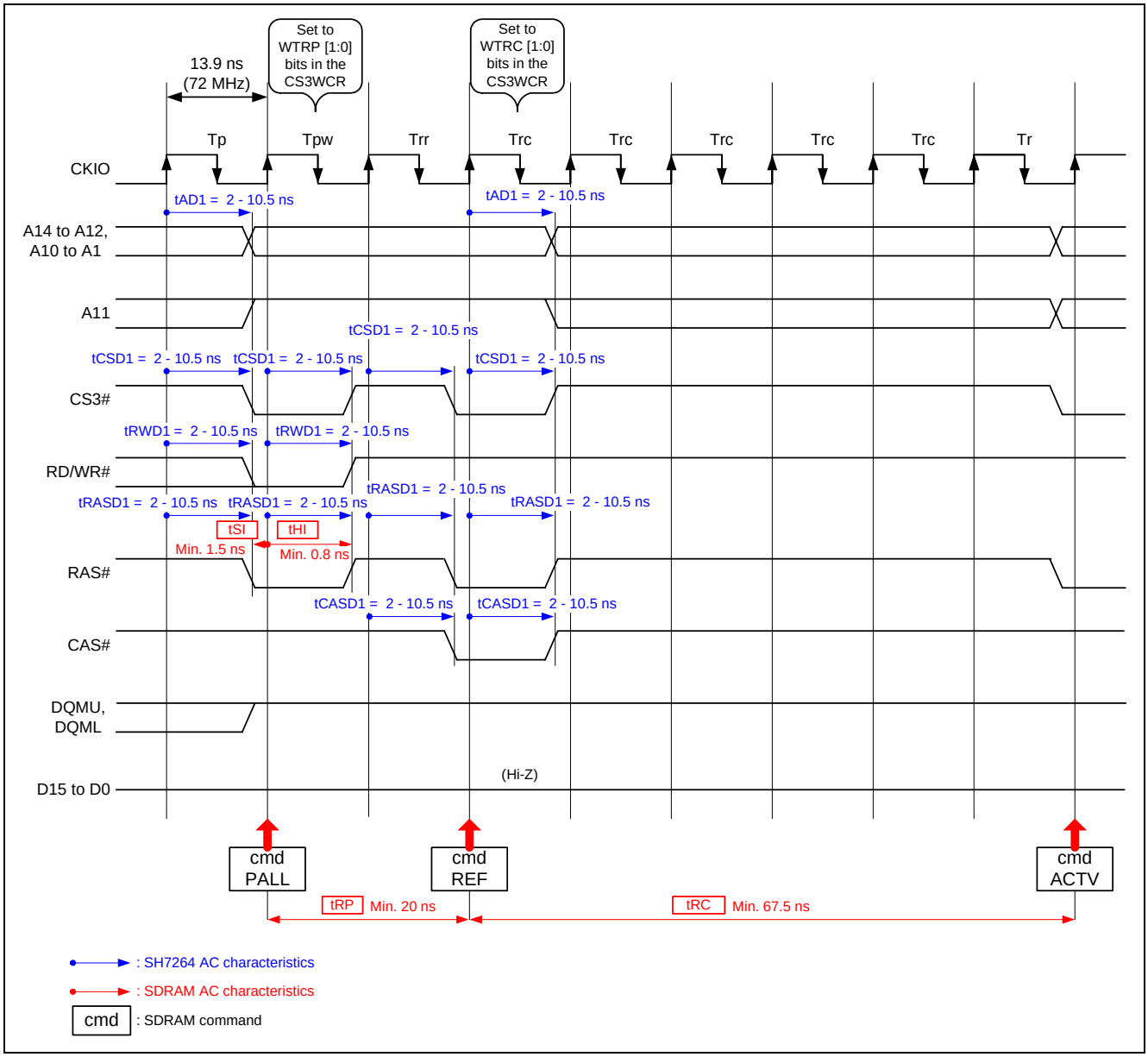


Figure 10 SDRAM Auto-refresh Timing Example

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "hwsetup.c" (1/4)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Electronics Corp. and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Electronics Corp. and is protected under
8       *   all applicable laws, including copyright laws.
9       *
10      *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11      *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12      *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14      *   DISCLAIMED.
15      *
16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17      *   ELECTRONICS CORP. NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18      *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19      *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
20      *   AFFILIATES HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
21      *
22      *   Renesas reserves the right, without notice, to make changes to this
23      *   software and to discontinue the availability of this software.
24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ************************************************************************
28      * (C) 2009(2010) Renesas Electronics Corporation. All rights reserved.
29      *""FILE COMMENT""************ Technical reference data *********************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : hwsetup.c
32      *   Abstract    : Hardware initialization function
33      *   Version     : 1.02.00
34      *   Device      : SH7262/SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                             (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board)
40      *   Description :
41      ************************************************************************
42      *   History     : Jan.13,2009 Ver.1.00.00
43      *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44      *               : Apr.07,2010 Ver.1.02.00 Changed the company name
45      *""FILE COMMENT END""*************************************************/
46      #include "iodefine.h"
47
```

3.3 Sample Program Listing "hwsetup.c" (2/4)

```
48    /* ==== Prototype declaration ==== */
49    void  HardwareSetup(void);
50
51    /* ==== referenced external Prototype declaration ==== */
52    extern void io_set_cpg(void);
53    extern void io_init_bsc_cs0(void);
54    extern void io_init_sdram(void);
55    extern void io_init_cache(void);
56    static void init_puram_section(void);
57    void set_acswr(void);
58
59    #pragma section ResetPRG
60    /*""FUNC COMMENT""*****************************************************************
61     * ID           :
62     * Outline      : Hardware initialization function
63     *-----------------------------------------------------------------------------
64     * Include      : iodefine.h
65     *-----------------------------------------------------------------------------
66     * Declaration  : void  HardwareSetup(void);
67     *-----------------------------------------------------------------------------
68     * Description  : The initial settings of CPG, PFC, and BSC (Flash memory
69     *              : access control and SDRAM initialization) are processed.
70     *-----------------------------------------------------------------------------
71     * Argument     : void
72     *-----------------------------------------------------------------------------
73     * Return Value : void
74     *-----------------------------------------------------------------------------
75     * Note         : None
76     *""FUNC COMMENT END""*************************************************************/
77    void  HardwareSetup(void)
78    {
79      /*====CPG setting====*/
80      io_set_cpg();
81
82      /*====CS0 initialization====*/
83      io_init_bsc_cs0();
84
85      /*====SDRAM area initialization====*/
86      /* ---- Switches AC characteristics ---- */
87      init_puram_section();
88      set_acswr();
89
90      io_init_sdram();
91
92      /*====Cache setting====*/
93      io_init_cache();
94    }
95
```

3.4 Sample Program Listing "hwsetup.c" (3/4)

```
96    /*""FUNC COMMENT""*****************************************************************
97     * ID           :
98     * Outline      : URAM section transfer from ROM to internal RAM
99     *-------------------------------------------------------------------------------
100    * Include      : iodefine.h
101    *-------------------------------------------------------------------------------
102    * Declaration  : static void init_puram_section(void);
103    *-------------------------------------------------------------------------------
104    * Description  : Transfers the program in the URAM section from
105    *              : ROM to internal RAM.
106    *              : Transfer must be executed before setting the SDRAM.
107    *              : This function transfers the URAM section separately before
108    *              : initializing other sections.
109    *-------------------------------------------------------------------------------
110    * Argument     : void
111    *-------------------------------------------------------------------------------
112    * Return Value : void
113    *-------------------------------------------------------------------------------
114    * Note         : None
115    *""FUNC COMMENT END""*************************************************************/
116   static void init_puram_section(void)
117   {
118     unsigned long *src, *end, *dst;
119
120     src = (unsigned long *)__sectop("PURAM");
121     end = (unsigned long *)__secend("PURAM");
122     dst = (unsigned long *)__sectop("RPURAM");
123
124     while(src < end){
125       *dst++ = *src++;
126     }
127   }
128
```

3.5 Sample Program Listing "hwsetup.c" (4/4)

```
129   #pragma section URAM
130   /*""FUNC COMMENT""*****************************************************************
131    * ID           :
132    * Outline      : AC characteristics switch function
133    *-----------------------------------------------------------------------------
134    * Include      : iodefine.h
135    *-----------------------------------------------------------------------------
136    * Declaration  : void set_acswr(void);
137    *-----------------------------------------------------------------------------
138    * Description  : Extends the AC characteristics delay time.
139    *-----------------------------------------------------------------------------
140    * Argument     : void
141    *-----------------------------------------------------------------------------
142    * Return Value : void
143    *-----------------------------------------------------------------------------
144    * Note         : None
145    *""FUNC COMMENT END""*************************************************************/
146   void set_acswr(void)
147   {
148     volatile unsigned long reg;
149
150     /* ==== Sequence to write to the ACSWR register ==== */
151     do{
152       BSC.ACKEYR = 0;
153       BSC.ACKEYR = 0;
154       BSC.ACSWR.LONG = 0x2;      /* Extends the delay time   */
155     }while(BSC.ACSWR.LONG != 0x2 ); /* Checks ACSWR register correctly written */
156
157   }
158
159   /* End of File */
```

3.6 Sample Program Listing "bscsdram.c" (1/4)

```
1     /***********************************************************************
2     *   DISCLAIMER
3     *
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29    *""FILE COMMENT""*********** Technical reference data *********************
30    *   System Name : SH7264 Sample Program
31    *   File Name   : bscsdram.c
32    *   Abstract    : SH7264 Initial Settings
33    *   Version     : 1.02.00
34    *   Device      : SH7262/SH7264
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                             (Ver.9.03 Release00).
38    *   OS          : None
39    *   H/W Platform: M3A-HS64G50(CPU board)
40    *   Description :
41    ************************************************************************
42    *   History     : Feb.02,2008 Ver.1.00.00
43    *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44    *               : Apr.07,2010 Ver.1.02.00 Changed the company name
45    *""FILE COMMENT END""*****************************************************/
46    #include "iodefine.h"
47
```

3.7 Sample Program Listing "bscsdram.c" (2/4)

```
48    /* ==== Macro name definition ==== */
49    /* The address when writing in a SDRAM mode register */
50    #define SDRAM_MODE     (*(volatile unsigned short *)(0xfffc5040))
51
52    /* ==== Prototype Declaration ==== */
53    void io_init_sdram(void);
54
55    #pragma section ResetPRG
56    /*""FUNC COMMENT""*****************************************************************
57     * ID           :
58     * Outline      : SDRAM 16 bit bus width connection settings
59     *-----------------------------------------------------------------------------
60     * Include      : iodefine.h
61     *-----------------------------------------------------------------------------
62     * Declaration  : void io_init_sdram(void);
63     *-----------------------------------------------------------------------------
64     * Description  : A connection setup to SDRAM of CS3 space.
65     *              : The PFC setting is set by bit manipulation not to change the PFC
66     *              : set value which is set by other process.
67     *-----------------------------------------------------------------------------
68     * Argument     : void
69     *-----------------------------------------------------------------------------
70     * Return Value : void
71     *-----------------------------------------------------------------------------
72     * Note         : None
73     *""FUNC COMMENT END""*************************************************************/
74    void io_init_sdram(void)
75    {
76      volatile int j = 133;                 /* 200usec wait count  */
77
78      /* ==== PFC settings ==== */
79      PORT.PCCR2.BIT.PC8MD = 1u;            /* CS3#     */
80      PORT.PCCR1.BIT.PC7MD = 1u;            /* CKE      */
81      PORT.PCCR1.BIT.PC6MD = 1u;            /* CAS#     */
82      PORT.PCCR1.BIT.PC5MD = 1u;            /* RAS#     */
83      PORT.PCCR1.BIT.PC4MD = 1u;            /* DQMU#    */
84      PORT.PCCR0.BIT.PC3MD = 1u;            /* DQML#    */
85      PORT.PCCR0.BIT.PC2MD = 1u;            /* RD/WR#   */
86
```

3.8 Sample Program Listing "bscsdram.c" (3/4)

```
87      /* ==== 200us interval elapsed ? ==== */
88      while(j-- > 0){
89        /* wait */
90      }
91
92      /* ==== CS3BCR settings ==== */
93      BSC.CS3BCR.LONG = 0x00004400ul;
94                                      /*
95                                          Idle Cycles between Write-read Cycles
96                                          and Write-write Cycles : 0 idle cycles
97                                          Memory type :SDRAM
98                                          Data Bus Size : 16-bit
99                                      */
100
101     /* ==== CS3WCR settings ==== */
102     BSC.CS3WCR.SDRAM.LONG = 0x0000288aul;
103                                     /*
104                                         Precharge completion wait cycles: 1 cycle
105                                         Wait cycles between ACTV command
106                                         and READ(A)/WRITE(A) command : 2 cycles
107                                         CAS latency for Area 3 : 2 cycles
108                                         Auto-precharge startup wait cycles : 1 cycle
109                                         Idle cycles from REF command/self-refresh
110                                         Release to ACTV/REF/MRS command
111                                         : 5 cycles
112                                     */
113
114
115     /* ==== SDCR settings ==== */
116     BSC.SDCR.LONG = 0x00000809ul;
117                                     /*
118                                         Refresh Control :Refresh
119                                         RMODE :Auto-refresh is performed
120                                         BACTV :Auto-precharge mode
121                                         Row address for Area 3 : 12-bit
122                                         Column Address for Area 3 : 9-bit
123                                     */
124
125     /* ==== RTCOR settings ==== */
126     BSC.RTCOR.LONG = 0xa55a0046ul;      /*
127                                         15.625us/222ns
128                                         = 70(0x46)cycles per refresh
129                                     */
130
131
132
133
```

3.9 Sample Program Listing "bscsdram.c" (4/4)

```
134     /* ==== RTCSR settings ==== */
135     BSC.RTCSR.LONG = 0xa55a0010ul;
136                                     /*
137                                         Initialization sequence start
138                                         Clock select B-phy/16
139                                         Refresh count :Once
140                                     */
141
142     /* ==== Written in SDRAM Mode Register ==== */
143     SDRAM_MODE = 0;                     /*
144                                         The writing data is arbitrary
145                                         SDRAM mode register setting CS3 space
146                                         Burst read (burst length 1)./Burst write
147                                     */
148   }
149
150   /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.05.09	—	First edition issued
2.00	Jun.18.10	All	Timing examples added Format changed
2.01	Mar.31.11	5	Table 3 Row address corrected

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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