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SH7262/SH7264 Group

Example of Initialization

Summary

This application note gives an example of configuration items to activate the SH7262/SH7264 Microcomputers.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

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2. Applications 3
3. Sample Program Listing 7
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1. Introduction

1.1 Specifications

Configure the clock pulse generator (CPG), bus state controller (BSC), pin function controller (PFC), and cache after the reset is canceled.

1.2 Modules Used

- Clock pulse generator (CPG)
- Bus state controller (BSC)
- Pin Function Controller (PFC)
- Cache

1.3 Applicable Conditions

MCU	**SH7262/SH7264**
Operating Frequency	**Internal clock: 144 MHz** **Bus clock: 72 MHz** **Peripheral clock: 36 MHz**
Integrated Development Environment	**Renesas Technology Corp.** **High-performance Embedded Workshop Ver.4.07.00**
C compiler	**Renesas Technology SuperH RISC engine Family** **C/C++ compiler package Ver.9.03 Release 00**
Compiler options	**Default setting in the High-performance Embedded Workshop** **(-cpu=sh2afpu -fpu=single** **-object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto** **-chgincpath -errorpath -global_volatile=0 -opt_range=all** **-infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)**

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group SDRAM Interface Setting
- SH7262/SH7264 Group Connecting the NOR Flash Memory

2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7264 application notes assume to use the sample program described in this application note as the configuration program.

2.1 Sample Program

The configuration program consists of several source files such as the resetprg.c, describing the PowerON_Reset_PC function, and the hwsetup.c, describing the hardware setup function. Main source files are as follows:

- resetprg.c

This is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the PowerON_Reset_PC function. The PowerON_Reset_PC function is initially executed after the reset is canceled. Beginning address of the function is set in the reset vector defined by the vecttbl.c. Figure 1 shows the flow chart of the PowerON_Reset_PC function.

- hwsetup.c

This source file describes the HardwareSetup function called by the PowerON_Reset_PC function. The HardwareSetup function calls the function to set the CPG, BSC, and cache to configure the hardware at minimum requirements.

Figure 2 shows the flow chart of the HardwareSetup function.

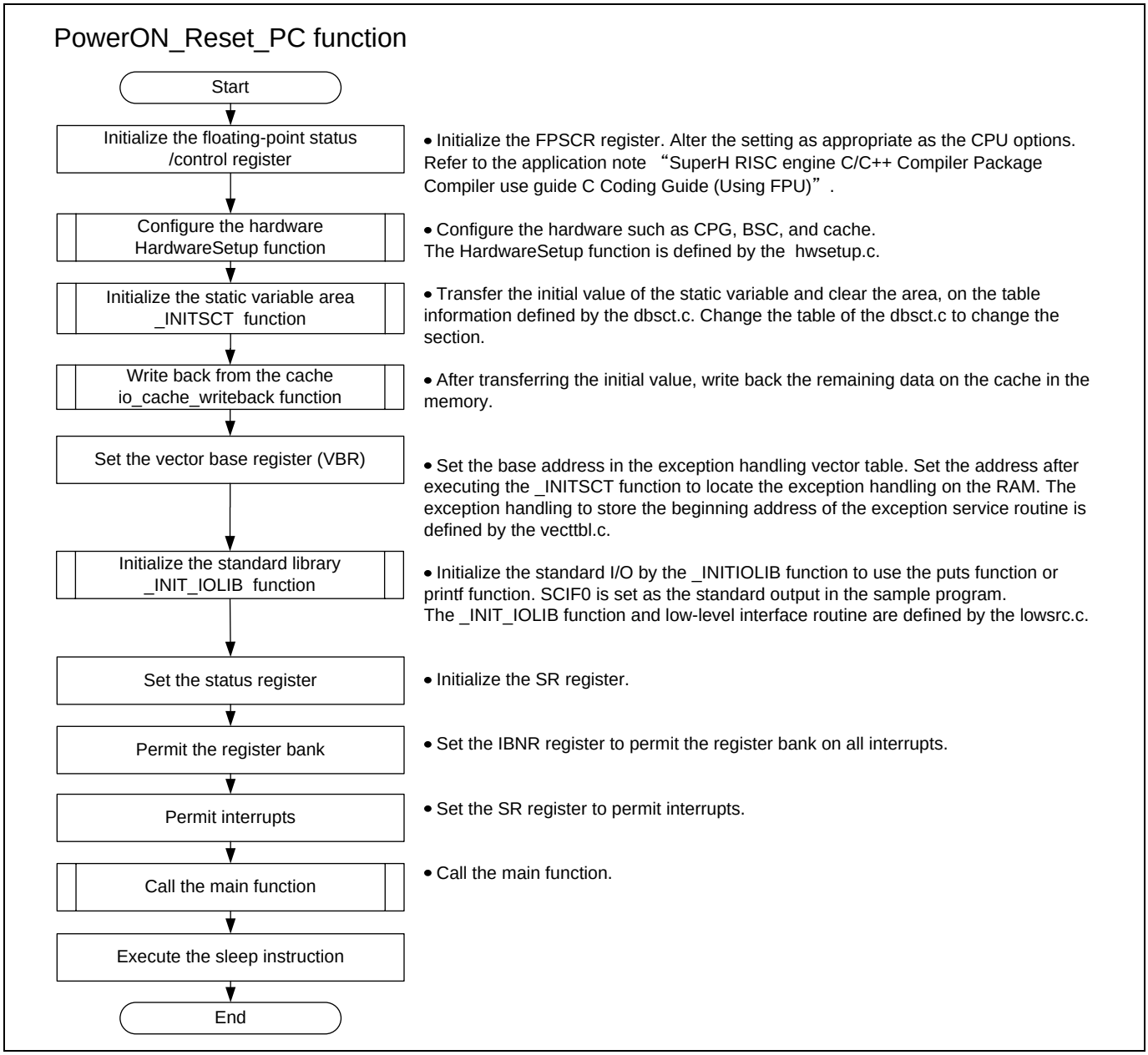

Figure 1 Flow Chart of the PowerON_Reset_PC Function

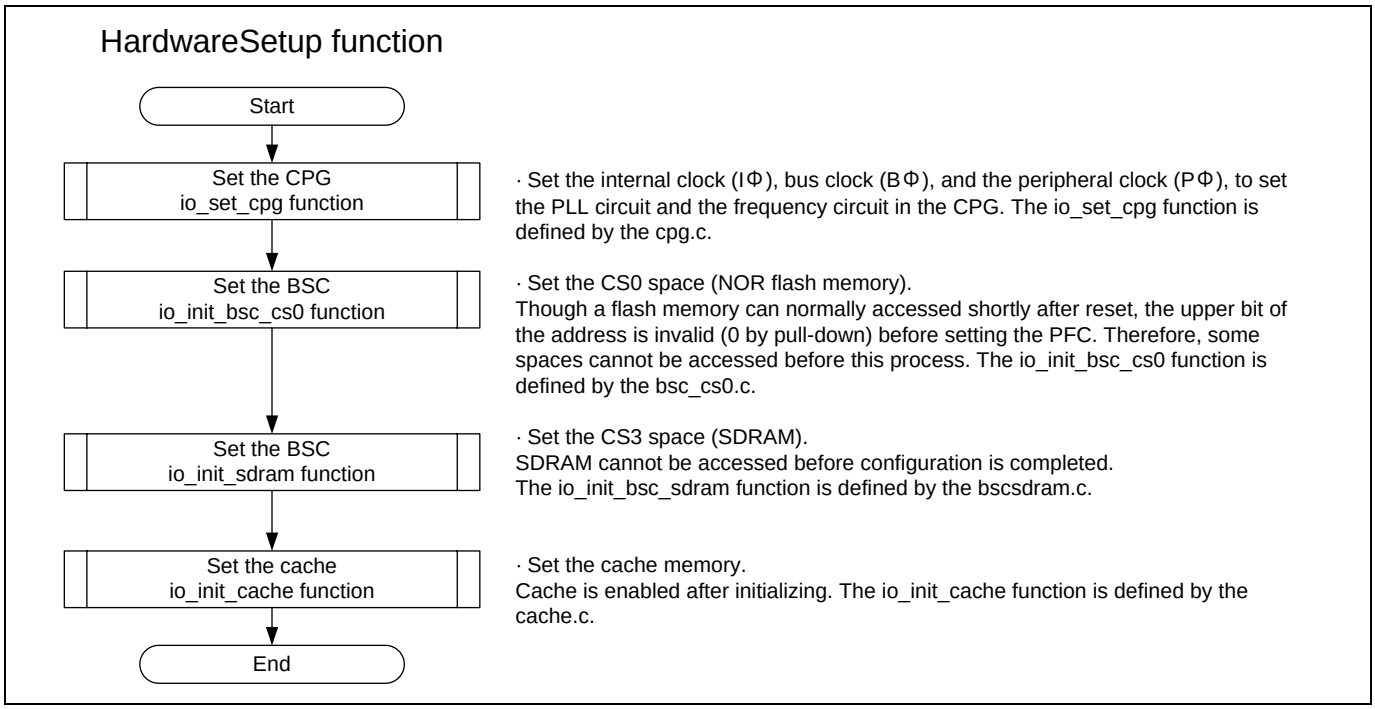

Figure 2 Flow Chart of the HardwareSetup Function

2.2 Setting in the Sample Program

Table 1 shows the setting in the sample program.

Table 1 Sample Program Setting

Module	Setting
FPU	Single-precision Round to zero
CPG	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz (Clockin = 18 MHz)
BSC	CS0: Flash memory Data bus width: 16 bits Number of access wait cycles: 6 CS3: SDRAM Data bus width: 16 bits Row address bits: 12 Column address bits: 9 CAS latency: 2 cycles
PFC	Sets the address bus, data bus, and bus control pin used in the CS0 and CS3 spaces.
Cache	Instruction cache enabled Operand cache enabled
SCIF	Set as the standard output • Channel 0 • Asynchronous, 8-bit data, no parity, 1 stop bit • 57600 bps

2.3 Notes on Using the Sample Program

- The SDRAM must be initialized before being accessed.
  The sample program uses the SDRAM space after configuring the BSC. When using the SDRAM that is not configured, the sample program does not work correctly.
- Do not locate the S section (the stack space) on the SDRAM.
  The initial value of the stack pointer (R15) is set as the value in the reset vector (End address of the S section + 1).
  The sample program locates the S section on the internal memory. When locating the S section on the SDRAM, the sample program accidentally accesses the SDRAM that is not configured upon calling the function in the configuration program.
- Access the static variable area after executing the _INITSCT function.
  The static variable area in C code is initialized by executing the _INITSCT function. When accessing the static variable area before executing the function, the value is undetermined.

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "resetprg.c" (1/3)

```
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29      *""FILE COMMENT""*********** Technical reference data *************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : resetprg.c
32      *   Abstract    : Reset Program
33      *   Version     : 1.01.00
34      *   Device      : SH7262/SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                               (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board)
40      *   Description :
41      ************************************************************************
42      *   History     : Dec.03,2008 Ver.1.00.00
43      *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44      *""FILE COMMENT END""*****************************************************/
```

3.3 Sample Program Listing "resetprg.c" (2/3)

```
45    #include <machine.h>
46    #include <_h_c_lib.h>
47    #include "stacksct.h"
48    #include "iodefine.h"
49
50    #define FPSCR_Init    0x00040001
51
52    #define SR_Init    0x000000F0
53    #define INT_OFFSET 0x10
54
55    extern unsigned int INT_Vectors;
56    void PowerON_Reset_PC(void);
57    void Manual_Reset_PC(void);
58
59    extern void main(void);
60    extern void HardwareSetup(void);
61    extern void io_cache_writeback(void);
62    extern void _INIT_IOLIB(void);
63
64
65
66    //extern void srand(unsigned int);    // Remove the comment when you use rand()
67    //extern char *_s1ptr;                // Remove the comment when you use strtok()
68
69    /*==== Switch section name to ResetPRG ====*/
70    #pragma section ResetPRG
71
72    /*==== Specify the entry function ====*/
73    #pragma entry PowerON_Reset_PC
74
75    /*""FUNC COMMENT""*****************************************************************
76     * ID           :
77     * Outline      : CPU initialization function
78     *-----------------------------------------------------------------------------
79     * Include      : iodefine.h
80     *-----------------------------------------------------------------------------
81     * Declaration  : void PowerON_Reset_PC(void);
82     *-----------------------------------------------------------------------------
83     * Description  : It is the CPU initialization process to register the power on
84     *              : reset exception vector table.
85     *              : This function is firstly executed after power on reset.
86     *              : Enable the processes that are commented depending on its needs.
87     *-----------------------------------------------------------------------------
88     * Argument     : void
89     *-----------------------------------------------------------------------------
90     * Return Value : void
91     *-----------------------------------------------------------------------------
92     * Note         : None
93     *""FUNC COMMENT END""*************************************************************/
```

3.4 Sample Program Listing "resetprg.c" (3/3)

```
94    void PowerON_Reset_PC(void)
95    {
96      set_fpscr(FPSCR_Init);
97
98      /*==== HardwareSetup function====*/
99      HardwareSetup();            // Use Hardware Setup
100
101     /*==== B and D sections initialization ====*/
102     _INITSCT();
103     io_cache_writeback();
104
105     /*==== Vector base register (VBR) setting ====*/
106     set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
107
108     _INIT_IOLIB();              // Use stdio I/O
109
110    //errno=0;                  // Remove the comment when you use errno
111    //srand(1);                 // Remove the comment when you use rand()
112    //_s1ptr=NULL;              // Remove the comment when you use strtok()
113
114     /*==== Status register setting ====*/
115     set_cr(SR_Init);
116     nop();
117
118     /* ==== Bank number register setting ==== */
119     INTC.IBNR.BIT.BE = 0x01;/* Use the register bank in all interrupts */
120
121     /* ==== Interrupt mask level change ==== */
122     set_imask(0);
123
124     /*==== Function call of main function ====*/
125     main();
126
127     /*==== sleep instruction execution ====*/
128     sleep();
129   }
130
131
```

… additional information deleted …

3.5 Sample Program Listing "hwsetup.c" (1/4)

```
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28   *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29   *""FILE COMMENT""*********** Technical reference data *************************
30   *   System Name : SH7264 Sample Program
31   *   File Name   : hwsetup.c
32   *   Abstract    : Hardware initialization function
33   *   Version     : 1.01.00
34   *   Device      : SH7262/SH7264
35   *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36   *               : C/C++ compiler package for the SuperH RISC engine family
37   *               :                             (Ver.9.03 Release00).
38   *   OS          : None
39   *   H/W Platform: M3A-HS64G50(CPU board)
40   *   Description :
41   ***********************************************************************
42   *   History     : Jan.13,2009 Ver.1.00.00
43   *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44   *""FILE COMMENT END""*****************************************************/
45   #include "iodefine.h"
```

3.6 Sample Program Listing "hwsetup.c" (2/4)

```
46    /* ==== Prototype declaration ==== */
47    void  HardwareSetup(void);
48
49    /* ==== referenced external Prototype declaration ==== */
50    extern void io_set_cpg(void);
51    extern void io_init_bsc_cs0(void);
52    extern void io_init_sdram(void);
53    extern void io_init_cache(void);
54    static void init_puram_section(void);
55    void set_acswr(void);
56
57    #pragma section ResetPRG
58    /*""FUNC COMMENT""*****************************************************************
59     * ID           :
60     * Outline      : Hardware initialization function
61     *-----------------------------------------------------------------------------
62     * Include      : iodefine.h
63     *-----------------------------------------------------------------------------
64     * Declaration  : void  HardwareSetup(void);
65     *-----------------------------------------------------------------------------
66     * Description  : The initial settings of CPG, PFC, and BSC (Flash memory
67     *              : access control and SDRAM initialization) are processed.
68     *-----------------------------------------------------------------------------
69     * Argument     : void
70     *-----------------------------------------------------------------------------
71     * Return Value : void
72     *-----------------------------------------------------------------------------
73     * Note         : None
74     *""FUNC COMMENT END""*************************************************************/
75    void  HardwareSetup(void)
76    {
77      /*====CPG setting====*/
78      io_set_cpg();
79
80      /*====CS0 initialization====*/
81      io_init_bsc_cs0();
82
83      /*====SDRAM area initialization====*/
84      /* ---- Switches AC characteristics ---- */
85      init_puram_section();
86      set_acswr();
87
88      io_init_sdram();
89
90      /*====Cache setting====*/
91      io_init_cache();
92    }
93
```

3.7 Sample Program Listing "hwsetup.c" (3/4)

```
94    /*""FUNC COMMENT""*****************************************************************
95     * ID           :
96     * Outline      : URAM section transfer from ROM to internal RAM
97     *-------------------------------------------------------------------------------
98     * Include      : iodefine.h
99     *-------------------------------------------------------------------------------
100    * Declaration  : static void init_puram_section(void);
101    *-------------------------------------------------------------------------------
102    * Description  : Transfers the program in the URAM section from
103    *              : ROM to internal RAM.
104    *              : Transfer must be executed before setting the SDRAM.
105    *              : This function transfers the URAM section separately before
106    *              : initializing other sections.
107    *-------------------------------------------------------------------------------
108    * Argument     : void
109    *-------------------------------------------------------------------------------
110    * Return Value : void
111    *-------------------------------------------------------------------------------
112    * Note         : None
113    *""FUNC COMMENT END""*************************************************************/
114   static void init_puram_section(void)
115   {
116     unsigned long *src, *end, *dst;
117
118     src = (unsigned long *)__sectop("PURAM");
119     end = (unsigned long *)__secend("PURAM");
120     dst = (unsigned long *)__sectop("RPURAM");
121
122     while(src < end){
123       *dst++ = *src++;
124     }
125   }
```

3.8 Sample Program Listing "hwsetup.c" (4/4)

```
126   /*""FUNC COMMENT""*****************************************************************
127    * ID           :
128    * Outline      : URAM section transfer from ROM to internal RAM
129    *-------------------------------------------------------------------------------
130    * Include      : iodefine.h
131    *-------------------------------------------------------------------------------
132    * Declaration  : static void init_puram_section(void);
133    *-------------------------------------------------------------------------------
134    * Description  : Transfers the program in the URAM section from
135    *              : ROM to internal RAM.
136    *              : Transfer must be executed before setting the SDRAM.
137    *              : This function transfers the URAM section separately before
138    *              : initializing other sections.
139    *-------------------------------------------------------------------------------
140    * Argument     : void
141    *-------------------------------------------------------------------------------
142    * Return Value : void
143    *-------------------------------------------------------------------------------
144    * Note         : None
145    *""FUNC COMMENT END""*************************************************************/
146   static void init_puram_section(void)
147   {
148     unsigned long *src, *end, *dst;
149
150     src = (unsigned long *)__sectop("PURAM");
151     end = (unsigned long *)__secend("PURAM");
152     dst = (unsigned long *)__sectop("RPURAM");
153
154     while(src < end){
155       *dst++ = *src++;
156     }
157   }
```

3.9 Sample Program Listing "cpg.c" for 1 MB (1/2)

```
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29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7264 Sample Program
31  *   File Name   : cpg.c
32  *   Abstract    : CPG setting process
33  *   Version     : 1.01.00
34  *   Device      : SH7262/SH7264
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36  *               : C/C++ compiler package for the SuperH RISC engine family
37  *               :                               (Ver.9.03 Release00).
38  *   OS          : None
39  *   H/W Platform: M3A-HS64G50(CPU board)
40  *   Description :
41  ************************************************************************
42  *   History     : Oct.28,2008 Ver.1.00.00
43  *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44  *""FILE COMMENT END""*****************************************************/
45  #include "iodefine.h"
46
47
48  /* ==== Prototype Declaration ==== */
49  void io_set_cpg(void);
```

3.10 Sample Program Listing "cpg.c" for 1 MB (2/2)

```
#pragma section ResetPRG
/*""FUNC COMMENT""*****************************************************************
 * ID           :
 * Outline      : CPG settings
 *-----------------------------------------------------------------------------
 * Include      : iodefine.h
 *-----------------------------------------------------------------------------
 * Declaration  : void io_set_cpg(void);
 *-----------------------------------------------------------------------------
 * Description  : Clock pulse generator (CPG) is set to set to the internal clock
 *              : (I Clock), peripheral clock (P Clock), bus clock (B Clock), and
 *              : I Clock = 144MHz, B Clock = 72MHz,  P Clock = 36MHz.
 *              : This setting example is the case that the function's input clock
 *              : is 18MHz and clock mode is 2.
 *-----------------------------------------------------------------------------
 * Argument     : void
 *-----------------------------------------------------------------------------
 * Return Value : void
 *-----------------------------------------------------------------------------
 * Note         : None
 *""FUNC COMMENT END""*************************************************************/
void io_set_cpg(void)
{
  /* ==== CPG Setting ==== */
  CPG.FRQCR.WORD = 0x1003u;       /* PLL1(x8),I:B:P= 8:4:2
                                   * CKIO:Output at time usually,Output when bus right is
                                   * opened,output at standby"L"
                                   * Clockin = 18MHz, CKIO = 72MHz
                                   * I Clock = 144MHz, B Clock = 72MHz,
                                   * P Clock = 36MHz
                                   */


    /* ---- The clock of all modules is permitted. ---- */
  CPG.STBCR3.BYTE = 0x02u;    /* Port level is keep in standby mode                  */
                              /* IEBus, MTU2,SDHI0, SDHI1, A/D, [1], RTClock         */
  CPG.STBCR4.BYTE = 0x00u;    /* SCIF0, SCIF1, SCIF2, SCIF3, SCIF4, SCIF5, SCIF6, SCIF7*/
  CPG.STBCR5.BYTE = 0x10u;    /* I2C30, I2C31, I2C32, [1], RCAN0, RCAN1, RSPI0, RSPI1  */
  CPG.STBCR6.BYTE = 0x00u;    /* SSI0, SSI1, SSI2, SSI3, CD-ROMDEC, SRC0, SRC1, USB    */
  CPG.STBCR7.BYTE = 0x2au;    /* SIOF, RSPDIF, [1], VDC3, [1], CMT, [1], NAND          */
  CPG.STBCR8.BYTE = 0x7eu;    /* PWM, [1], [1], [1], [1], [1], [1], DECOMP             */

}

/* End of File */
```

3.11 Sample Program Listing "cpg.c" for 640 KB (1/2)

```
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***********************************************************************
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*""FILE COMMENT""*********** Technical reference data *************************
*   System Name : SH7264 Sample Program
*   File Name   : cpg.c
*   Abstract    : CPG setting process
*   Version     : 1.00.00
*   Device      : SH7262(640KB)/SH7264(640KB)
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
*               : C/C++ compiler package for the SuperH RISC engine family
*               :                               (Ver.9.03 Release00).
*   OS          : None
*   H/W Platform: M3A-HS64G60(CPU board)
*   Description :
***********************************************************************
*   History     : Jun.30,2009 Ver.1.00.00
*""FILE COMMENT END""*****************************************************/
#include "iodefine.h"


/* ==== Prototype Declaration ==== */
void io_set_cpg(void);

```

3.12 Sample Program Listing "cpg.c" for 640 KB (2/2)

```
#pragma section ResetPRG
/*""FUNC COMMENT""*****************************************************************
 * ID           :
 * Outline      : CPG settings
 *-----------------------------------------------------------------------------
 * Include      : iodefine.h
 *-----------------------------------------------------------------------------
 * Declaration  : void io_set_cpg(void);
 *-----------------------------------------------------------------------------
 * Description  : Clock pulse generator (CPG) is set to set to the internal clock
 *              : (I Clock), peripheral clock (P Clock), bus clock (B Clock), and
 *              : I Clock = 144MHz, B Clock = 72MHz,  P Clock = 36MHz.
 *              : This setting example is the case that the function's input clock
 *              : is 18MHz and clock mode is 2.
 *-----------------------------------------------------------------------------
 * Argument     : void
 *-----------------------------------------------------------------------------
 * Return Value : void
 *-----------------------------------------------------------------------------
 * Note         : None
 *""FUNC COMMENT END""*************************************************************/
void io_set_cpg(void)
{
  /* ==== CPG Setting ==== */
  CPG.FRQCR.WORD = 0x1003u;       /* PLL1(x8),I:B:P= 8:4:2
                                   * CKIO:Output at time usually,Output when bus right is
                                   * opened,output at standby"L"
                                   * Clockin = 18MHz, CKIO = 72MHz
                                   * I Clock = 144MHz, B Clock = 72MHz,
                                   * P Clock = 36MHz
                                   */


    /* ---- The clock of all modules is permitted. ---- */
  CPG.STBCR3.BYTE = 0x02u;    /* Port level is keep in standby mode                  */
                              /* IEBus, MTU2,SDHI0, SDHI1, A/D, [1], RTClock         */
  CPG.STBCR4.BYTE = 0x00u;    /* SCIF0, SCIF1, SCIF2, SCIF3, SCIF4, SCIF5, SCIF6, SCIF7*/
  CPG.STBCR5.BYTE = 0x10u;    /* I2C30, I2C31, I2C32, [1], RCAN0, RCAN1, RSPI0, RSPI1  */
  CPG.STBCR6.BYTE = 0x00u;    /* SSI0, SSI1, SSI2, SSI3, CD-ROMDEC, SRC0, SRC1, USB    */
  CPG.STBCR7.BYTE = 0x2au;    /* SIOF, RSPDIF, [1], VDC3, [1], CMT, [1], NAND          */
  CPG.STBCR8.BYTE = 0x7eu;    /* PWM, [1], [1], [1], [1], [1], [1], DECOMP             */

  /* ----  Writing to large-capacity RAM is enabled. ---- */
  CPG.SYSCR5.BYTE = 0x0fu;

}

/* End of File */
```

3.13 Sample Program Listing "bsc_cs0.c" (1/3)

```
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29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7264 Sample Program
31  *   File Name   : bsc_cs0.c
32  *   Abstract    : SH7264 Initial Settings
33  *   Version     : 1.01.00
34  *   Device      : SH7262/SH7264
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36  *               : C/C++ compiler package for the SuperH RISC engine family
37  *               :                               (Ver.9.03 Release00).
38  *   OS          : None
39  *   H/W Platform: M3A-HS64G50(CPU board)
40  *   Description :
41  ************************************************************************
42  *   History     : Dec.11,2008 Ver.1.00.00
43  *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44  *""FILE COMMENT END""*****************************************************/
45  #include "iodefine.h"
46  /*  CS0 PAGEMODE setting */
47  //#define PAGEMODE
48  /* ==== Prototype Declaration ==== */
49  void io_init_bsc_cs0(void);
```

3.14 Sample Program Listing "bsc_cs0.c" (2/3)

```
50      #pragma section ResetPRG
51      /*""FUNC COMMENT""*****************************************************************
52       * ID           :
53       * Outline      : CS0 setting
54       *-------------------------------------------------------------------------------
55       * Include      : iodefine.h
56       *-------------------------------------------------------------------------------
57       * Declaration  : void io_init_bsc_cs0(void);
58       *-------------------------------------------------------------------------------
59       * Description  : Pin function controller (PFC) and bus state controller (BSC)
60       *              : are set, and the access timing to the Flash Memory of CS0 space
61       *              : is set.
62       *              : The PFC setting is set by bit manipulation not to change the PFC
63       *              : set value which is set by other process.
64       *-------------------------------------------------------------------------------
65       * Argument     : void
66       *-------------------------------------------------------------------------------
67       * Return Value : void
68       *-------------------------------------------------------------------------------
69       * Note         : None
70       *""FUNC COMMENT END""*************************************************************/
71      void io_init_bsc_cs0(void)
72      {
73        /* ==== PFC settings ==== */
74        PORT.PBCR5.BIT.PB21MD  = 1u;/* Set A21 */
75        PORT.PBCR5.BIT.PB20MD  = 1u;/* Set A20 */
76        PORT.PCCR0.BIT.PC3MD   = 1u;/* Set WE0# */
77
78
79      #ifdef PAGEMODE
80
81        /* ==== CS0WCR settings ====  */
82        BSC.CS0WCR.BROM_ASY.LONG = 0x002303c0ul;
83                                   /* Number of Burst: 4-4 or 2-4-2         */
84                                   /* Number of Burst Wait Cycles: 3 cycles  */
85                                   /* Number of Access Wait Cycles: 8 cycles */
86
87
88
89        /* ==== CS0BCR settings ==== */
90        BSC.CS0BCR.LONG = 0x30001400ul;
91                                   /* Idle Cycles between Write-read Cycles  */
92                                   /*  and Write-write Cycles: 4 idle cycles */
93                                   /* Type: Burst ROM (ASY)                  */
94                                   /* Data Bus Size: 16-bit                  */
95
96      #else /* PAGEMODE */
97
```

3.15 Sample Program Listing "bsc_cs0.c" (3/3)

```
98
99        /* ==== CS0WCR settings ====  */
100       BSC.CS0WCR.NORMAL.LONG = 0x00000b41ul;
101                                 /* Number of Delay Cycles from Address,   */
102                                 /*  CS0# Assertion to RD#,WEn Assertion   */
103                                 /*  : 1.5 cycles                          */
104                                 /* Number of Access Wait Cycles: 6 cycles    */
105                                 /* Delay Cycles from RD,WEn# negation to  */
106                                 /*  Address,CSn# negation: 1.5 cycles        */
107
108
109       /* ==== CS0BCR settings ==== */
110       BSC.CS0BCR.LONG = 0x12400400ul;
111                                 /* Idle Cycles between Write-read Cycles  */
112                                 /*  and Write-write Cycles : 1 idle cycle    */
113                                 /*  and read-write Cycles : 1 idle cycle  */
114                                 /* Data Bus Size: 16-bit                  */
115
116     #endif /* PAGEMODE */
117     }
118
119     /* End of File */
120
```

3.16 Sample Program Listing "bscsdram.c" (1/3)

```
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27  ************************************************************************
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29  *""FILE COMMENT""*********** Technical reference data *********************
30  *   System Name : SH7264 Sample Program
31  *   File Name   : bscsdram.c
32  *   Abstract    : SH7264 Initial Settings
33  *   Version     : 1.01.00
34  *   Device      : SH7262/SH7264
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36  *               : C/C++ compiler package for the SuperH RISC engine family
37  *               :                             (Ver.9.03 Release00).
38  *   OS          : None
39  *   H/W Platform: M3A-HS64G50(CPU board)
40  *   Description :
41  ************************************************************************
42  *   History     : Feb.02,2008 Ver.1.00.00
43  *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44  *""FILE COMMENT END""*****************************************************/
45  #include "iodefine.h"
46  /* ==== Macro name definition ==== */
47  /* The address when writing in a SDRAM mode register */
48  #define SDRAM_MODE     (*(volatile unsigned short *)(0xfffc5040))
49  /* ==== Prototype Declaration ==== */
50  void io_init_sdram(void);
```

3.17 Sample Program Listing "bscsdram.c" (2/3)

```
#pragma section ResetPRG
/*""FUNC COMMENT""*****************************************************************
 * ID           :
 * Outline      : SDRAM 16 bit bus width connection settings
 *-----------------------------------------------------------------------------
 * Include      : iodefine.h
 *-----------------------------------------------------------------------------
 * Declaration  : void io_init_sdram(void);
 *-----------------------------------------------------------------------------
 * Description  : A connection setup to SDRAM of CS3 space.
 *              : The PFC setting is set by bit manipulation not to change the PFC
 *              : set value which is set by other process.
 *-----------------------------------------------------------------------------
 * Argument     : void
 *-----------------------------------------------------------------------------
 * Return Value : void
 *-----------------------------------------------------------------------------
 * Note         : None
 *""FUNC COMMENT END""*************************************************************/
void io_init_sdram(void)
{
  volatile int j = 133;                 /* 200usec wait count  */

  /* ==== PFC settings ==== */
  PORT.PCCR2.BIT.PC8MD = 1u;            /* CS3#     */
  PORT.PCCR1.BIT.PC7MD = 1u;            /* CKE      */
  PORT.PCCR1.BIT.PC6MD = 1u;            /* CAS#     */
  PORT.PCCR1.BIT.PC5MD = 1u;            /* RAS#     */
  PORT.PCCR1.BIT.PC4MD = 1u;            /* DQMU#    */
  PORT.PCCR0.BIT.PC3MD = 1u;            /* DQML#    */
  PORT.PCCR0.BIT.PC2MD = 1u;            /* RD/WR#   */

  /* ==== 200us interval elapsed ? ==== */
  while(j-- > 0){
    /* wait */
  }

  /* ==== CS3BCR settings ==== */
  BSC.CS3BCR.LONG = 0x00004400ul;
                                    /*
                                        Idle Cycles between Write-read Cycles
                                        and Write-write Cycles : 0 idle cycles
                                        Memory type :SDRAM
                                        Data Bus Size : 16-bit
                                    */

```

3.18 Sample Program Listing "bscsdram.c" (3/3)

```
97      /* ==== CS3WCR settings ==== */
98      BSC.CS3WCR.SDRAM.LONG = 0x0000288aul;
99                                      /*
100                                         Precharge completion wait cycles: 1 cycle
101                                         Wait cycles between ACTV command
102                                         and READ(A)/WRITE(A) command : 2 cycles
103                                         CAS latency for Area 3 : 2 cycles
104                                         Auto-precharge startup wait cycles : 1 cycle
105                                         Idle cycles from REF command/self-refresh
106                                         Release to ACTV/REF/MRS command
107                                         : 5 cycles
108                                     */
109
110
111     /* ==== SDCR settings ==== */
112     BSC.SDCR.LONG = 0x00000809ul;
113                                     /*
114                                         Refresh Control :Refresh
115                                         RMODE :Auto-refresh is performed
116                                         BACTV :Auto-precharge mode
117                                         Row address for Area 3 : 12-bit
118                                         Column Address for Area 3 : 9-bit
119                                     */
120
121     /* ==== RTCOR settings ==== */
122     BSC.RTCOR.LONG = 0xa55a0046ul;      /*
123                                         15.625us/222ns
124                                         = 70(0x46)cycles per refresh
125                                     */
126
127
128
129
130     /* ==== RTCSR settings ==== */
131     BSC.RTCSR.LONG = 0xa55a0010ul;
132                                     /*
133                                         Initialization sequence start
134                                         Clock select B-phy/16
135                                         Refresh count :Once
136                                     */
137
138     /* ==== Written in SDRAM Mode Register ==== */
139     SDRAM_MODE = 0;                     /*
140                                         The writing data is arbitrary
141                                         SDRAM mode register setting CS3 space
142                                         Burst read (burst length 1)./Burst write
143                                     */
144   }
145   /* End of File */
```

3.19 Sample Program Listing "cache.c" (1/3)

```
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29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7264 Sample Program
31  *   File Name   : cache.c
32  *   Abstract    : sample of cache register
33  *   Version     : 1.01.00
34  *   Device      : SH7262/SH7264
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36  *               : C/C++ compiler package for the SuperH RISC engine family
37  *               :                              (Ver.9.03 Release00).
38  *   OS          : None
39  *   H/W Platform: M3A-HS64G50(CPU board)
40  *   Description :
41  ************************************************************************
42  *   History     : Dec.03,2008 Ver.1.00.00
43  *               : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
44  *""FILE COMMENT END""*****************************************************/
45  #include <machine.h>
46  #include "iodefine.h"
47  /* ==== Prototype Declaration ==== */
48  void io_init_cache(void);
49  int io_cache_writeback(void);
```

3.20 Sample Program Listing "cache.c" (2/3)

```
50      #pragma section CACHE     /* It is placed in the CS0 cache-disabled space */
51      /*""FUNC COMMENT""*****************************************************************
52       * ID            :
53       * Outline       : Cache initialization
54       *-----------------------------------------------------------------------------
55       * Include       : iodefine.h
56       *-----------------------------------------------------------------------------
57       * Declaration   : void io_init_cache(void);
58       *-----------------------------------------------------------------------------
59       * Description   : Instruction/operand cache are flushed and enabled.
60       *               : The section name of this function is changed to be placed in
61       *               : the cache-disabled.
62       *               : When this function is used only in the state of interrupt level 15,
63       *               : the setting and clearing of interrupt mask need not be processed.
64       *-----------------------------------------------------------------------------
65       * Argument      : void
66       *-----------------------------------------------------------------------------
67       * Return Value : void
68       *-----------------------------------------------------------------------------
69       * Note          : None
70       *""FUNC COMMENT END""*************************************************************/
71      void io_init_cache(void)
72      {
73        volatile unsigned long reg;
74        int mask;
75
76        /* ==== Interrupt mask setting ==== */
77        mask = get_imask();
78        set_imask(15);              /* Set to the level 15 */
79
80        /* ==== Cache register setting ==== */
81        CCNT.CCR1.LONG = 0x0909ul;  /* Write back ON */
82
83                                    /*
84                                        ICF=1:Instruction cache flushed
85                                        ICE=1:Instruction cache enabled
86                                        OCF=1:Operand cache flushed
87                                        OCE=1:Operand cache enabled
88                                    */
89        /* ==== Reading cache register ==== */
90        reg = CCNT.CCR1.LONG ;
91
92        /* ==== Clearing interrupt mask ==== */
93        set_imask(mask);            /* Set to the original level */
94
95      }
96
```

3.21 Sample Program Listing "cache.c" (3/3)

```
97      /*""FUNC COMMENT""*****************************************************************
98       * ID           :
99       * Outline      : Write-back of cache
100      *-------------------------------------------------------------------------------
101      * Include      : iodefine.h
102      *-------------------------------------------------------------------------------
103      * Declaration  : int io_cache_writeback(void);
104      *-------------------------------------------------------------------------------
105      * Description  : All lines of operand cache are disabled, and the contents of
106      *              : cache memory are written back to the external memory.
107      *              : It has nothing to do with the write-through mode.
108      *-------------------------------------------------------------------------------
109      * Argument     : void
110      *-------------------------------------------------------------------------------
111      * Return Value : 0 : Normal completion
112      *-------------------------------------------------------------------------------
113      * Note         : None
114      *""FUNC COMMENT END""*************************************************************/
115     int io_cache_writeback(void)
116     {
117       volatile unsigned long *arry;
118       unsigned int i,j;
119       int mask;
120
121       /* ==== Interrupt mask setting ==== */
122       mask = get_imask();
123       set_imask(15);                  /* Set to the level 15 */
124
125       /* ====  All entries disabled ==== */
126       for(i=0u; i <4u; i++){
127         for(j=0u; j < 128u; j++){
128             /* ---- Creating an address array address ---- */
129             arry = (volatile unsigned long *)(0xf0800000 | (i<<11) | (j<<4));
130             /* ---- Write U=0 and V=0 in the address array ---- */
131             *arry &= 0xfffffffcul;     /* V=0,U=0 */
132         }
133       }
134
135       /* ==== Interrupt mask recovery ==== */
136       set_imask(mask);                /* Set to the original level */
137
138       return 0;
139     }
140
141
142     /* End of File */
143
```

4. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  (Download the latest version from the Renesas website.)

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  (Download the latest version from the Renesas website.)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.05, 09	—	First edition issued
1.01	Oct.09, 09	—	Sample program for 640-KB RAM added

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