SH7239 Group

Connecting SRAM with the Bus State Controller

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Abstract

This document describes the connection to SRAM using the SH7239 bus state controller interface in normal space.

Products

SH7239

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

The interface function in the normal space is used in this application note. Two SRAMs of 32K bytes (32K words × 8 bits) are connected to the bus state controller in 16-bit bus width.

Table 1.1 lists the peripheral functions and their applications. Figure 1.1 shows the memory map associated with the SRAM.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Bus state controller (BSC)	Sets the access timing to the SRAM in the CS0 space.
Pin function controller (PFC)	Sets the pin functions to the output function as follows, each function respectively: — PA17 to PA15, and PA0 at port A to $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, and $\overline{CS0}$ — PC15 to PC1 at port C to A15 to A1 — PD15 to PD0 at port D to D15 to D0

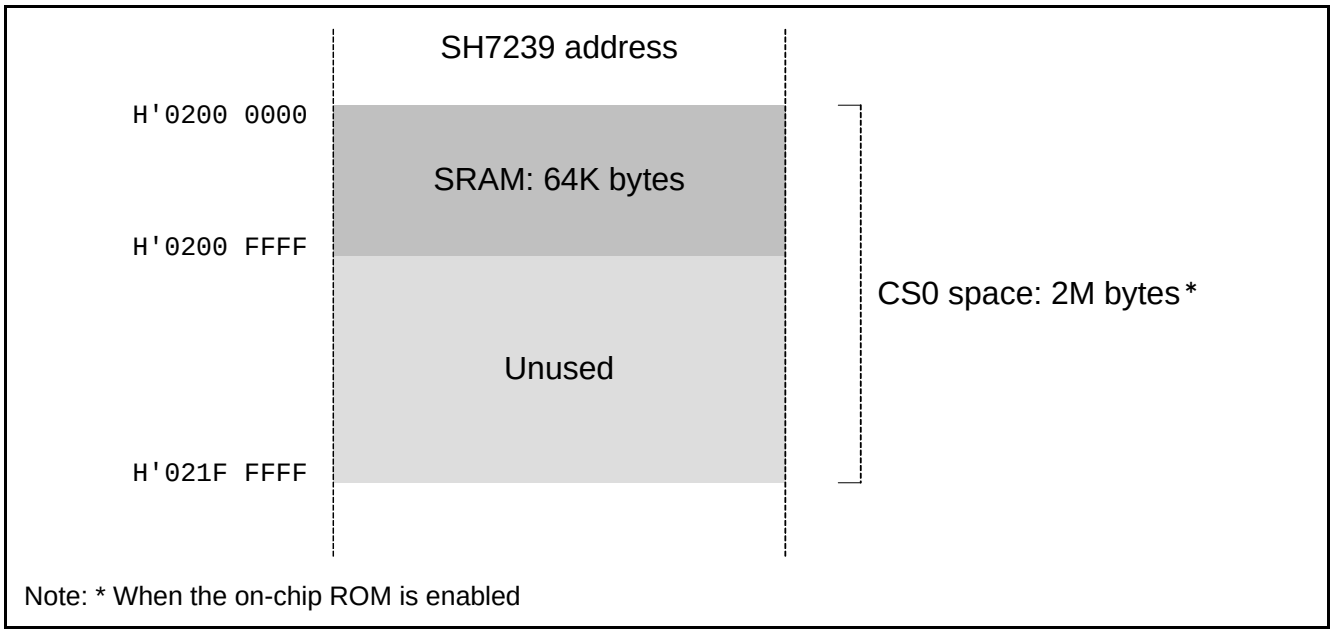

Figure 1.1 Memory Map Associated with the SRAM

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7239 (R5F72395ADFP)
Operating frequency	Main clock: 160MHz Bus clock: 40MHz Peripheral clock: 40MHz
Operating voltage	Vcc: 3.3V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics Corporation SuperH RISC Family C/C++ Compiler Package Ver.9.03 Release 02
	Complier option -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	MCU extension mode 2
Sample code version	1.00
Board used	R0K572390C000BR
Device used	SRAM (R1LV5256ESA-7SR)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- SH7239 Group Example of Initialization (R01AN0297EJ)

4. Peripheral Function

This chapter provides supplementary information on the features of the bus state controller (BSC). Refer to the "SH7239 Group, SH7237 Group User's Manual: Hardware" for basic information.

4.1 Bus State Controller (BSC)

The bus state controller outputs control signals to the memory devices connected to the external space and to the external devices, which allows the memory devices such as the SRAM and external devices to connect directly. The features of the bus state controller are described below.

- A maximum of 2M bytes for each of areas CS0, CS1, and CS3 to CS6.
- Can specify the normal space interface and MPX-I/O for each address space:
  - Supports interfaces connectable to the SRAM directly in the normal space interface.
  - Can directly connect the peripheral LSIs that require address/data multiplex in the MPX-I/O interface.
- Can select the data bus width (8 or 16 bits) for each address space.
- Controls insertion of wait cycles for each address space.
- Controls insertion of wait cycles for each read access and write access.
- Can set independent idle cycles during the continuous access for five cases: read-write (in same space/different spaces), read-read (in same space/different spaces), the first cycle is a write access.
- Supports bus arbitration function: shares all of the resources with other CPU and outputs the bus enable after receiving the bus request from external devices.

In this application note, the normal space interface connectable to the SRAM is used.

5. Hardware

5.1 Hardware Configuration

Figure 5.1 shows the example of configuration for the 16-bit data-width SRAM.

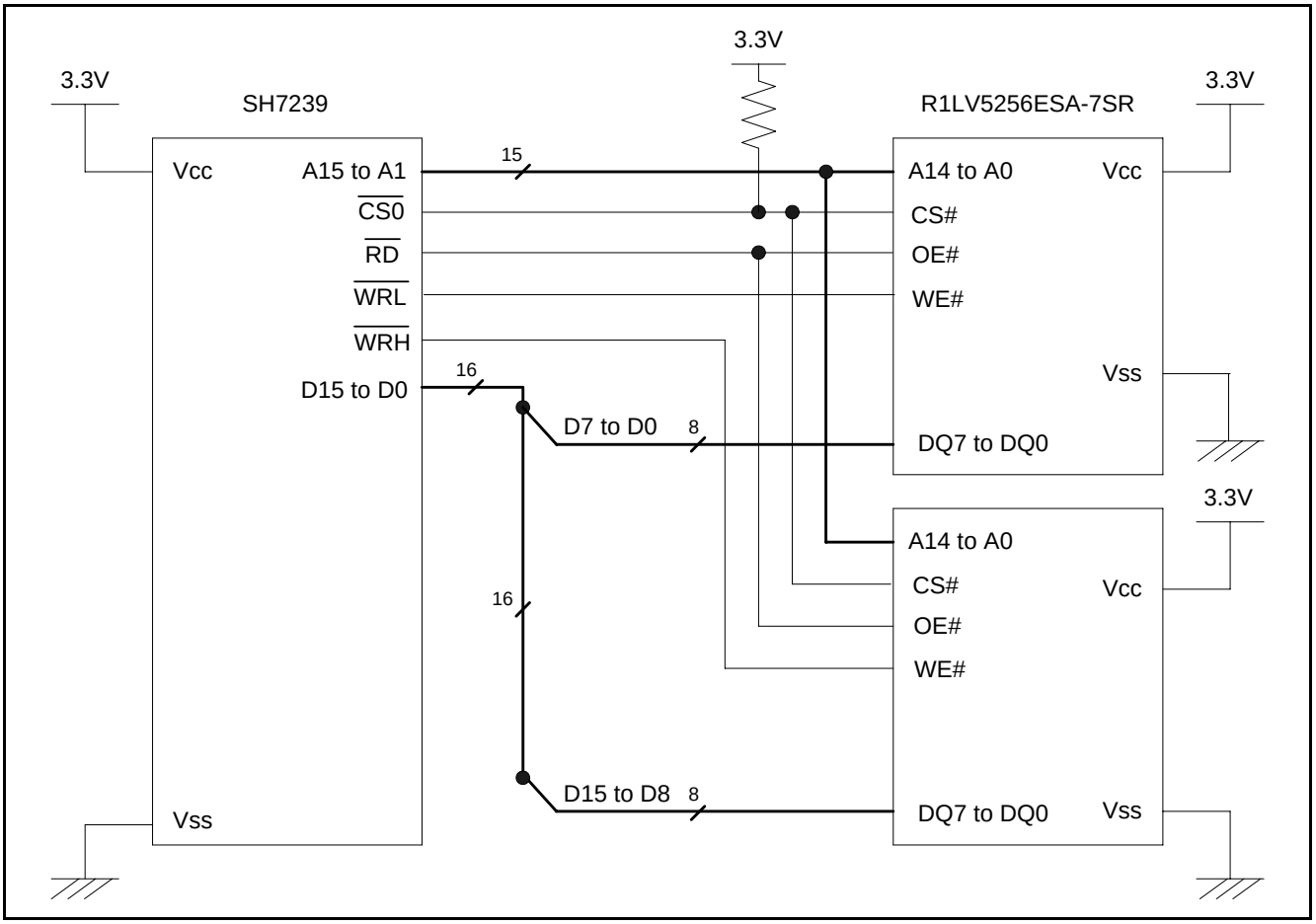

Figure 5.1 16-Bit Data-Width SRAM Connection

5.2 Pins Used

Table 5.1 lists the pins used and their functions. The pin function is switched by the pin function controller.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
A15 to A1	**Output**	Address bus
D15 to D0	**Input/Output**	Data bus
$\overline{\text{CS0}}$	**Output**	Chip select
$\overline{\text{RD}}$	**Output**	Read pulse signal (read data output enable signal)
$\overline{\text{WRH}}$	**Output**	Byte-write instruction for D15 to D8
$\overline{\text{WRL}}$	**Output**	Byte-write instruction for D7 to D0

6. Software

6.1 Operation Overview

This section describes a read-write access timing in the same space to the normal space interface that is connectable to the SRAM directly which is used in this application note.

Figure 6.1 shows a read-write access timing. Figure 6.2 shows a read-read access timing including t_{ACC} and t_{OE} in the specification with the read data set up.

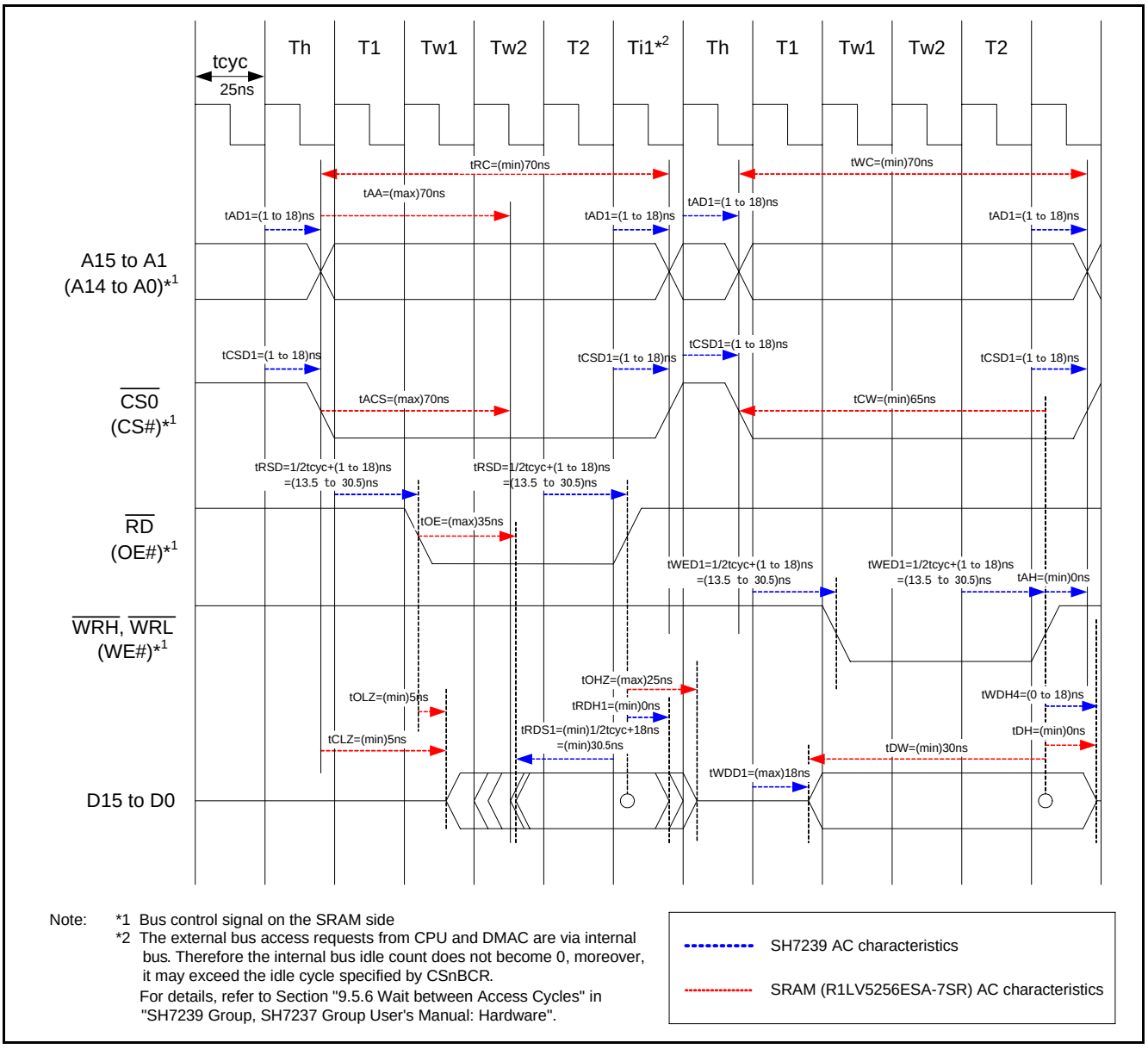

Figure 6.1 Read-Write Access Timing

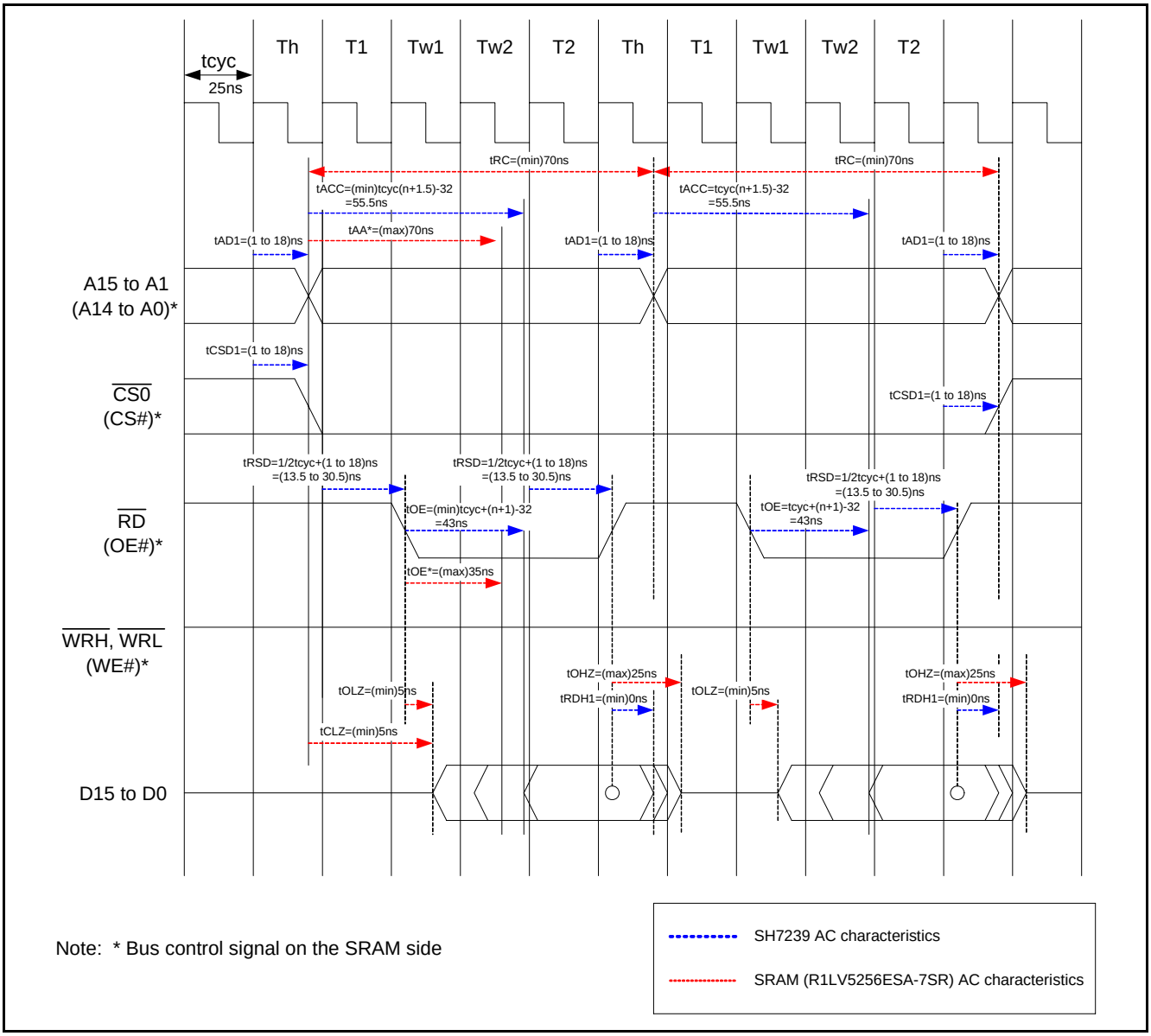

Figure 6.2 Read-Read Access Timing including t_{ACC} and t_{OE}

[Remarks] Specification of set up timing for the data signal when reading

The SH-2/SH-2A series products with the general flash ROM (including this MCU) is added two times for data set up timing to read the general external memory besides the read data set up time (t_{RDS}). Refer to the following descriptions.

- Read data access time (t_{ACC})
- Access time from read strobe (t_{OE})

Design the read timing to fulfill the following relationship at the same fulfilling the above specification of the t_{ACC} and t_{OE} . In this case, the specification of the t_{PDS} does not need to be considered.

- The address access time on the SRAM side t_{AA}*(max) ≤ t_{ACC}(min) on the MCU side.
- The access time from the read strobe on the SRAM side t_{OE}*(max) ≤ t_{OE}(min) on the MCU side.

When designing the read timing to fulfill the specification of t_{PDS}, the above mentioned specification on the MCU side concerning t_{ACC} and t_{OE} does not need to be considered.

Note: "*" represents the timing specification on the SRAM (R1LV5256ESA-7SR) side used in this application note.

6.2 File Composition

Table 6.1 lists the file used in the sample code. The files generated automatically in the integrated development environment are excluded in this table.

Table 6.1 File Used in the Sample Code

File Name	Outline	Remarks
bscsram.c	PFC and BSC setting	

6.3 Function

Table 6.2 lists the function.

Table 6.2 Function

File Name	Outline	Remarks
io_init_bscsram	PFC and BSC setting	

6.4 Function Specification

The following table lists the function specification in the sample code.

io_init_bscsram	
Outline	PFC and BSC setting
Header	
Declaration	void io_init_bscsram(void)
Description	Sets for PFC and BSC. • Sets the pin function PA17 to PA15 to outputs $\overline{RD}$, $\overline{WRL}$, and $\overline{WRH}$. • Sets the pin function PA0 to $\overline{CS0}$ output. • Sets the pin function PC15 to PC1 to outputs A15 to A1. • Sets the pin function PD15 to PD0 to inputs/outputs D15 to D0. • Idle between read and write in the same space/different spaces: 1 cycle • Interface: normal space interface • Endian: big endian • Data bus width: 16 bits • External wait mask specification: ignore the external wait input • Delay cycles from address and assertions $\overline{CS0}$ to $\overline{RD}$, $\overline{WRL}$, and $\overline{WRH}$: 1.5 cycles • Access wait cycles: 2 cycles • Delay cycles from negates $\overline{RD}$, $\overline{RD}$, and $\overline{WRL}$ to: 0.5 cycles
Arguments	None
Return Value	None

6.5 Flowchart

Figure 6.3 shows the procedure of PFC setting and BSC setting.

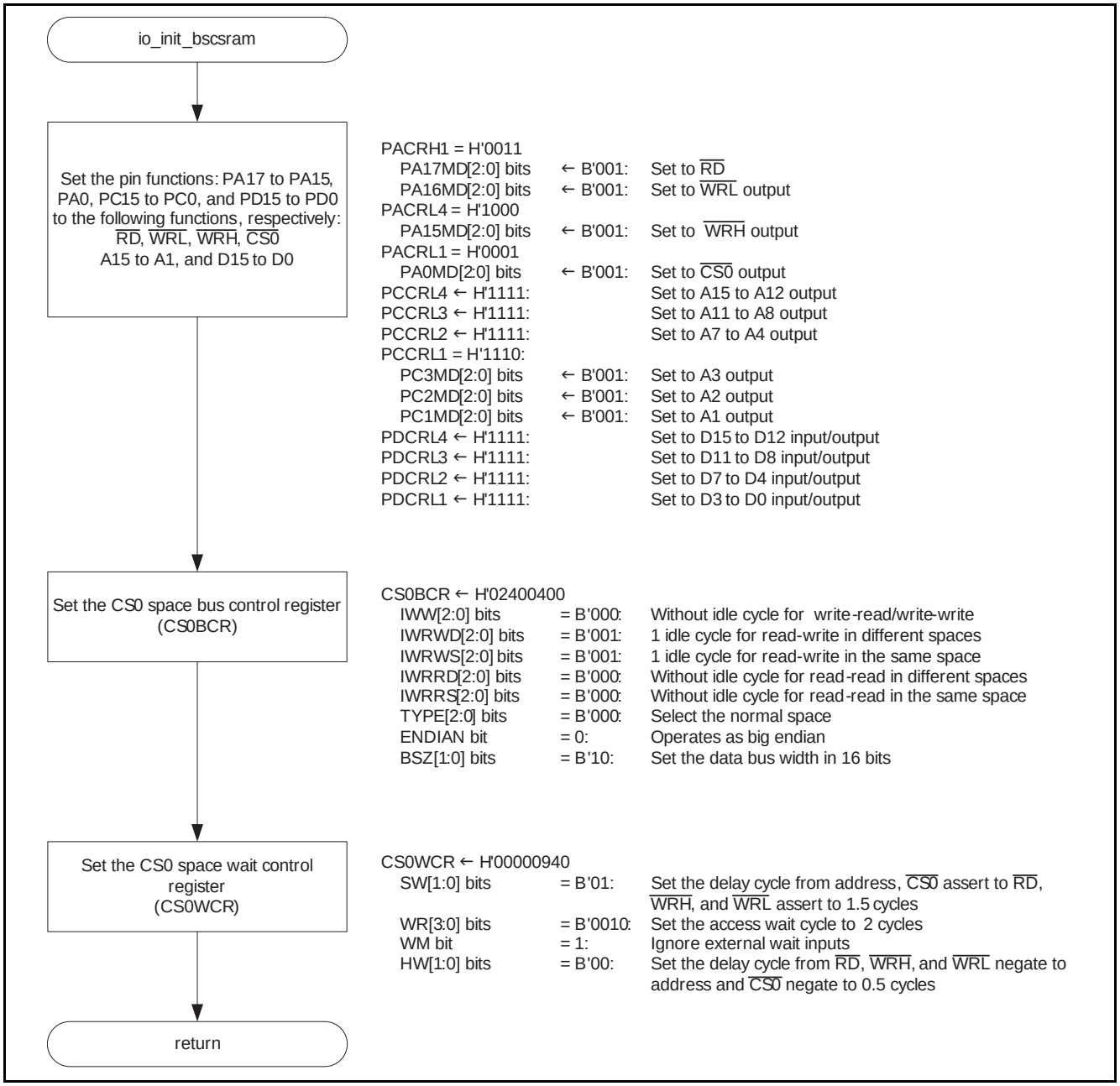

Figure 6.3 Procedure of PFC Setting and BSC Setting

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware

SH7239 Group, SH7237 Group User's Manual: Hardware Rev.1.00 (R01UH0086EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01 (R20UT0704EJ)
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	SH7239 Group Application Note Connecting SRAM with the Bus State Controller

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 16, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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