SH7231 Group

Data Transfer to an Internal Peripheral Module Using the DMAC

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Abstract

This application note describes a sample program for the SH7231 Group MCUs that uses the direct memory access controller (DMAC) to transfer data to an internal peripheral module.

The operation of this program has the following features.

- Use of DMAC channel 1
- Use of the serial communications interface (SCI channel 0) transmit data empty state as the DMA transfer start factor.
- Use of cycle stealing mode as the bus mode
- The transfer source is internal RAM and the transfer destination is the transmit data register of the SCI channel 0. Character string data stored in internal RAM is transmitted from the SCI.

Products

SH7231

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This application note uses the direct memory access controller (DMAC) to transfer data from internal RAM to the serial communications interface (SCI channel 0).

The sample program transmits character string data stored in internal RAM from SCI channel 0 by using DMA transfers. The DMAC is set to cycle stealing mode and the SCI channel 0 transmit data empty state is used as the DMA transfer start factor. The transfer data size is set to single byte transfers and the transfer count is taken to be exactly the size of the transfer source character string data. Note that transfer count is one transfer for each transfer request.

Table 1.1 lists the peripheral functions used and their uses and figure 1.1 shows the block diagram of the peripheral functions used.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Direct memory access controller (DMAC)	DMA data transfers
Internal RAM	Transfer source
Serial communications interface (SCI channel 0)	Transfer destination

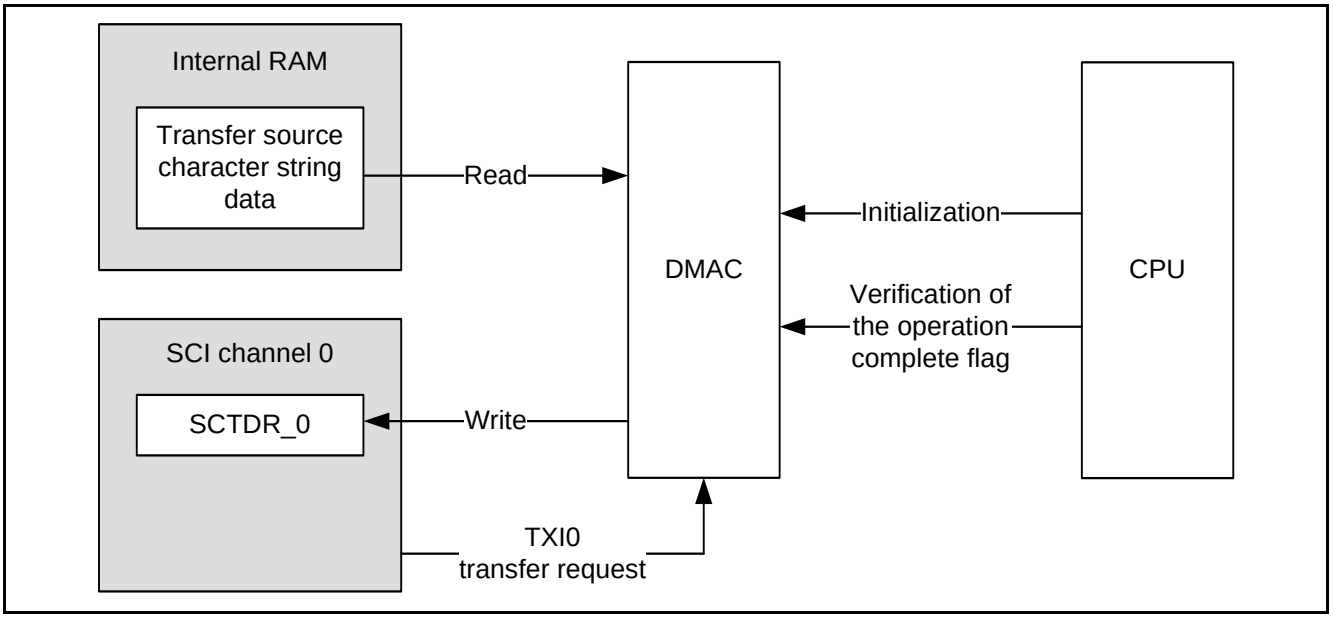


Figure 1.1 Used Peripheral Function Block Diagram

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed to run normally following conditions.

Table 2.1 Operating Conditions

Item	Contents
MCU used	SH7231
Operating frequency	Main clock: 100 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Operating voltage	Vcc: 3.3 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.08.00
C compiler	Renesas Electronics Renesas SuperH RISC engine Family C/C++ Compiler Package Ver.9.04 Release 00
	Compiler options: -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo
Operating mode	Single-chip mode
Version of the sample code	1.00
Board used	R0K572310C000BR

3. Reference Application Note

The following application note is related to this document and should be referred to when using this application note.

- SH7231 Group Example of Initialization (R01AN0322EJ)

4. Peripheral Functions

4.1 Direct Memory Access Controller (DMAC)

This section describes the direct memory access controller (DMAC). The basic description of this peripheral module is included in the SH7231 Group User's Manual: Hardware document.

When there are DMA transfer requests, the DMAC starts the transfer according to a predetermined channel priority and when the transfer complete conditions are met, it terminates the transfer. There are three transfer request modes: auto-request, external request, and internal peripheral module request. The bus mode can be selected to be either burst mode or cycle stealing mode.

Table 4.1 provides an overview of the DMAC. Figure 4.1 shows an example of a cycle stealing normal mode DMA transfer, and figure 4.2 shows an example of a burst mode DMA transfer. Figure 4.3 shows the block diagram for the DMAC.

Table 4.1 DMAC Overview

Item	Description
Number of channels	4 channels, CH0 to CH3 (Only the two channels CH0 and CH1 can accept external requests.)
Address space	4 GB (Logical address space)
Transfer data lengths	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address modes	Single address mode and dual address mode
Transfer requests	External requests, internal peripheral module requests, auto-requests (SCI: 8 factors, SCIF: 8 factors, IIC3: 2 factors, LVDS: 1 factor*, A/D converter: 2 factors, MTU2S: 2 factors, MTU2: 5 factors, CMT2: 5 factors, CMT: 2 factors, RSPI: 2 factors, RCAN-ET: 1 factor)
Bus modes	Cycle stealing mode (normal mode and intermittent mode), burst mode
Priority	Channel priority fixed mode, round robin mode
Interrupt requests	CPU interrupt requests can be generated at data transfer 1/2 complete and at data transfer complete.
External request detection	Low or high level detection and rising or falling edge detection for the DREQ input
Transfer request accept signal and transfer complete signal	The active levels for the DACK and TEND signals can be set.

Note: * Only the SH72315A has the internal peripheral module LVDS factor as a transfer request.

In cycle stealing normal mode, the DMAC releases bus rights to another bus master each time the transfer of a single transfer unit (byte, word, longword, or 16-byte unit) completes. If there is a transfer request after that, the DMAC reacquires bus rights from the other master, once again performs a single transfer unit transfer, and when that transfer completes releases bus rights to another bus master. This operation is repeated until the transfer complete conditions are met.
Cycle stealing normal mode can be used in all transfer periods, regardless of the transfer request source, transfer source, or transfer destination.

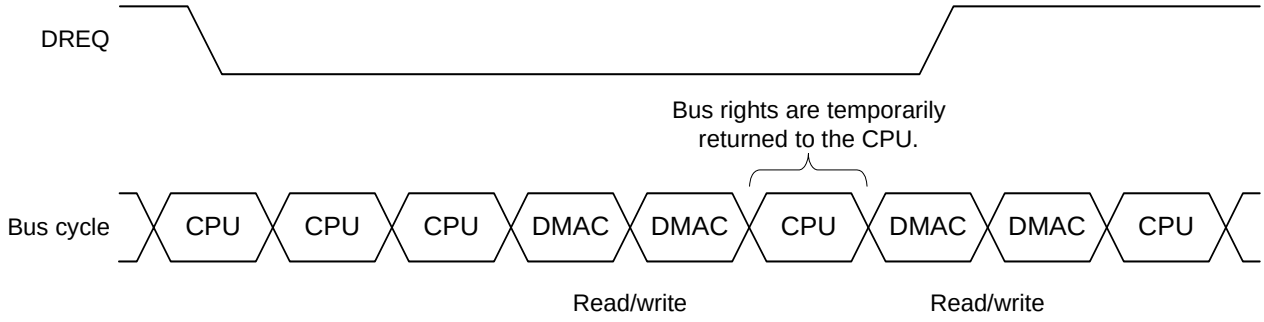


Figure 4.1 Cycle Stealing Normal Mode DMA Transfer Example (dual address, DREQ low-level detection)

In burst mode, once the DMAC has acquired bus rights, it continues the transfer operations without releasing those rights until the transfer complete conditions are met. However, in external request mode when level detection is used for DREQ, if the DREQ signal transitions away from the active level, after the DMAC transfer request that was already accepted completes, bus rights will be passed to another bus master, even if the transfer complete conditions are not met.

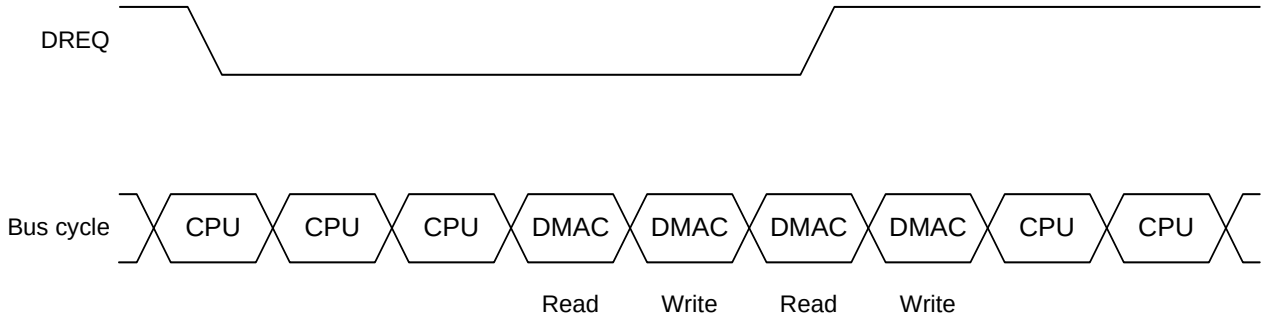


Figure 4.2 Bus Mode DMA Transfer Example (dual address, DREQ low-level detection)

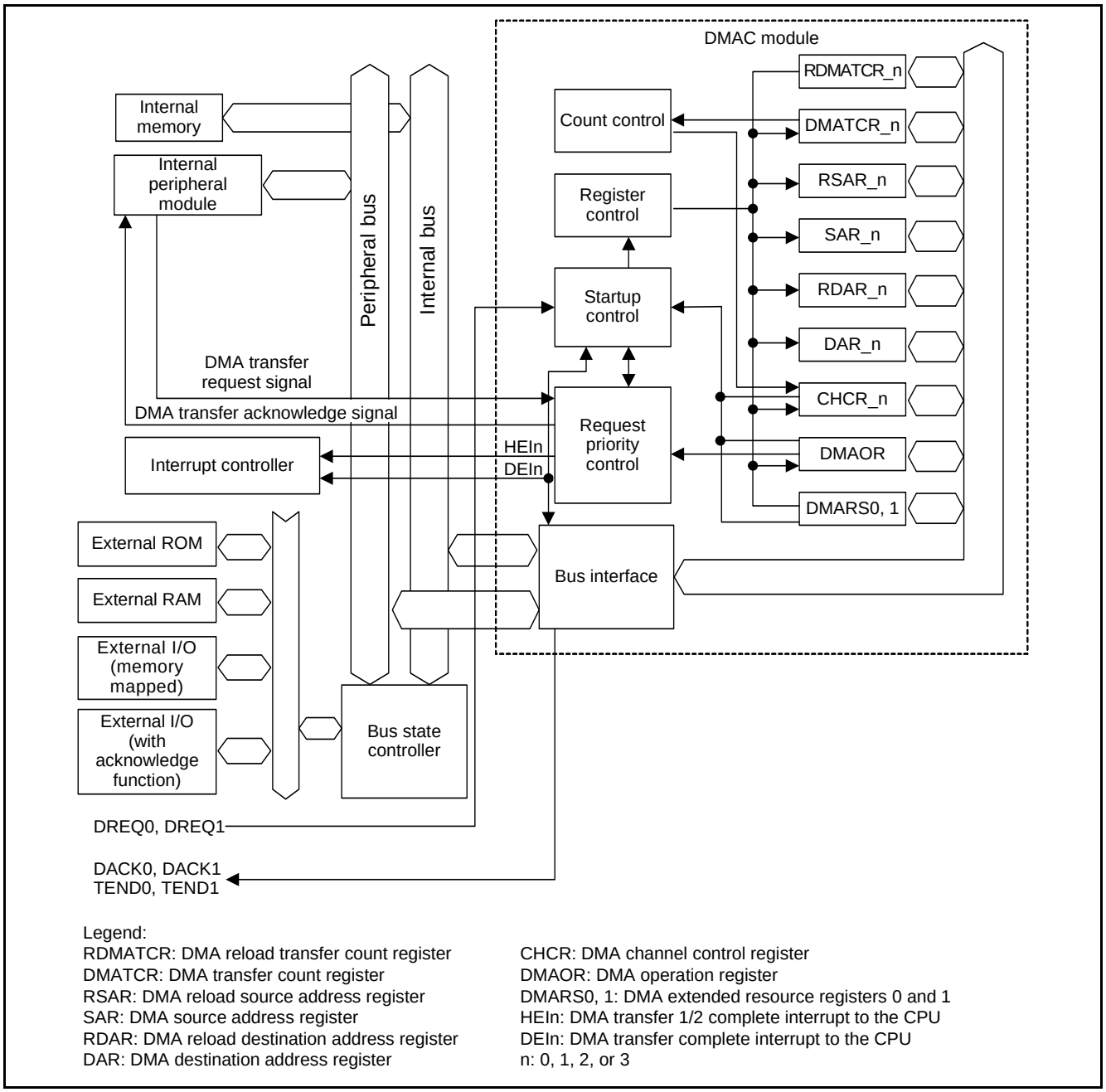


Figure 4.3 DMAC Block Diagram

4.2 Serial Communications Interface (SCI)

This section describes the serial communications interface (SCI). The basic description of this peripheral module is included in the SH7231 Group User's Manual: Hardware document.

The SCI supports two transfer methods: asynchronous communication and clock synchronous communication. When asynchronous communication is used, one of twelve serial data communication formats may be selected. The asynchronous communication mode also provides a function (the multiprocessor communications function) that supports communication between multiple processors.

Table 4.2 presents an overview of the SCI. Figure 4.4 shows an example of the data formats that can be used in asynchronous communication and figure 4.5 shows an example of the data formats that can be used in clock synchronous communication. Furthermore, figure 4.6 shows the SCI block diagram.

Table 4.2 SCI Overview

Item	Contents
Number of channels	Four channels (channels 0 to 3)
Communication modes	• Asynchronous serial communication and clock synchronous serial communication. • Full duplex communication is supported.
Communication formats in asynchronous communication	Data length: 7 or 8 bits Stop bits: 1 or 2 bits Parity: even, odd, or no parity
Clock sources	Baud rate generator (internal clock) or SCK input pin (external clock)
Interrupts	Transmit data empty interrupt, transmission complete interrupt, receive data full interrupt, and reception error
Other features	• Supports multiprocessor communication • Reception error detection • Break detection • Either LSB or MSB first may be selected (except when the 7-bit data length is used in asynchronous communication).

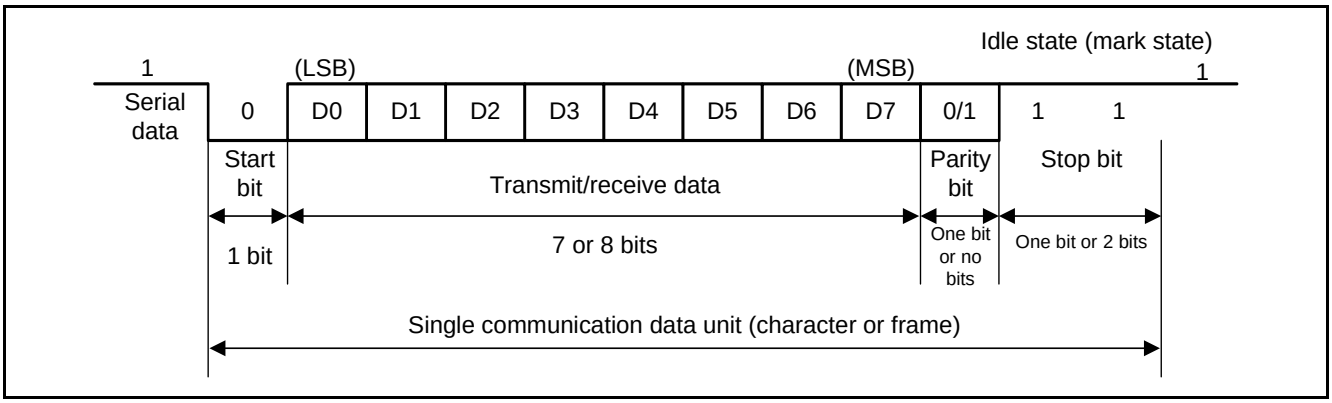


Figure 4.4 Asynchronous Communication Data Format Examples

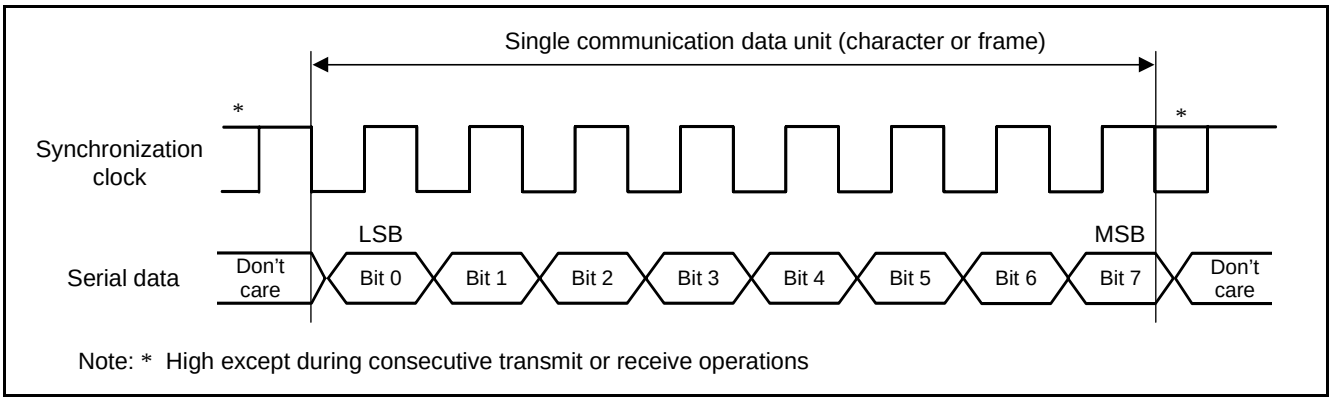
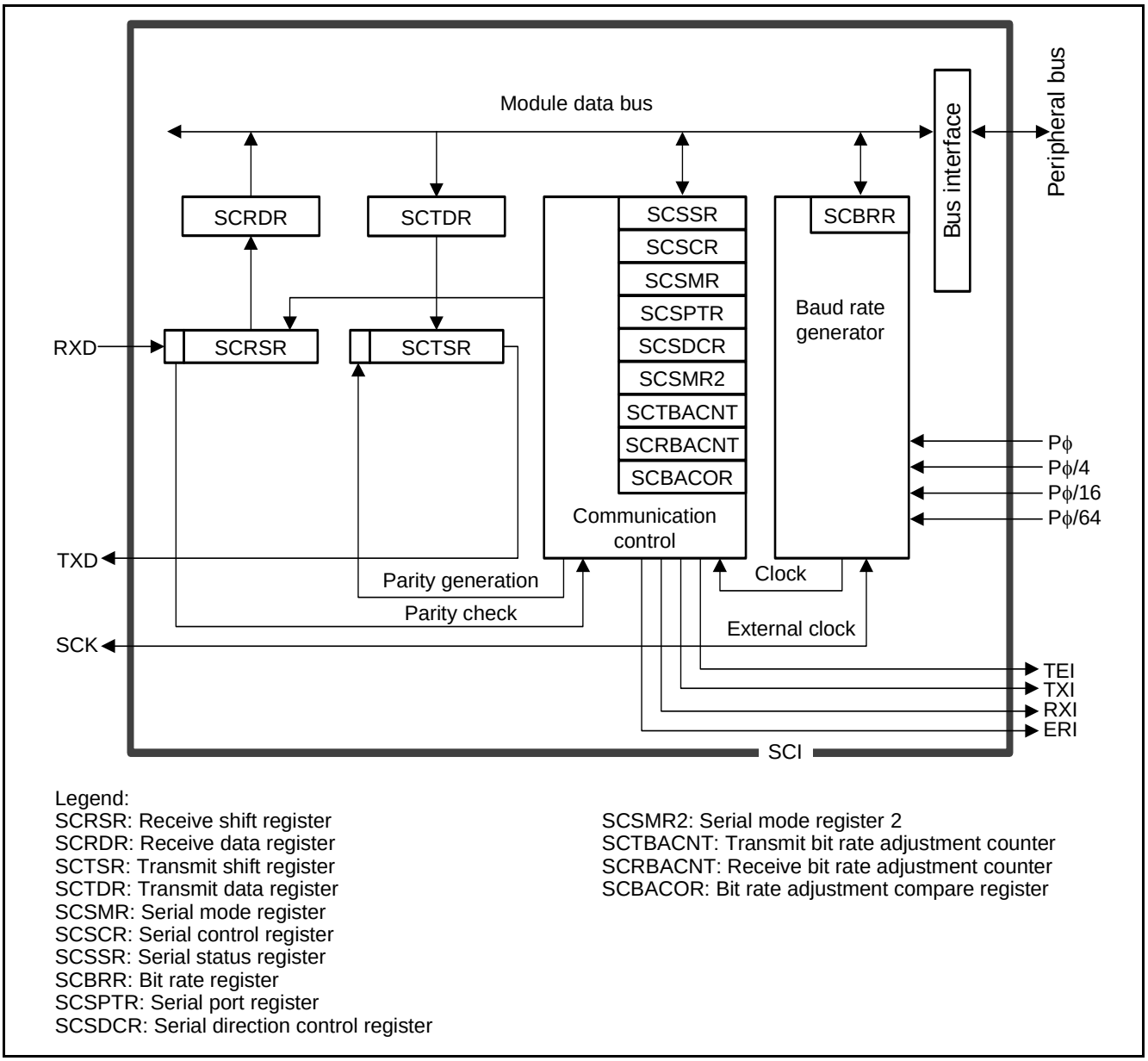


Figure 4.5 Clock Synchronous Communication Data Format Examples



Legend:
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register
SCSMR2: Serial mode register 2
SCTBACNT: Transmit bit rate adjustment counter
SCRBACNT: Receive bit rate adjustment counter
SCBACOR: Bit rate adjustment compare register

Figure 4.6 SCI Block Diagram

5. Hardware

5.1 Pin Used

Table 5.1 lists the pin used and its function.

Table 5.1 Pin Used and Its Function

Pin Name	I/O	Description
PA1/TXD0	Output	Asynchronous transmit data

6. Software

6.1 Operation Overview

The sample program first sets up the DMAC and SCI and then enables the DMAC. During SCI initialization, the SCI transmit data register (SCTDR) is in the empty state. Therefore, when the DMAC is enabled, a DMA transfer from the transfer source memory area to the SCTDR register will start by the DMA transfer request due to the transmit data empty state. The data written to the SCTDR register will be transmitted from the TXD pin in the communication format set in the SCI.

Table 6.1 lists the DMAC settings and table 6.2 lists the SCI settings. Figure 6.1 presents an overview of this operation and figure 6.2 shows the operation timing.

Table 6.1 DMAC Settings

Item	Description
Channel used	CH0
Transfer data length	Byte
Transfer count	Number of bytes in the character string that will be the transfer source
Address mode	Dual address mode
Transfer request	TXI0 (SCI channel 0 transmit data empty interrupt)
Bus mode	Cycle stealing mode (normal mode)
Priority	Channel priority fixed mode
Interrupt	Interrupts disabled

Table 6.2 SCI Settings

Item	Description
Channel used	CH0
Communication mode	Asynchronous
Data length	8 bits
Stop bit	1 bit
Parity	None
Clock source	Baud rate generator (internal clock)
Baud rate	9,600 bps
Interrupt	The TXI0 interrupt (transmit data empty interrupt) is enabled. (Note, to enable DMA transfer requests, this interrupt is unused in practical.)

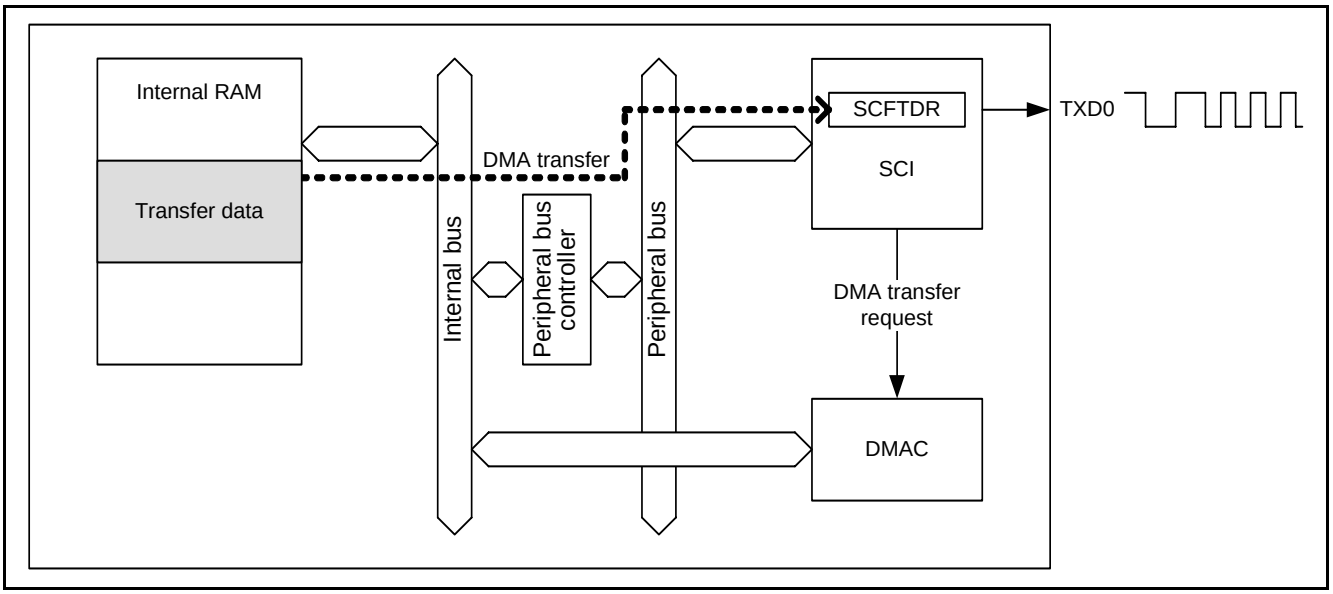


Figure 6.1 Operation Overview

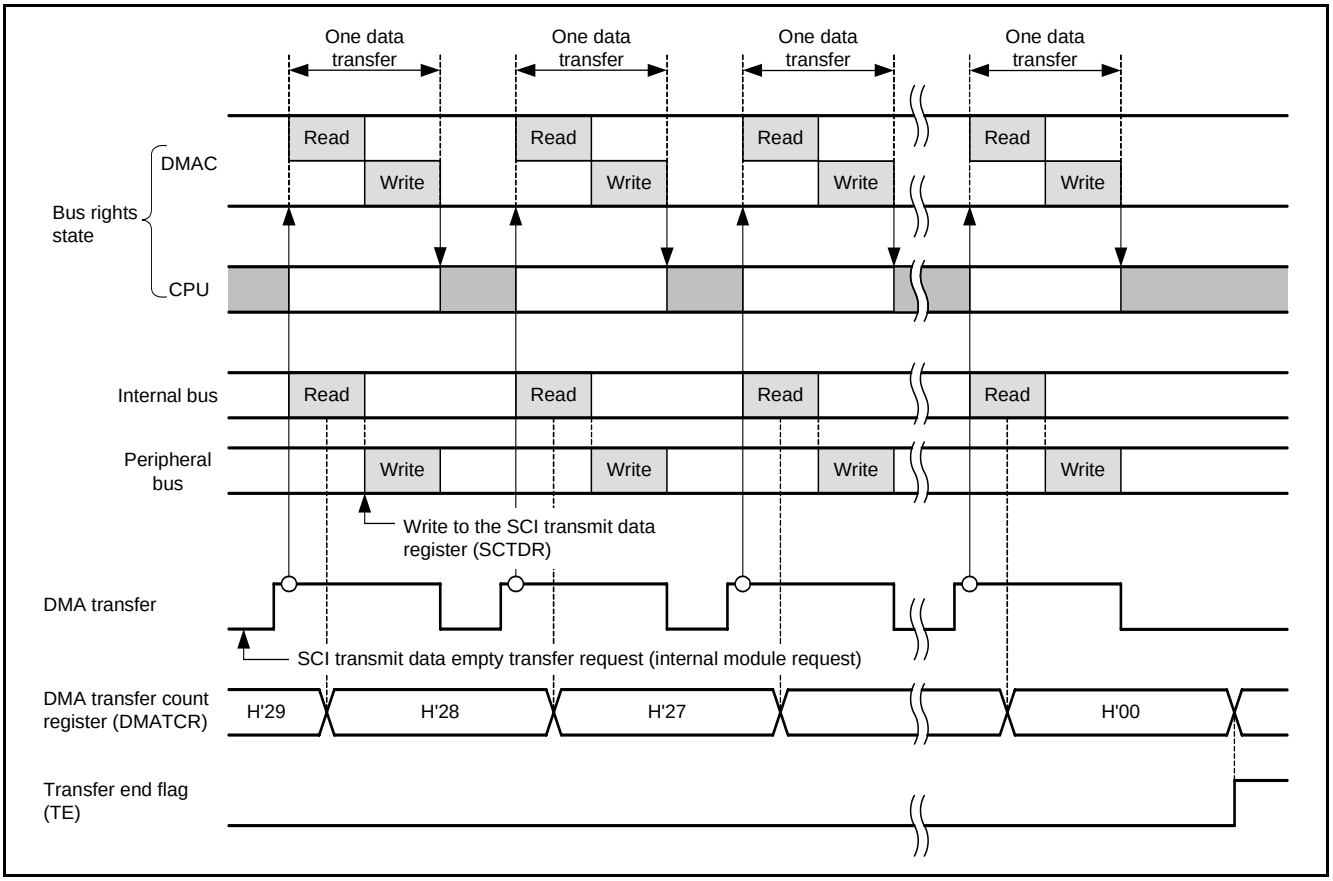


Figure 6.2 Operation Timing

6.2 File Composition

Table 6.3 lists the file used in the sample code. Files not generated by the integrated development environment should not be listed in this table.

Table 6.3 File Used in the Sample Code

File Name	Outline	Remarks
main.c	Main module	Initialization and DMA transfer processing

6.3 Structures and Enumerations

Figure 6.3 shows the structures and enumerations used in the sample program.

```
typedef enum
{
      DMA_SIZE_BYTE,                    /* 8bit Transfer */
      DMA_SIZE_WORD,                    /* 16bit Transfer */
      DMA_SIZE_LONG,                    /* 32bit Transfer */
      DMA_SIZE_16B                      /* 16Byte Transfer */
} dma_size_t;

typedef enum
{
      DMA_INT_DISABLE,
      DMA_INT_ENABLE
} dma_int_ctrl_t;

typedef struct
{
      dma_size_t size;                  /* size of transfer */
      dma_int_ctrl_t int_ctrl;          /* mode of interrupt */
} dma_mode_t;

typedef struct
{
      uint8_t scbrr;                    /* setting of SCBRR */
      uint8_t scsmr;                    /* setting of SCSMR */
} sci_baud_setting_t;

typedef enum
{
      BAUD_1200,                        /*   1,200 bps */
      BAUD_2400,                        /*   2,400 bps */
      BAUD_4800,                        /*   4,800 bps */
      BAUD_9600,                        /*   9,600 bps */
      BAUD_19200,                       /*  19,200 bps */
      BAUD_31250,                       /*  31,250 bps */
      BAUD_38400,                       /*  38,400 bps */
      BAUD_57600,                       /*  57,600 bps */
      BAUD_115200                       /* 115,200 bps */
} sci_baud_t;
```

Figure 6.3 Structures and Enumerations Used in the Sample Code

6.4 Variables

Table 6.4 lists the global variable and table 6.5 lists the const variables.

Table 6.4 Global Variable

Type	Variable Name	Contents	Function Used
int8_t	g_send_strings[]	Array that holds the character string transmitted from the SCI via DMA transfer.	main

Table 6.5 const Variables

Type	Variable Name	Contents	Function Used
dma_mode_t	g_dma_mode	DMA transfer mode setting value	main
sci_baud_setting_t	g_sci_baud_ settings[]	Array of baud rate setting data that corresponds to the various communication rates.	io_sci_init

6.5 Functions

Table 6.6 lists the functions.

Table 6.6 Functions

Function Name	Outline
main	Main processing
io_sci_init	SCI initialization
io_dma_init	DMAC initialization
io_dma_enable	Enable DMA transfers
io_dma_poll_end	Wait for DMA transfer completion

6.6 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	
Declaration	void main(void)
Description	After initializing the DMAC and SCI, main() enables DMA transfers and waits for completion of the transfer. After that, it enters an infinite loop.
Arguments	None
Return Value	None

io_sci_init	
Outline	SCI initialization
Header	
Declaration	void io_sci_init(sci_baud_t boudrate)
Description	After clearing the SCI module standby state, this function sets the SCI registers.
Arguments	sci_baud_t boudrate : SCI baud rate
Return Value	None

io_dma_init	
Outline	DMAC initialization
Header	
Declaration	void io_dma_init(uint32_t src_addr, uint32_t dst_addr, uint32_t data_size, dma_mode_t mode)
Description	After clearing the DMAC module standby state, this function sets the DMAC registers.
Arguments	uint32_t src_addr : Transfer source memory area address uint32_t dst_addr : Transfer destination memory area address uint32_t data_size : Transfer data size dma_mode_t mode : DMA transfer mode settings
Return Value	None

io_dma_enable	
Outline	Enable DMA transfers
Header	
Declaration	void io_dma_enable(void)
Description	Enables DMA transfers.
Arguments	None
Return Value	None

io_dma_poll_end	
Outline	Wait for DMA transfer completion
Header	
Declaration	void io_dma_poll_end(void)
Description	After waiting for completion of the DMA transfer, disables DMA transfers.
Arguments	None
Return Value	None

6.7 Flowcharts

6.7.1 Main Processing

Figure 6.1 shows the main processing.

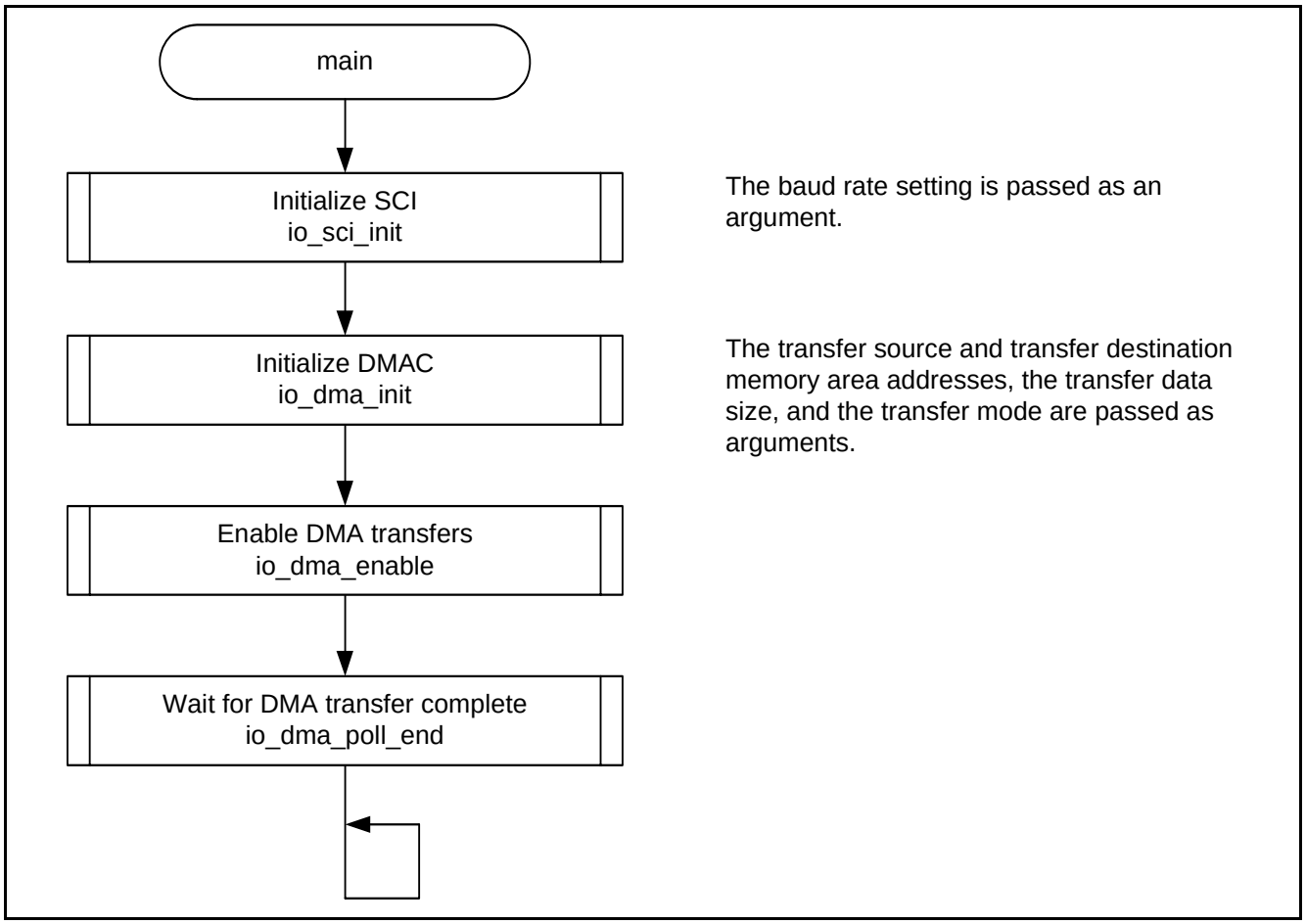


Figure 6.1 Main Processing

6.7.2 SCI initialization

Figure 6.5 shows the flowchart for SCI initialization.

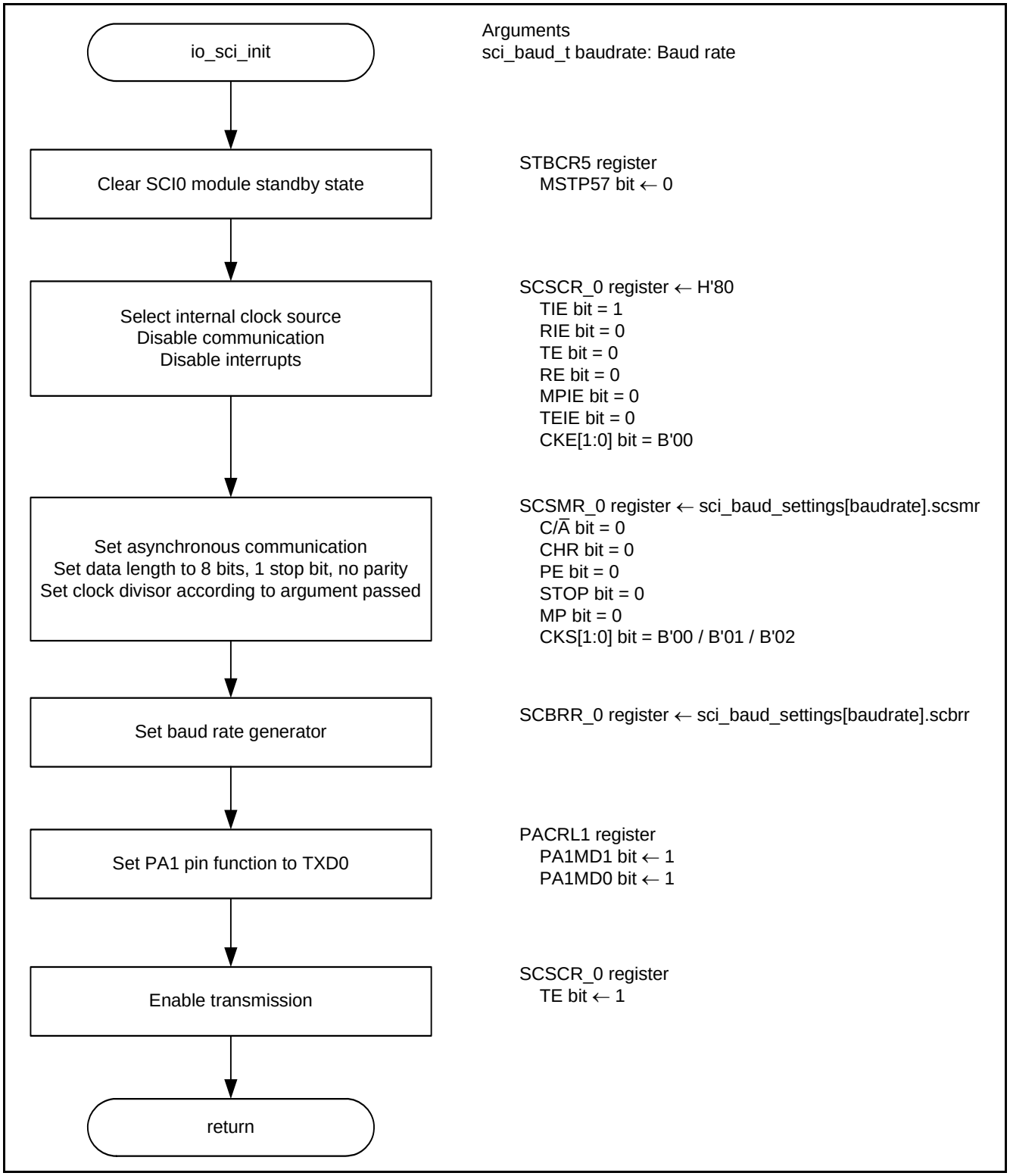


Figure 6.5 SCI Initialization

6.7.3 DMAC initialization

Figure 6.6 shows the flowchart for DMAC initialization.

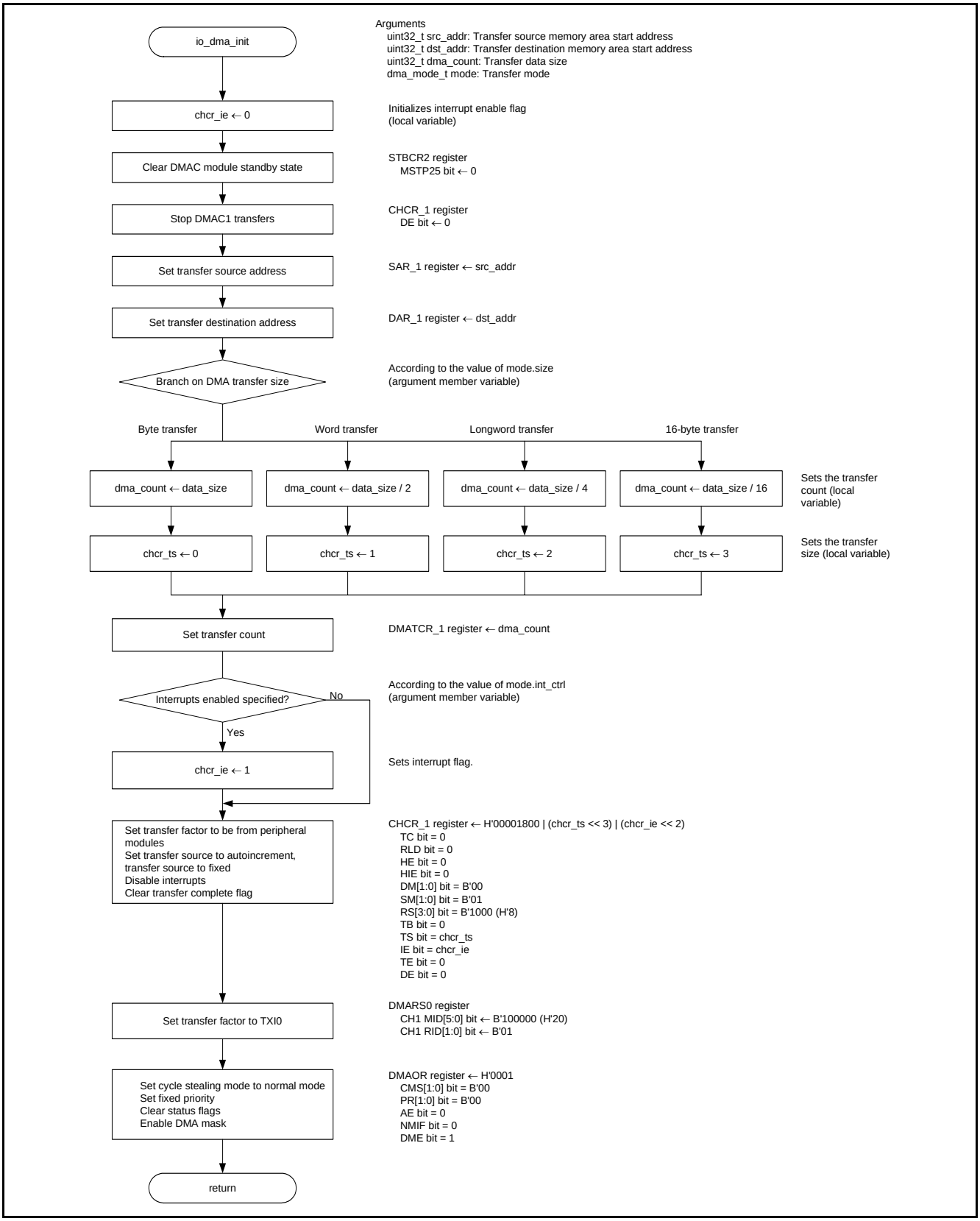


Figure 6.6 DMAC Initialization

6.7.4 Start DMA transfer

Figure 6.7 shows the flowchart for enabling DMA transfers.

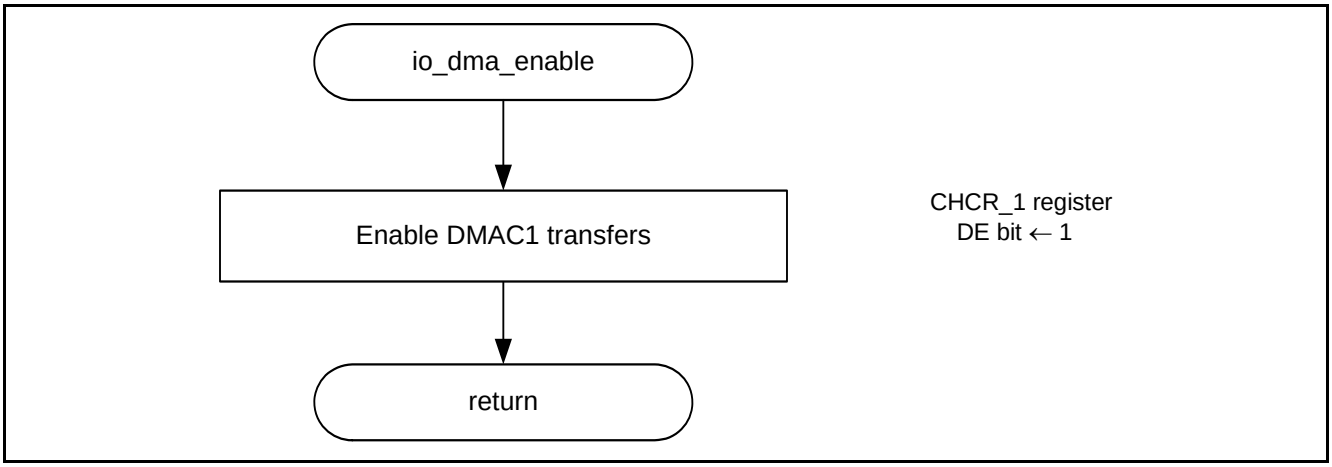


Figure 6.7 Enabling DMA Transfers

6.7.5 DMA Transfer End Processing

Figure 6.8 shows the flowchart for DMA transfer end processing.

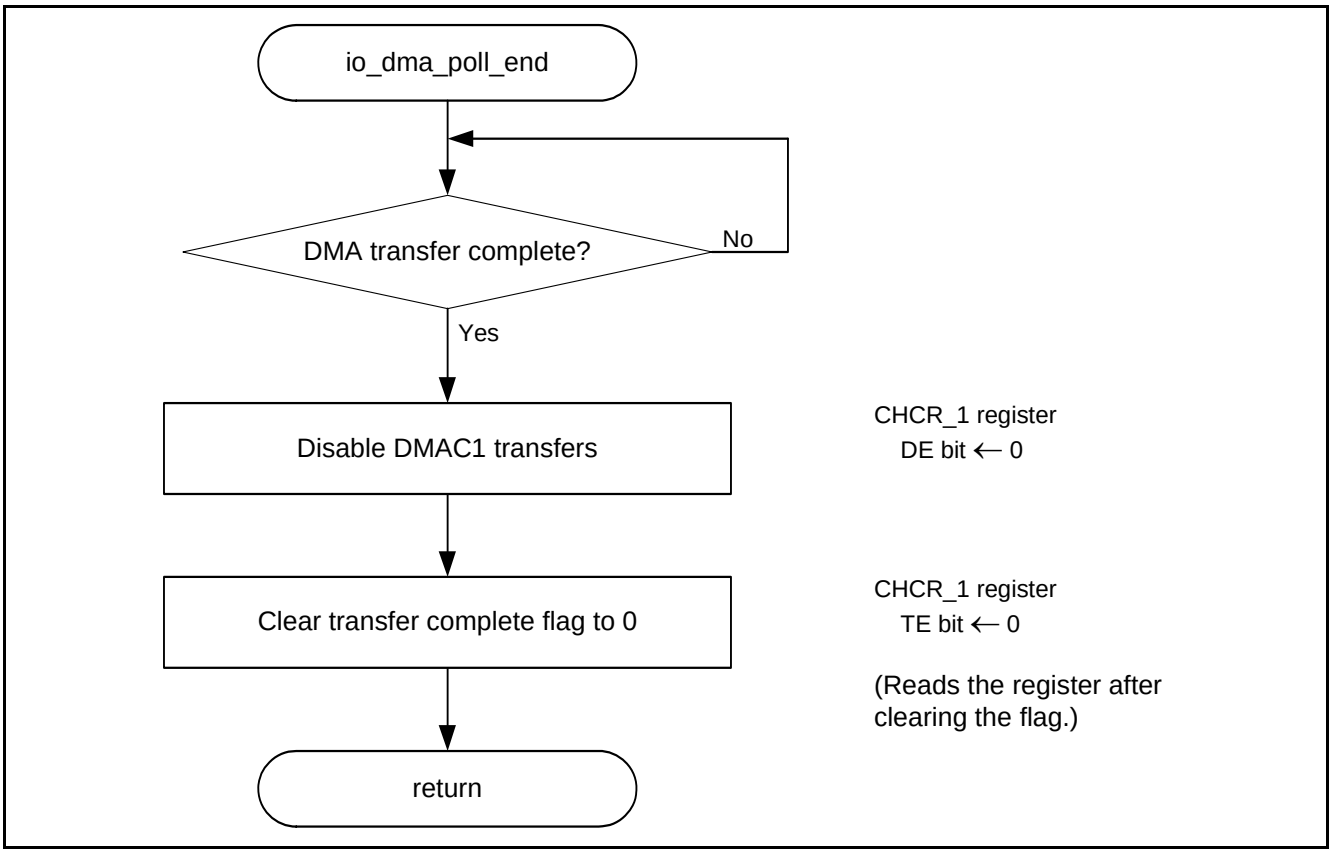


Figure 6.8 DMA Transfer End Processing

7. Reference Documents

- User's Manual: Hardware
  SH7231 GroupUser's Manual: Hardware Rev.2.00 (R01UH0073EJ)
  The latest version can be downloaded from the Renesas Electronics website.

- Software Manual
  SH-2A, SH2A-FPU User's Manual: Software Rev.4.00 (R01US0031EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

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REVISION HISTORY	SH7231 Group Application Note Data Transfer to an Internal Peripheral Module Using the DMAC

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 07, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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