SH7231 Group

Example of Initialization

R01AN0322EJ0100
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Summary

This application note gives an example of configuration items to activate the SH7231 Microcomputers (MCUs).

Target Device

SH7231 MCU

Contents

1. Introduction

1.1 Specifications

Configure the clock pulse generator (CPG) after the reset release.

1.2 Modules Used

- Clock pulse generator (CPG)

1.3 Applicable Conditions

MCU	SH7231 (R5F72315A)
Operating Frequency	Internal clock: 100 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated Development Environment	Renesas Electronics High-performance Embedded Workshop Ver.4.08.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.04 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu - fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7231 application notes assume to use the sample program described in this application note as the configuration program.

2.1 Sample Program

The configuration program consists of several source files such as the resetprg.c, describing the PowerON_Reset_PC function, and the hwsetup.c, describing the hardware setup function. Main source files are as follows.

- resetprg.c
- hwsetup.c
- cpg.c

"resetprg.c" is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the PowerON_ResetPC function. The PowerON_ResetPC function initially executed after the reset is canceled. Its beginning address is set in the reset vector defined by the vecttbl.c.

"hwsetup.c" describes the HardwareSetup function called by the PowerON_Reset_PC function. The HardwareSetup function calls the io_set_cpg function to set the CPG. When using the external bus interface such as interfacing SDRAM, call the io_set_cpg function, and then add processing to set the Bus State Controller (BSC) to the HardwareSetup function as appropriate.

"cpg.c" describes the io_set_cpg function which is called from the HardwareSetup function. The io_set_cpg function initially sets the Frequency control register (FRQCR), and subsequently sets the MTU2S clock frequency control register (MCLKCR) and also the AD clock frequency control register (ACLKCR). Then the io_set_cpg function finally cancels the module standby function for internal peripheral modules.

Figure 1 shows flow charts of the configuration program in above source files used in this application.

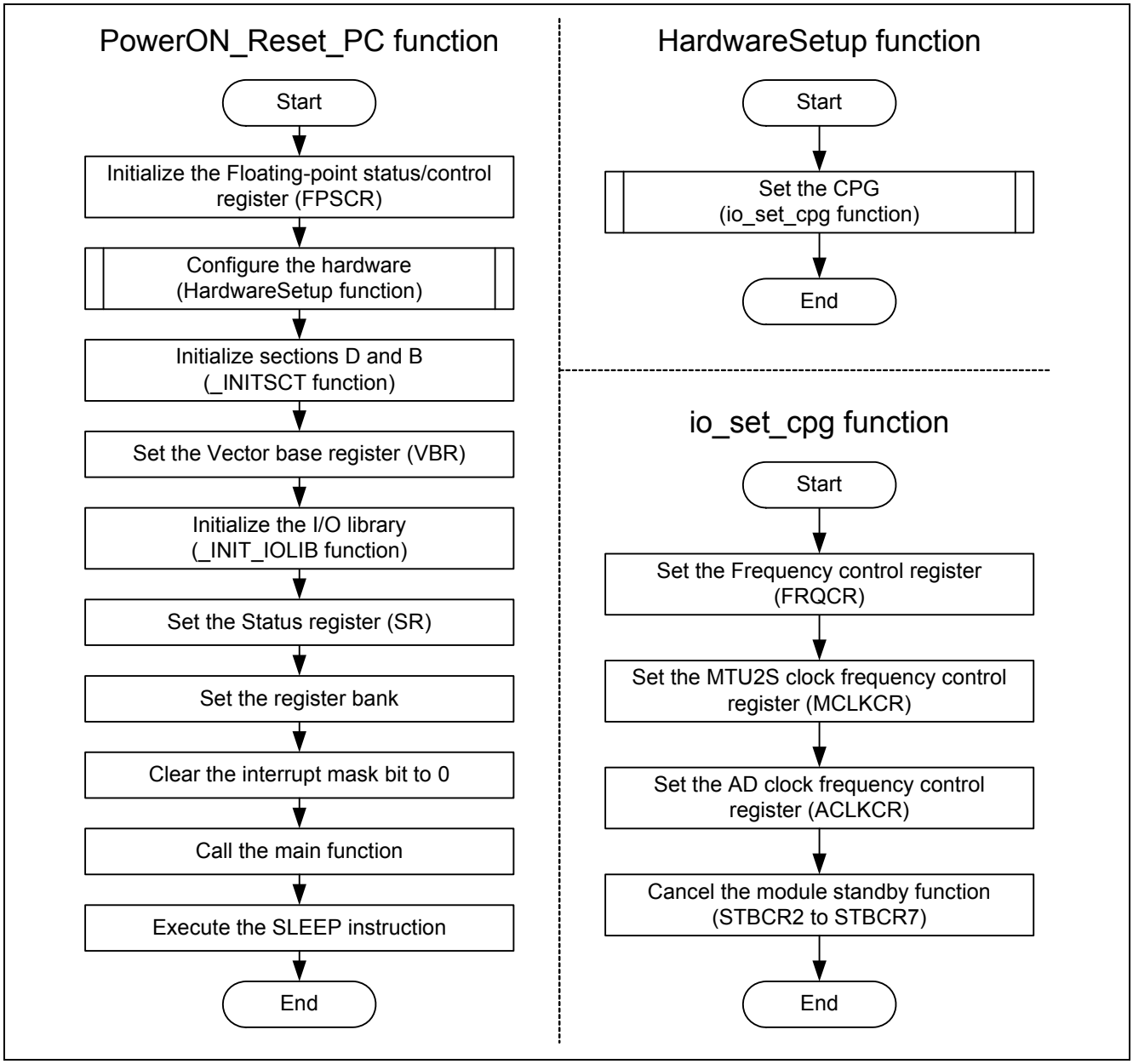


Figure 1 Flow Charts of Functions (PowerON_Reset_PC, HardwareSetup, and io_set_cpg)

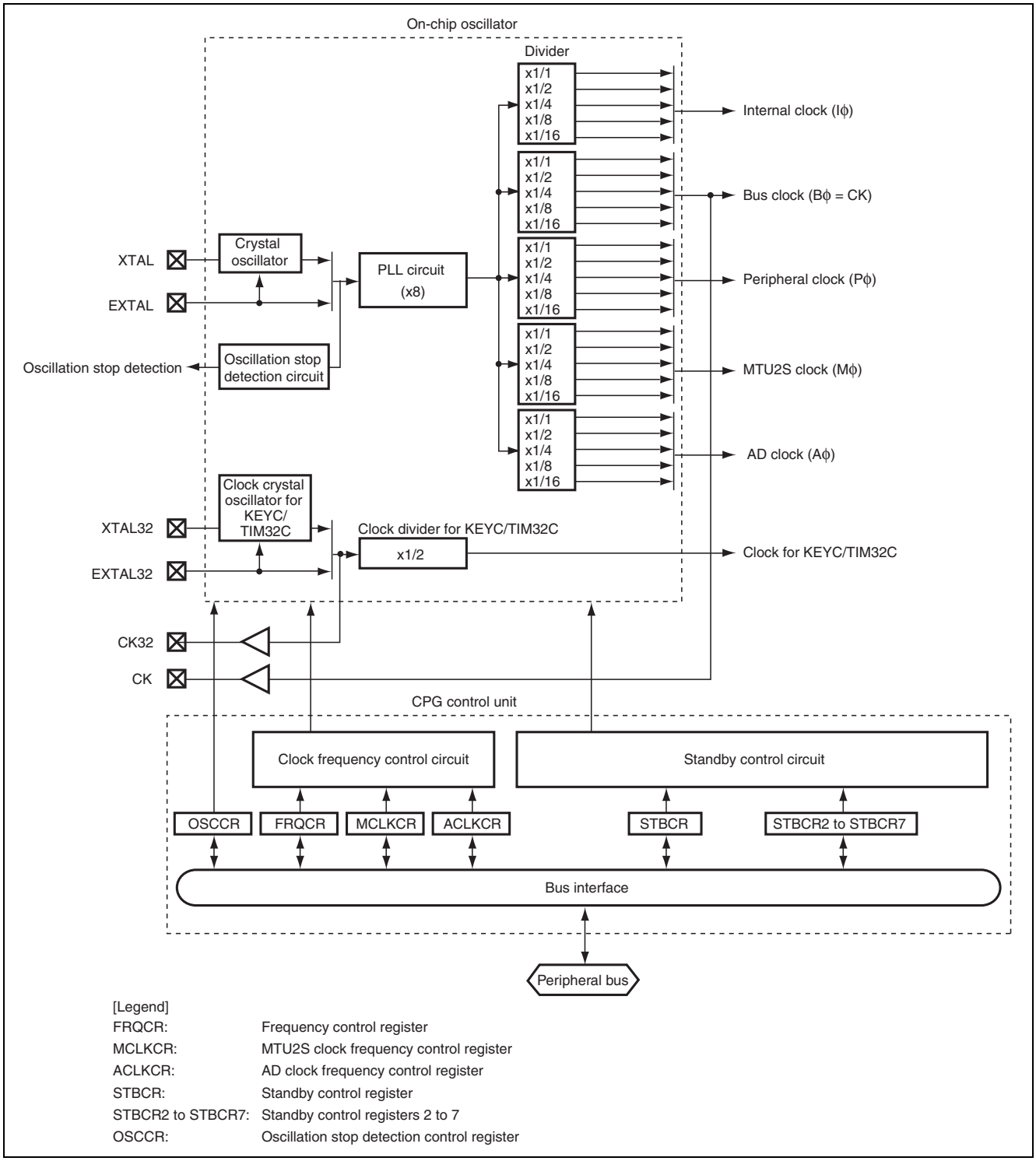
2.2 CPG Operation

The CPG generates an internal clock (Iφ), a bus clock (Bφ), a peripheral clock (Pφ), an MTU2S clock (Mφ), and an AD clock (Aφ), as well as controlling power-down mode.

The following table gives an overview of the CPG. Figure 2 shows the CPG block diagram.

Table 1 CPG Overview

Item	Description	
Generate clock	• Internal clock (Iφ):	Used by the CPU
	• Bus clock (Bφ):	Used by the external bus interface
	• Peripheral clock (Pφ):	Used by the internal peripheral module
	• MTU2S clock (Mφ):	Used by the MTU2S module
	• AD clock (Aφ):	Used by the ADC module
Change frequency	• Sets frequencies for clocks independently using the PLL (Phase Locked Loop) and divider circuits in the CPG. • Changes frequency by software using the frequency control registers (FRQCR, MCLKCR, and ACLKCR).	
Control power-down mode	Stops clock in sleep mode or software standby mode. Stops the module specified by module standby function.	



[Legend]

FRQCR:	Frequency control register
MCLKCR:	MTU2S clock frequency control register
ACLKCR:	AD clock frequency control register
STBCR:	Standby control register
STBCR2 to STBCR7:	Standby control registers 2 to 7
OSCCR:	Oscillation stop detection control register

Figure 2 CPG Block Diagram

2.3 CPG Setting

The figure below shows the flow chart of setting CPG. Internal peripheral modules are in module standby mode after the reset release. The sample program cancels the module standby function for internal peripheral modules after setting the Frequency control register (FRQCR), the MTU2S clock frequency control register (MCLKCR), and the AD clock frequency control register (ACLKCR). For details on these registers, refer to the Clock Pulse Generator (CPG) chapter in the SH7231 Group Hardware User's Manual.

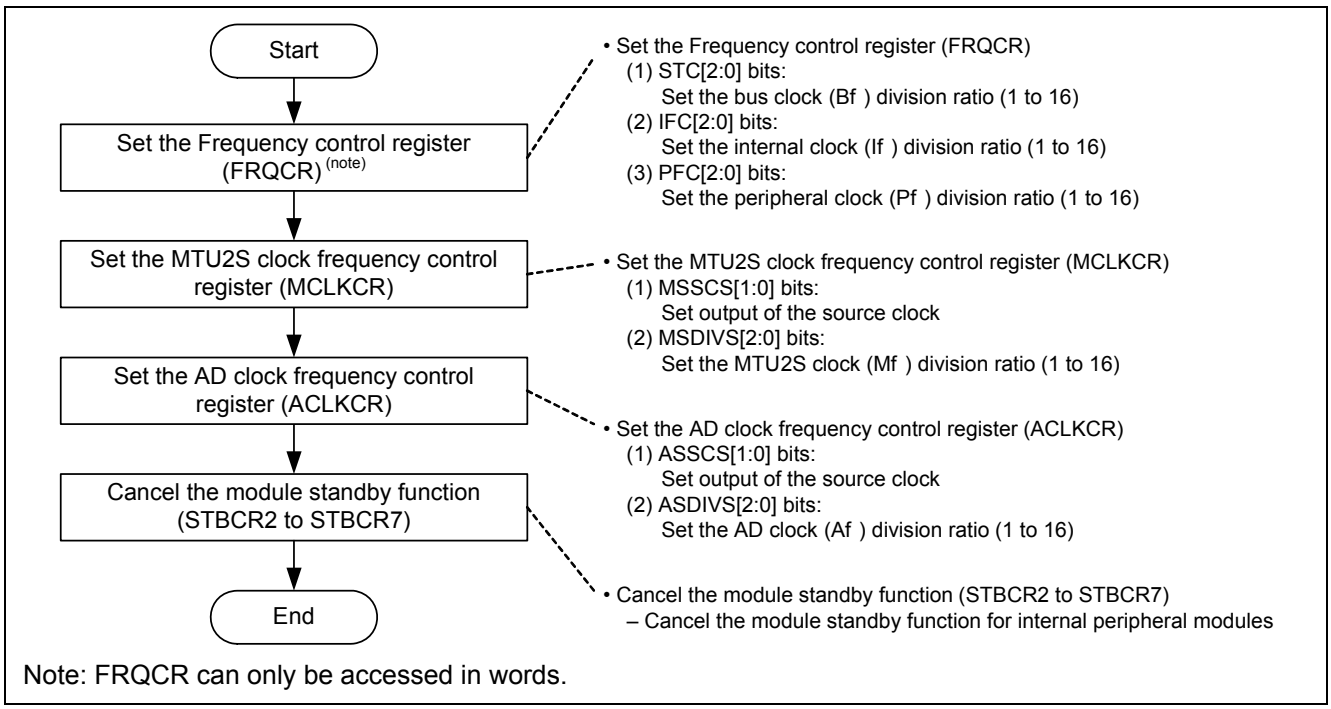


Figure 3 Flow Chart of CPG Setting

2.4 Setting in the Sample Program

Table 2 lists the setting in the sample program. Table 3 to Table 5 list register settings for each module.

Table 2 Module Setting in the Sample Program

Module	Setting
Floating point status/control unit (FPU)	• Precision mode Executes floating-point instructions in single-precision • Round mode Round to zero
Clock pulse generator (CPG)	• Clock frequency (input clock is 12.5 MHz) — Internal clock: 100 MHz — Bus clock: 50 MHz — Peripheral clock: 50 MHz — MTU2S clock: 100 MHz — AD clock: 50 MHz • Modules cancelled the module standby function UBC, DMAC, DTC, MTU2S, MTU2, IIC3, SCI0, SCI1, SCI2, SCI3, SCIF4, SCIF5, SCIF6, SCIF7, RSPI, CMT, CMT2, ADC0, ADC1, RCAN-ET, LVDS, TIM32C, KEYC

Table 3 CPG Register Settings (1/3)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	• STC[2:0] = "B'001": Bus clock (Bφ) division ratio: 2 • IFC[2:0] = "B'000": Internal clock (Iφ) division ratio = 1 • PFC[2:0] = "B'001": Peripheral clock (Pφ) division ratio = 2
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'40	• MSSCS[1:0] = "B'01": PLL output clock • MSDIVS[2:0] = "B'000": MTU2S clock (Mφ) division ratio = 1
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	• ASSCS[1:0] = "B'01": PLL output clock • ASDIVS[2:0] = "B'001": AD clock (Aφ) division ratio = 2

Table 4 CPG Register Settings (2/3)

Register Name	Address	Setting	Description
Standby control register 2 (STBCR2)	H'FFFE 0404	H'01	• MSTP27 = "0": H-UDI is operating • MSTP26 = "0": UBC is operating • MSTP25 = "0": DMAC is operating • MSTP24 = "0": FPU is operating • MSTP21 = "0": DTC is operating
Standby control register 3 (STBCR3)	H'FFFE 0408	H'00	• HIZ = "0": The pin state is held in software standby mode • MSTP36 = "0": MTU2S is operating • MSTP35 = "0": MTU2 is operating • MSTP33 = "0": IIC3 is operating • MSTP32 = "0": On-chip RAM (for high-speed access) is operating • MSTP31 = "0": On-chip RAM (for data retention) is operating • MSTP30 = "0": ROM and FLD are operating
Standby control register 4 (STBCR4)	H'FFFE 040C	H'01	• MSTP47 = "0": SCIF4 is operating • MSTP46 = "0": SCIF5 is operating • MSTP45 = "0": SCIF6 is operating • MSTP44 = "0": SCIF7 is operating • MSTP42 = "0": CMT is operating • MSTP41 = "0": CMT2 is operating

Table 5 CPG Register Settings (3/3)

Register Name	Address	Setting	Description
Standby control register 5 (STBCR5)	H'FFFE 0418	H'00	• MSTP57 = "0": SCI0 is operating • MSTP56 = "0": SCI1 is operating • MSTP55 = "0": SCI2 is operating • MSTP52 = "0": ADC1 is operating • MSTP51 = "0": ADC2 is operating • MSTP50 = "0": RSPI is operating
Standby control register 6 (STBCR6)	H'FFFE 041C	H'60	• MSTP67 = "0": LVDS is operating
Standby control register 7 (STBCR7)	H'FFFE 0500	H'00	• MSTP77 = "0": TIM32C is operating • MSTP76 = "0": KEYC is operating • MSTP[75:74] = "B'00": EXTAL32 and XTAL32 are connected to crystal resonator

3. Sample Program Listing

3.1 Sample Program Listing "resetprg.c" (1/3)

```
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***********************************************************************/
/* Copyright (C) 2011 Renesas Electronics Corporation. All rights reserved.   */
/***********************************************************************
* System Name  : SH7231 Sample Program
* File Name    : resetprg.c
* Abstract     : SH7231 Initial Setting
* Version      : 1.00
* Device       : SH7231
* Tool-Chain   : High-performance Embedded Workshop (Ver.4.08.00).
*              : C/C++ compiler package for the SuperH RISC engine family
*              :                             (Ver.9.04 Release00).
* OS           : None
* H/W Platform : R0K572310C000BR (CPU board)
* Description  :
***********************************************************************
* History      : May 16,2011 Ver.1.00
***********************************************************************/

```

3.2 Sample Program Listing "resetprg.c" (2/3)

```
45    /***********************************************************************
46    Includes   <System Includes> , "Project Includes"
47    ***********************************************************************/
48    #include <machine.h>
49    #include <_h_c_lib.h>
50    #include "stacksct.h"
51    #include "iodefine.h"
52
53    /***********************************************************************
54    Macro definitions
55    ***********************************************************************/
56    #define FPSCR_Init 0x00040001
57    #define SR_Init    0x000000f0
58    #define INT_OFFSET 0x10
59
60    /***********************************************************************
61    Imported global variables and functions (from other files)
62    ***********************************************************************/
63    /* ---- Function prototype ---- */
64    extern void main(void);
65    extern void HardwareSetup(void);
66    /* ---- Global variable ---- */
67    extern unsigned int INT_Vectors;
68
69    /***********************************************************************
70    Exported global variables and functions (to be accessed by other files)
71    ***********************************************************************/
72    void PowerON_Reset_PC(void);
73    void Manual_Reset_PC(void);
74
75    /* ==== Section name changed to ResetPRG ==== */
76    #pragma section ResetPRG
77
78    /* ==== Entry function specified ==== */
79    #pragma entry PowerON_Reset_PC
80
81    /***********************************************************************
82    * Outline      : CPU initialization
83    * Include      :
84    * Declaration  : void PowerON_Reset_PC(void);
85    * Description  : Executes the CPU initialization processing to register
86    *              : the power-on reset vector to the exception vector table.
87    *              : This function is executed first after power-on reset.
88    * Argument     : void
89    * Return Value : void
90    ***********************************************************************/
```

3.3 Sample Program Listing "resetprg.c" (3/3)

```
91    void PowerON_Reset_PC(void)
92    {
93      /* ==== Floating Point Status/Control Register setting ==== */
94      set_fpscr(FPSCR_Init);
95
96      /* ==== Hardware initialization ==== */
97      HardwareSetup();            /* HardwareSetup function */
98
99      /* ==== Sections initialization ==== */
100     _INITSCT();
101
102     /* ==== Vector Base Register setting ==== */
103     set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
104
105     /* ==== IO library initialization ==== */
106     _INIT_IOLIB();
107
108     /* ==== Status Register setting ==== */
109     set_cr(SR_Init);
110     nop();
111
112     /* ==== Bunk Number Register setting ==== */
113     INTC.IBNR.BIT.BE = 1;           /* Use of register banks enabled for all */
114                                     /*  interrupts except NMI and user break */
115
116     /* ==== Interrupt mask bits clear ==== */
117     set_imask(0);
118
119     /* ==== Main function call ==== */
120     main();
121
122     /* ==== Sleep instruction execution ==== */
123     sleep();
124   }
125
126   /******************************************************************************
127   * Outline      : Manual reset processing
128   * Include      :
129   * Declaration  : void Manual_Reset_PC(void);
130   * Description  : Registers the manual reset vector to the exception vector
131   *              : table.
132   *              : This sample does not describe the processing content at all.
133   *              : Add the program in this function as needed.
134   * Argument     : void
135   * Return Value : void
136   ******************************************************************************/
137   void Manual_Reset_PC(void)
138   {
139     /* NOP */
140   }
141
142   /* END of File */
```

3.4 Sample Program Listing "hwsetup.c" (1/2)

```
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27   ***********************************************************************/
28   /* Copyright (C) 2011 Renesas Electronics Corporation. All rights reserved.   */
29   /***********************************************************************
30   * System Name  : SH7231 Sample Program
31   * File Name    : hwsetup.c
32   * Abstract     : Hardware Function Initial Setting
33   * Version      : 1.00
34   * Device       : SH7231
35   * Tool-Chain   : High-performance Embedded Workshop (Ver.4.08.00).
36   *              : C/C++ compiler package for the SuperH RISC engine family
37   *              :                             (Ver.9.04 Release00).
38   * OS           : None
39   * H/W Platform : R0K572310C000BR (CPU board)
40   * Description  :
41   ***********************************************************************
42   * History      : May 16,2011 Ver.1.00
43   ***********************************************************************/
44
45   /***********************************************************************
46   Includes   <System Includes> , "Project Includes"
47   ***********************************************************************/
48   #include "iodefine.h"
49
```

3.5 Sample Program Listing "hwsetup.c" (2/2)

```
50    /***********************************************************************
51    Imported global variables and functions (from other files)
52    ***********************************************************************/
53    extern void io_set_cpg(void);
54
55    /***********************************************************************
56    Exported global variables and functions (to be accessed by other files)
57    ***********************************************************************/
58    void HardwareSetup(void);
59
60    /***********************************************************************
61    * Outline      : Hardware initialization
62    * Include      :
63    * Declaration  : void HardwareSetup(void);
64    * Description  : Initializes the hardware function.
65    * Argument     : void
66    * Return Value : void
67    ***********************************************************************/
68    void HardwareSetup(void)
69    {
70      /* ==== CPG setting ==== */
71      io_set_cpg();
72    }
73
74    /* End of File */
```

3.6 Sample Program Listing "cpg.c" (1/3)

```
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27    ***********************************************************************/
28    /* Copyright (C) 2011 Renesas Electronics Corporation. All rights reserved.   */
29    /***********************************************************************
30    * System Name  : SH7231 Sample Program
31    * File Name    : cpg.c
32    * Abstract     : CPG Setting Processing
33    * Version      : 1.00
34    * Device       : SH7231
35    * Tool-Chain   : High-performance Embedded Workshop (Ver.4.08.00).
36    *              : C/C++ compiler package for the SuperH RISC engine family
37    *              :                             (Ver.9.04 Release00).
38    * OS           : None
39    * H/W Platform : R0K572310C000BR (CPU board)
40    * Description  :
41    ***********************************************************************
42    * History      : May 16,2011 Ver.1.00
43    ***********************************************************************/
44
45    /***********************************************************************
46    Includes   <System Includes> , "Project Includes"
47    ***********************************************************************/
48    #include "iodefine.h"
49
```

3.7 Sample Program Listing "cpg.c" (2/3)

```
50    /***********************************************************************
51    Exported global variables and functions (to be accessed by other files)
52    ***********************************************************************/
53    void io_set_cpg(void);
54
55    /***********************************************************************
56    * Outline      : CPG setting
57    * Include      :
58    * Declaration  : void io_set_cpg(void);
59    * Description  : Initializes the clock pulse generator (CPG) as follows:
60    *              :   I-clock = 100MHz, B-clock = 50MHz, P-clock = 50MHz,
61    *              :   M-clock = 100MHz, and A-clock = 50MHz.
62    *              : And then supplies clock to all peripheral modules.
63    *              : This function is an example of CPG setting at the input clock
64    *              : of 12.5MHz.
65    * Argument     : void
66    * Return value : void
67    ***********************************************************************/
68    void io_set_cpg(void)
69    {
70      /* ==== CPG setting ==== */
71      /* ---- FRQCR setting ---- */
72      CPG.FRQCR.WORD = 0x0101;/* Clock-in =  12.5MHz:  */
73                              /*  I-clock = 100MHz,    */
74                              /*  B-clock =  50MHz,    */
75                              /*  P-clock =  50MHz     */
76      /* ---- MCLKCR setting ---- */
77      CPG.MCLKCR.BYTE = 0x40;     /*  M-clock = 100MHz     */
78      /* ---- ACLKCR setting ---- */
79      CPG.ACLKCR.BYTE = 0x41;     /*  A-clock =  50MHz     */
80
81
82      /* ==== Module standby clear ==== */
83      /* ---- STBCR2 setting ---- */
84      STB.CR2.BYTE = 0x01; /* H-UDI,UBC,DMAC,FPU,                          */
85                           /* Reserve(0),Reserve(0),DTC,Reserve(1)         */
86      /* ---- STBCR3 setting ---- */
87      STB.CR3.BYTE = 0x00; /* HIZ,MTU2S,MTU2,Reserve(0),                   */
88                           /* IIC3,FastRAM,KeepRAM,ROM/FLD                 */
89      /* ---- STBCR4 setting ---- */
90      STB.CR4.BYTE = 0x01; /* SCIF4,SCIF5,SCIF6,SCIF7,                     */
91                           /* Reserve(0),CMT,CMT2,Reserve(1)               */
92      /* ---- STBCR5 setting ---- */
93      STB.CR5.BYTE = 0x00; /* SCI0,SCI1,SCI2,SCI3,                         */
94                           /* RSPI,ADC0,ADC1,RCAN-ET                       */
95      /* ---- STBCR6 setting ---- */
96      STB.CR6.BYTE = 0x60; /* LVDS,Reserve(1),Reserve(1),Reserve(0),       */
97                           /* Reserve(0),Reserve(0),Reserve(0),Reserve(0) */
```

3.8 Sample Program Listing "cpg.c" (3/3)

```
98        /* ---- STBCR7 setting ---- */
99        STB.CR7.BYTE = 0x00; /* TIM32C,KEYC,Xtal_to_EXTAL32/XTAL32(B'00),   */
100                            /* Reserve(0),Reserve(0),Reserve(0),Reserve(0) */
101     }
102
103     /* End of File */
```

3.9 Sample Program Listing "vecttbl.c" (1/2)

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28   /* Copyright (C) 2011 Renesas Electronics Corporation. All rights reserved.   */
29   /***********************************************************************
30   * System Name  : SH7231 Sample Program
31   * File Name    : vecttbl.c
32   * Abstract     : Initialization for Vector Table
33   * Version      : 1.00
34   * Device       : SH7231
35   * Tool-Chain   : High-performance Embedded Workshop (Ver.4.08.00).
36   *              : C/C++ compiler package for the SuperH RISC engine family
37   *              :                              (Ver.9.04 Release00).
38   * OS           : None
39   * H/W Platform : R0K572310C000BR (CPU board)
40   * Description  :
41   ***********************************************************************
42   * History      : May 16,2011 Ver.1.00
43   ***********************************************************************/
44
45   /***********************************************************************
46   Includes   <System Includes> , "Project Includes"
47   ***********************************************************************/
48   #include "vect.h"
49
```

3.10 Sample Program Listing "vecttbl.c" (2/2)

```
50      /***********************************************************************
51      Exported global variables and functions (to be accessed by other files)
52      ***********************************************************************/
53      #pragma section VECTTBL
54      void *RESET_Vectors[] = {
55      // <<VECTOR DATA START (POWER ON RESET)>>
56      // 0 Power On Reset PC
57          (void *)PowerON_Reset_PC,
58      // <<VECTOR DATA END (POWER ON RESET)>>
59      // 1 Power On Reset SP
60          __secend("S"),
61      // <<VECTOR DATA START (MANUAL RESET)>>
62      // 2 Manual Reset PC
63          (void *)Manual_Reset_PC,
64      // <<VECTOR DATA END (MANUAL RESET)>>
65      // 3 Manual Reset SP
66          __secend("S")
67      };
68
69      #pragma section INTTBL
70      void *INT_Vectors[] = {
71      // 4 Illegal code
72          (void *)INT_Illegal_code,

…       …

573     // 255 SCI SCI3 TEI3
574         (void *)INT_SCI_SCI3_TEI3,
575     // xx Reserved
576         (void *)Dummy
577     };
578
579     /* End of File */
```

4. References

- Software Manual
  SH-2A, SH2A-FPU Software Manual Rev. 3.00
  The latest version can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7231 Group User's Manual: Hardware Rev. 1.00
  The latest version can be downloaded from the Renesas Electronics website.

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Revision Record

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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