SH7216/SH7239/SH7231 Groups

Data Transfer Within On-Chip RAM (Cycle Stealing Mode) Using the DMAC

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Abstract

This application note describes a sample program for the SH7216, SH7239, and SH7231 Group MCUs that transfers data using the direct memory access controller (DMAC).

The operation of this program has the following features.

- Use of DMAC channel 0
- Use of auto-request mode for DMA transfers
- Use of cycle stealing mode as the bus mode
- The transfer source and destination are both in RAM.

Products

SH7216, SH7239, and SH7231 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This application note uses the direct memory access controller (DMAC) to transfer data within internal RAM.

The sample program sets the DMAC to cycle stealing mode and uses auto-request as the DMA transfer start factor. The sample program performs 128 transfers of 32 bits of data (for a total of 512 bytes).

Table 1.1 lists the peripheral functions used and their uses and figure 1.1 shows the block diagram of the peripheral functions used.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Direct memory access controller (DMAC)	DMA data transfers
Internal RAM	Transfer source and destination

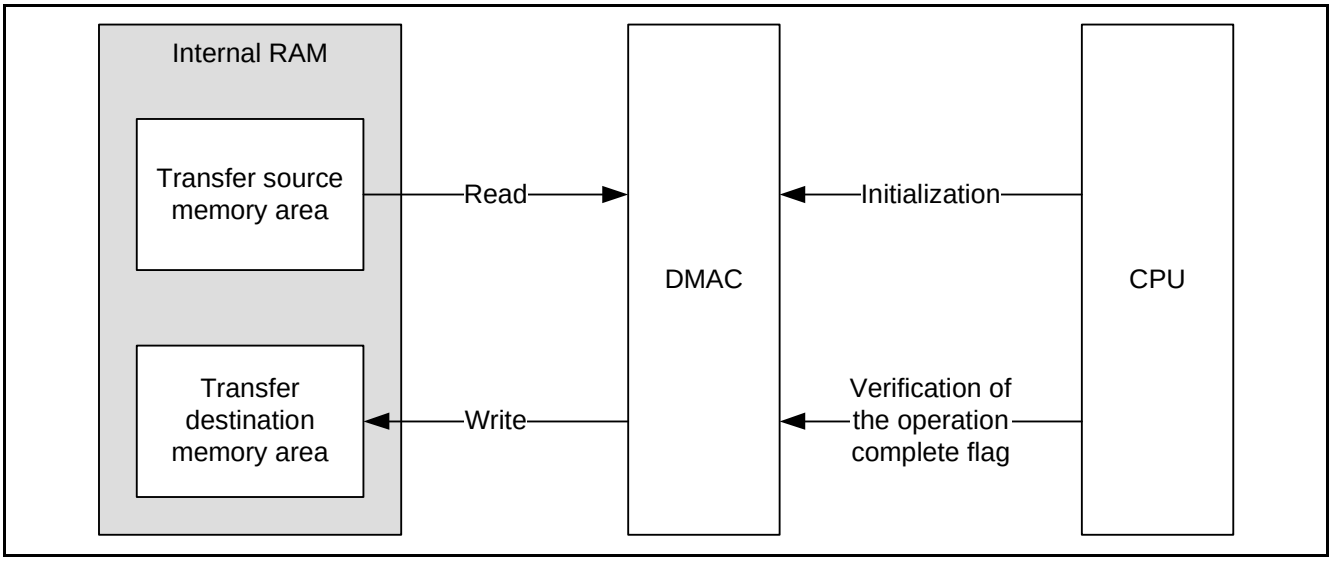

Figure 1.1 Used Peripheral Function Block Diagram

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed to run normally following conditions.

Table 2.1 Operating Conditions (SH7216)

Item	Contents
MCU used	SH7216
Operating frequency	Main clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Operating voltage	Vcc: 3.3 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics Renesas SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
	Compiler options: -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo
Operating mode	User program mode
Version of the sample code	1.00
Board used	R0K572167C001BR

Table 2.2 Operating Conditions (SH7239)

Item	Contents
MCU used	SH7239A
Operating frequency	Main clock: 160 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
Operating voltage	Vcc: 3.3 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics Renesas SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 02
	Compiler options: -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo
Operating mode	Single-chip mode
Version of the sample code	1.00
Board used	R0K572390C000BR

Table 2.3 Operating Conditions (SH7231)

Item	Contents
MCU used	SH7231
Operating frequency	Main clock: 100 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Operating voltage	Vcc: 3.3 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.08.00
C compiler	Renesas Electronics Renesas SuperH RISC engine Family C/C++ Compiler Package Ver.9.04 Release 00
	Compiler options: -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo
Operating mode	Single-chip mode
Version of the sample code	1.00
Board used	R0K572310C000BR

3. Reference Application Notes

The following application notes are related to this document and should be referred to when using this application note.

- SH7216 Group Example of Initialization (RJJ06B1073)
- SH7239 Group Example of Initialization (R01AN0297EJ)
- SH7231 Group Example of Initialization (R01AN0322EJ)

4. Peripheral Functions

This section describes the direct memory access controller (DMAC). The basic description of this peripheral module is included in the SH7216 Group User's Manual: Hardware, SH7239 Group User's Manual: Hardware, and SH7231 Group User's Manual: Hardware documents.

When there are DMA transfer requests, the DMAC starts the transfer according to a predetermined channel priority and when the transfer complete conditions are met, it terminates the transfer. There are three transfer request modes: auto-request, external request, and internal peripheral module request. The bus mode can be selected to be either burst mode or cycle stealing mode.

Table 4.1 provides an overview of the DMAC. Figure 4.1 shows an example of a cycle stealing normal mode DMA transfer, and figure 4.2 shows an example of a burst mode DMA transfer.

Table 4.1 DMAC Overview

Item	Description
Number of channels	• SH7216 and SH7239: 8 channels, CH0 to CH7 (Only the four channels CH0 to CH3 can accept external requests.) • SH7231: 4 channels, CH0 to CH3 (Only the two channels CH0 and CH1 can accept external requests.)
Address space	4 GB (Logical address space)
Transfer data lengths	Byte, word (2 bytes), long word (4 bytes), and 16 bytes (long word × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address modes	Single address mode and dual address mode
Transfer requests	External requests, internal peripheral module requests*, auto-requests
Bus modes	Cycle stealing mode (normal mode and intermittent mode), burst mode
Priority	Channel priority fixed mode, round robin mode
Interrupt requests	CPU interrupt requests can be generated at data transfer 1/2 complete and at data transfer complete.
External request detection	Low or high level detection and rising or falling edge detection for the DREQ input
Transfer request accept signal and transfer complete signal	The active levels for the DACK and TEND signals can be set.

Note: * The factors supported depend on the MCU.

In cycle stealing normal mode, the DMAC releases bus rights to another bus master each time the transfer of a single transfer unit (byte, word, longword, or 16-byte unit) completes. If there is a transfer request after that, the DMAC reacquires bus rights from the other master, once again performs a single transfer unit transfer, and when that transfer completes releases bus rights to another bus master. This operation is repeated until the transfer complete conditions are met.
Cycle stealing normal mode can be used in all transfer periods, regardless of the transfer request source, transfer source, or transfer destination.

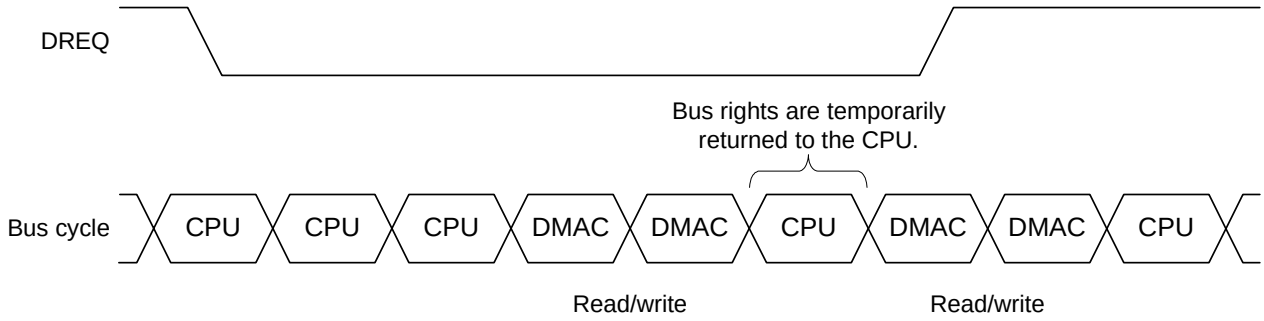

Figure 4.1 Cycle Stealing Normal Mode DMA Transfer Example (dual address, DREQ low-level detection)

In burst mode, once the DMAC has acquired bus rights, it continues the transfer operations without releasing those rights until the transfer complete conditions are met. However, in external request mode when level detection is used for DREQ, if the DREQ signal transitions away from the active level, after the DMAC transfer request that was already accepted completes, bus rights will be passed to another bus master, even if the transfer complete conditions are not met.

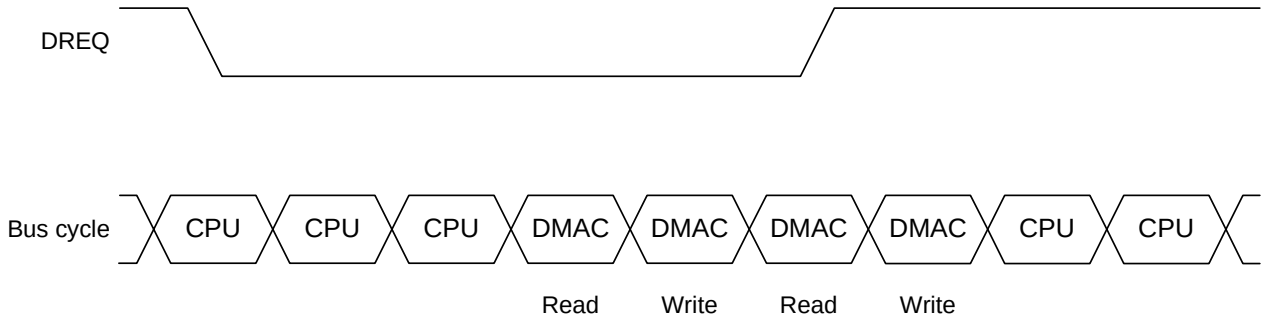

Figure 4.2 Bus Mode DMA Transfer Example (dual address, DREQ low-level detection)

5. Software

5.1 Operation Overview

The sample program writes a pattern to the transfer source memory area in advance and after setting up the DMAC, it starts an auto-request transfer to the transfer destination memory area by enabling DMAC operation in software.

Table 5.1 lists the DMAC settings. Figure 5.1 presents an overview of this operation.

Table 5.1 DMAC Settings

Item	Description
Channel used	CH0
Transfer data length	Long word (4 bytes)
Transfer count	128 transfers (128 transfers × 4 byte data length = 512 bytes of data)
Address mode	Dual address mode
Transfer request	Auto-request
Bus mode	Cycle stealing mode (normal mode)
Priority	Channel priority fixed mode
Interrupt	Interrupts disabled.

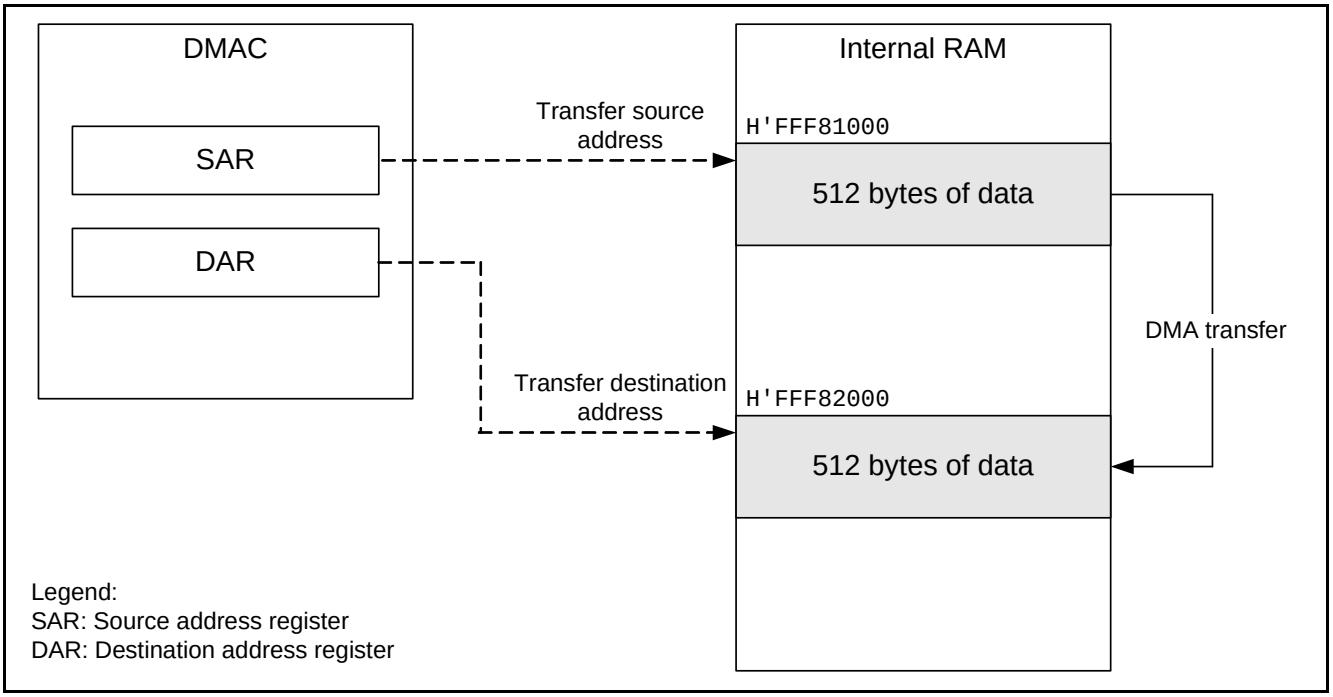

Figure 5.1 Operation Overview

5.2 File Composition

Table 5.2 lists the file used in the sample code. Files not generated by the integrated development environment should not be listed in this table.

Table 5.2 File Used in the Sample Code

File Name	Outline	Remarks
main.c	Main module	Initialization and DMA transfer processing

5.3 Constants

Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
IRAM_SRC_ADDR	H'FFF8 1000	Transfer source start address (internal RAM)
IRAM_DST_ADDR	H'FFF8 2000	Transfer destination start address (internal RAM)
DMA_COUNT	128	DMA transfer count
DMA_SIZE	4	DMA transfer size

5.4 Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Outline
main	Main processing
memory_init	Transfer source/transfer destination memory area initialization
io_dma_init	DMAC initialization
io_dma_start	DMA transfer start processing
io_dma_poll_end	DMA transfer end processing

5.5 Function Specifications

The following tables list the sample code function specifications.

main		
Outline	Main processing	
Header		
Declaration	void main(void)	
Description	This function first initializes the transfer source and transfer destination memory areas. Then it initializes the DMAC, starts a DMA transfer, and waits for that transfer to complete. Finally, it enters an infinite loop.	
Arguments	None	
Return Value	None	

memory_init		
Outline	Transfer source/transfer destination memory area initialization	
Header		
Declaration	void memory_init(uint32_t src_addr, uint32_t dst_addr, uint32_t size)	
Description	This function writes pattern data to the transfer source memory area. It clears the transfer destination memory area to all zeros.	
Arguments	uint32_t src_addr:	Transfer source memory area size
	uint32_t dst_addr:	Transfer destination memory area address
	uint32_t size:	Transfer source/transfer destination memory area sizes in bytes
Return Value	None	

io_dma_init		
Outline	DMAC initialization	
Header		
Declaration	void io_dma_init(uint32_t src_addr, uint32_t dst_addr, uint32_t dma_count)	
Description	After clearing the DMAC module standby state, this function sets the DMAC registers.	
Arguments	uint32_t src_addr:	Transfer source memory area size
	uint32_t dst_addr:	Transfer destination memory area address
	uint32_t dma_count:	DMA transfer count (number of longwords to transfer)
Return Value	None	

io_dma_start	
Outline	DMA transfer start processing
Header	
Declaration	void io_dma_start(void)
Description	Starts a DMA transfer.
Arguments	None
Return Value	None

io_dma_poll_end	
Outline	DMA transfer end processing
Header	
Declaration	void io_dma_poll_end(void)
Description	After waiting for the completion of the DMA transfer, terminates DMA transfer operation.
Arguments	None
Return Value	None

5.6 Flowcharts

5.6.1 Main Processing

Figure 5.2 shows the main processing.

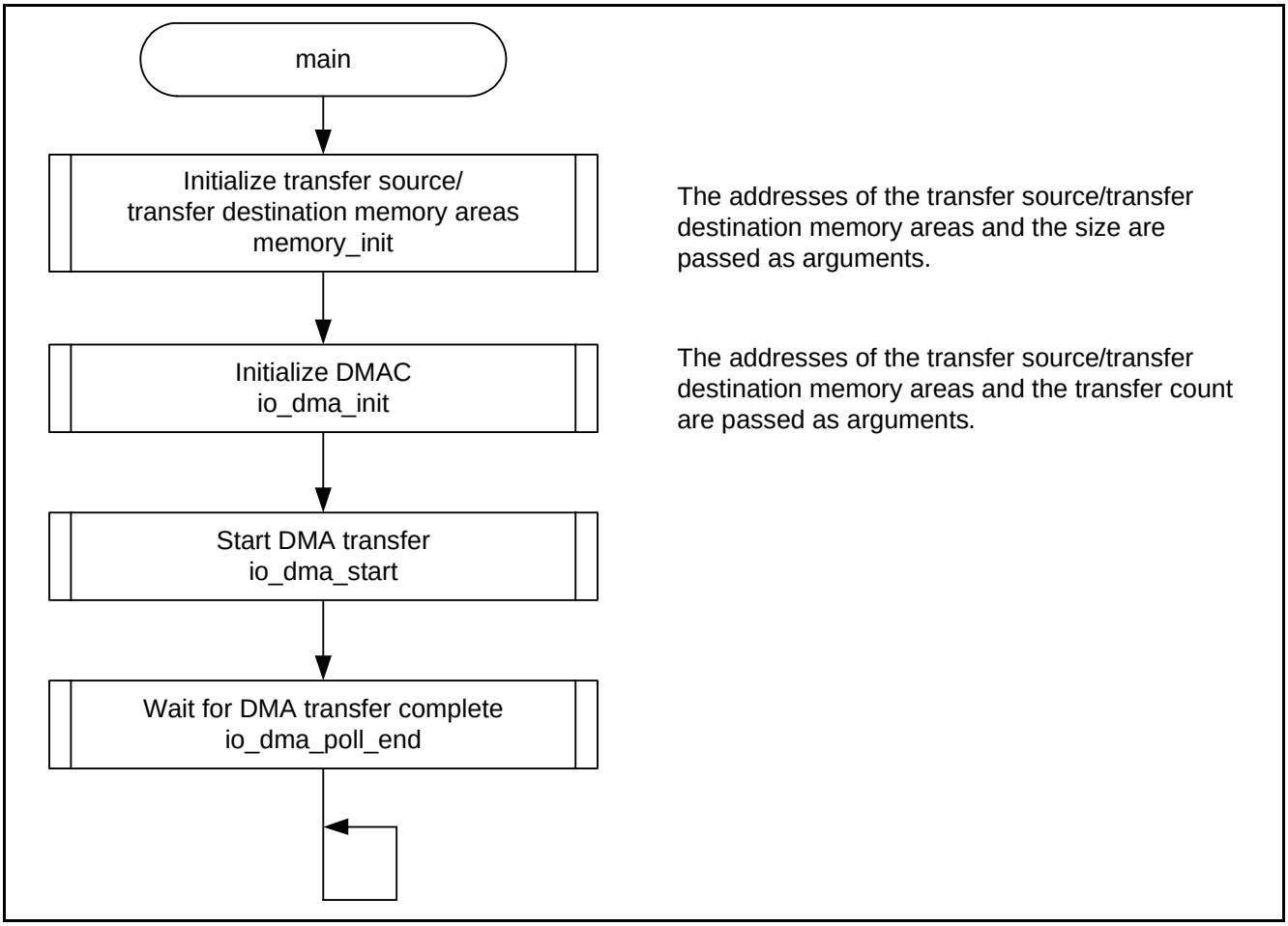

Figure 5.2 Main Processing

5.6.2 Transfer Source/Transfer Destination Memory Area Initialization

Figure 5.3 shows the flowchart for transfer source/transfer destination memory area initialization.

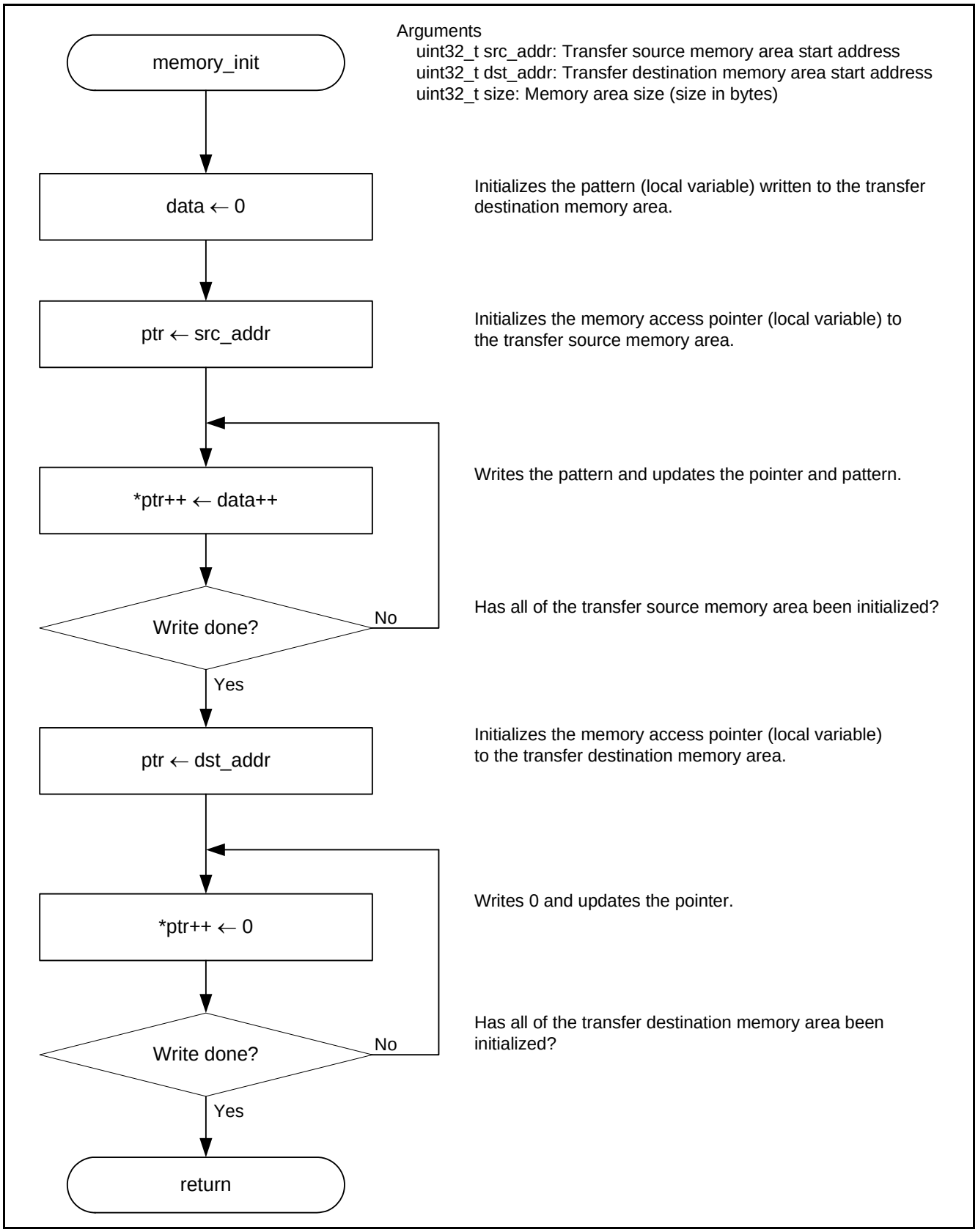

Figure 5.3 Transfer Source/Transfer Destination Memory Area Initialization

5.6.3 DMAC Initialization

Figure 5.4 shows the flowchart for DMAC initialization.

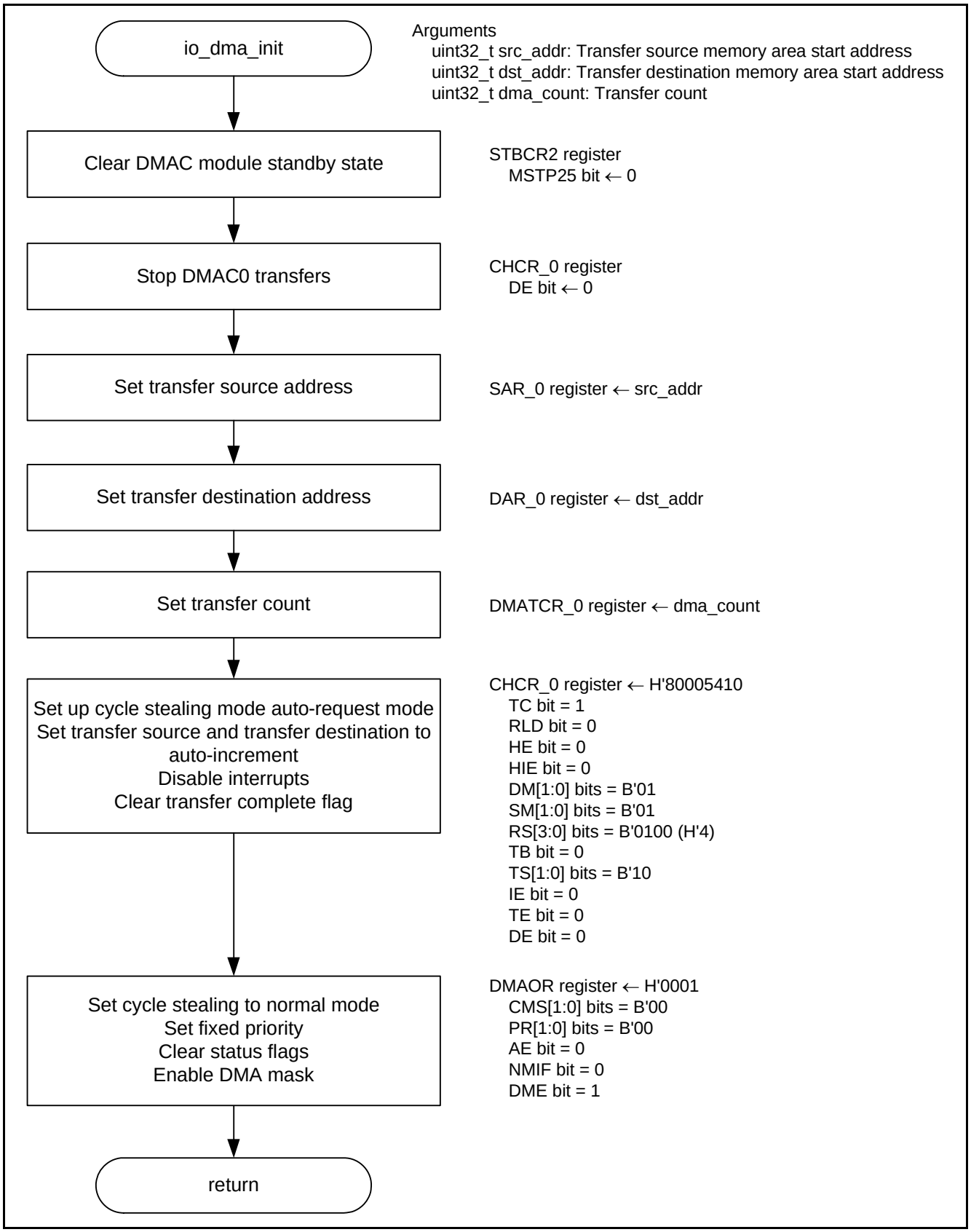

Figure 5.4 DMAC Initialization

5.6.4 DMA Transfer Start Processing

Figure 5.5 shows the flowchart for DMA transfer start processing.

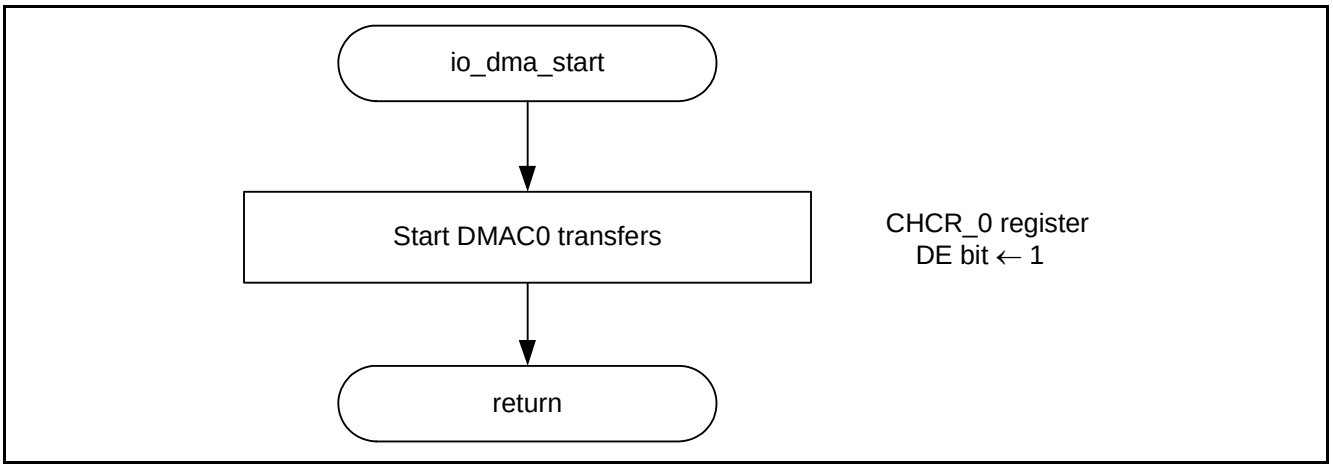

Figure 5.5 DMA Transfer Start Processing

5.6.5 DMA Transfer End Processing

Figure 5.6 shows the flowchart for DMA transfer end processing.

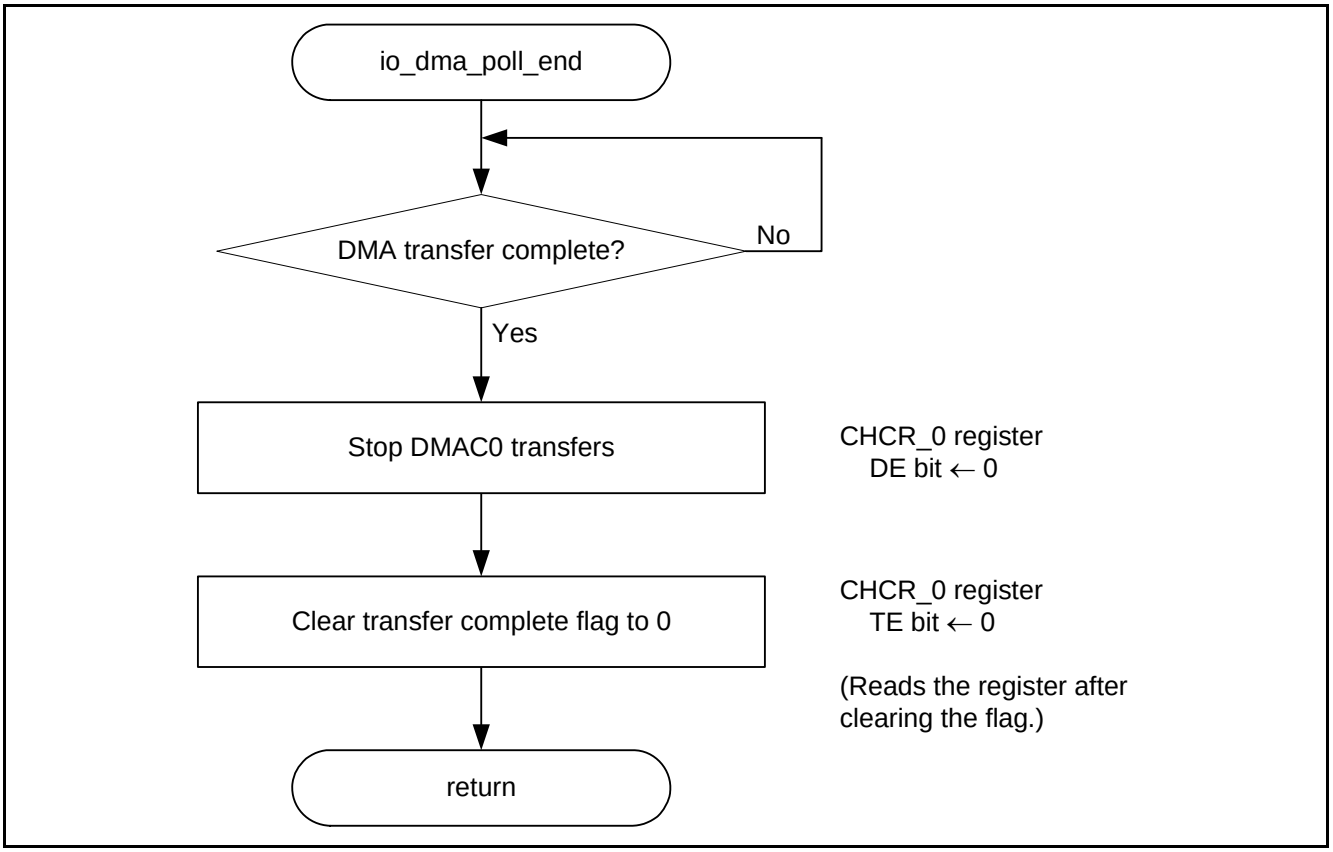

Figure 5.6 DMA Transfer End Processing

6. Reference Documents

- Hardware Manual:
  SH7216 Group Users Manual: Hardware Rev.3.00 (R01UH0230EJ)
  SH7239 Group Users Manual: Hardware Rev.1.00 (R01UH0086EJ)
  SH7231 Group Users Manual: Hardware Rev.2.00 (R01UH0073EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)
- Software Manual
  SH-2A, SH2A-FPU User's Manual: Software Rev.4.00 (R01US0031EJ)
  (The latest version can be downloaded from the Renesas Electronics website.)

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REVISION HISTORY	SH7216/SH7239/SH7231 Groups Application Note Data Transfer Within On-Chip RAM (Cycle Stealing Mode) Using the DMAC

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 07, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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