SH7216 Group

SCIF (Asynchronous) Data Transfer Using DMAC

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Introduction

This application note presents an overview of using the direct memory access controller (DMAC) and serial communication interface with FIFO (SCIF) of the SH7216 to perform asynchronous data transfer.

Note that although the sample tasks and applications presented in this application note have been verified to work as intended, they should be checked in the actual operating environment before being put into actual use.

Target Device

SH7216

Contents

1. Introduction

1.1 Specifications

- DMAC channels 0 and 1, and SCIF channel 3, are used.
- The activation source for DMAC channel 0 is the SCIF transmit FIFO data empty interrupt (TXI).
- The activation source for DMAC channel 1 is the SCIF receive FIFO data full interrupt (RXI).
- SCIF channel 3 is set to asynchronous mode, 8-bit data length, 1 stop bit, and no parity.
- The transmit data is a 32-byte character string that is allocated beforehand to the on-chip flash memory.
- The receive data is stored in the on-chip RAM.

1.2 Functions Used

- Serial communication interface with FIFO (SCIF), channel 3
- Direct memory access controller (DMAC), channels 0 and 1

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.06.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03.00, Release 00
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu –pic=1 –object="$(CONFIGDIR)¥$(FILELEAF).obj" -debug -gbr=auto –chgincpath –errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo))

2. Description of Sample Application

The sample application performs SCIF asynchronous data transmission and reception, using the SCIF as the DMAC activation source.

2.1 Operation of Functions Used

2.1.1 Serial Communication Interface with FIFO (SCIF)

The SCIF supports two data transfer modes: asynchronous and clock synchronous. It incorporates 16-stage first-in first-out (FIFO) registers for transmission and reception, enabling efficient and high-speed continuous communication.

For details of the SCIF, see the Serial Communication Interface with FIFO

(SCIF) section in the *SH7216 Group Hardware Manual*.

Table 1 shows an outline of the SCIF, table 2 asynchronous communication, and table 3 clock synchronous communication.

Figure 1 is a block diagram of the SCIF.

Table 1 SCIF Outline

Item	Description
Communication modes	Asynchronous serial communication, clock synchronous serial communication Support for full-duplex communication
Clock source	Baud rate generator (internal clock) or SCK pin (external clock)
Interrupts	Transmit FIFO data empty interrupt, break interrupt, receive FIFO data full interrupt, receive error interrupt
Other	Low-power mode setting Receive error count detection Timeout error detection (for reception in asynchronous mode)

Table 2 Outline of Asynchronous Communication

Item	Description
Data length	7 or 8 bits
Stop bit length	1 or 2 bits
Parity	Even, odd, or no parity
Receive error detection	Parity error, framing error, overrun error
Break detection	A break is detected when a framing error is followed by a space 0 level (low level) lasting for one frame length or more. A break can also be detected by reading the RXD pin level directly from the serial port register when a framing error occurs.

Table 3 Outline of Clock Synchronous Communication

Item	Description
Data length	8 bits
Receive error detection	Overrun error

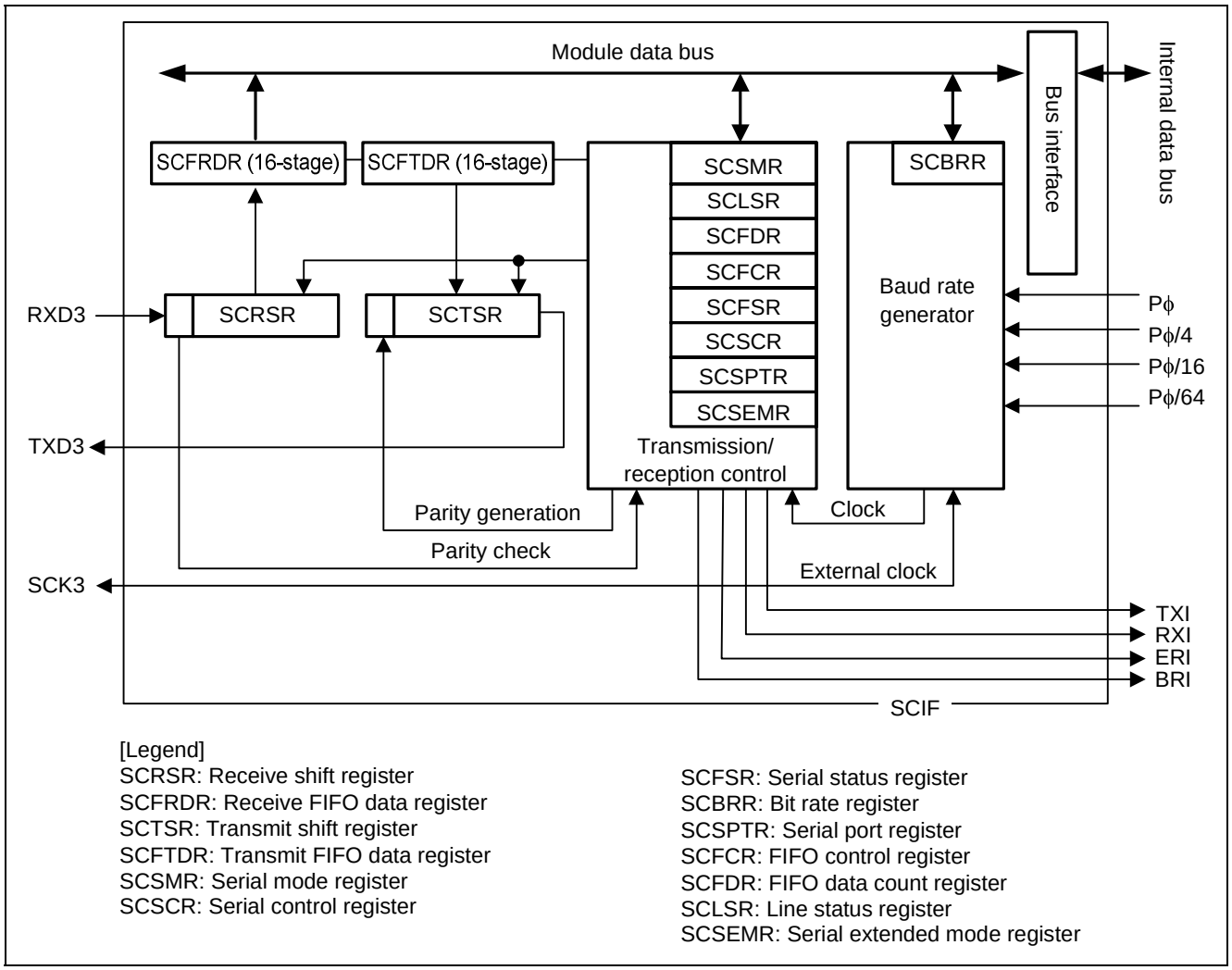


Figure 1 Block Diagram of SCIF

2.1.2 Direct Memory Access Controller (DMAC)

The DMAC of the SH7216 takes the place of the CPU to perform high-speed data transfers between external devices with DACK (transfer request acknowledge signal), external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral module.

The bus mode is selectable between cycle steal mode and burst mode.

For details of the DMAC, see the Direct Memory Access Controller (DMAC) section in the *SH7216 Group Hardware Manual*.

Table 4 shows an overview of the DMAC. Figure 2 shows an example of DMA transfer using cycle steal mode, and figure 3 shows an example of DMA transfer using burst mode. Figure 4 is a block diagram of the DMAC.

Table 4 DMAC Overview

Item	Description
Number of channels	8 channels: CH0 to CH7 External requests can be accepted on only four channels, CH0 to CH3.
Address space	4 GB
Transfer data length	Byte, word (2 bytes), longword (4 bytes), 16 bytes (longword × 4)
Max. transfer count	16,777,216 (24-bit) transfers
Addressing modes	Single address mode, dual address mode
Transfer requests	External request, on-chip peripheral module request, auto request (SCIF: 8 sources, I2C3: 2 sources, A/D converter: 1 source, MTU2: 5 sources, CMT: 2 sources)
Bus modes	Cycle steal mode (normal mode, intermittent mode), burst mode
Priority	Channel priority fixed mode, round-robin mode
Interrupt requests	Generation of interrupt request to CPU when data transfer half finished or at end of data transfer
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/ transfer end signal	Ability to set active level of DACK and TEND

In normal mode cycle steal operation, the DMAC releases bus mastership to another bus master each time transfer of a transfer unit (byte, word, longword, or 16-byte unit) completes. When the next transfer request occurs, the DMAC takes back bus mastership from another bus master, transfers another transfer unit, and again releases bus mastership to another master when the transfer completes. This process is repeated until the transfer end condition is satisfied. Normal mode cycle steal operation can be used for any transfer category, regardless of the transfer request source, transfer source, or transfer destination.

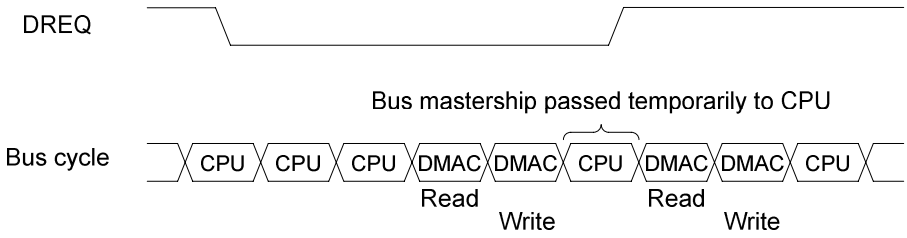


Figure 2 Example of DMA Transfer Using Cycle Steal Mode (Dual Address, DREQ Low Level Detection)

In burst mode, once the DMAC obtains bus mastership it performs data transfer continuously, not releasing bus mastership until the transfer end condition is satisfied. However, in external request mode when DREQ level detection is enabled and DREQ is not at the active level, the DMAC releases bus mastership to another bus master after all DMAC transfers for which requests have been received have completed, even if the transfer end condition has not been satisfied.

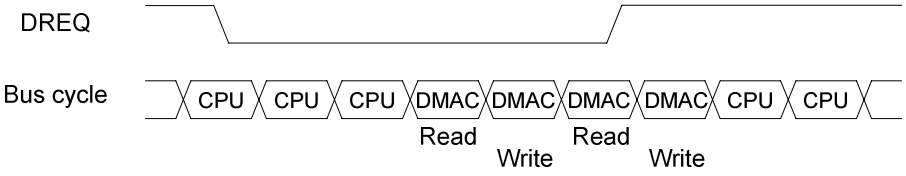
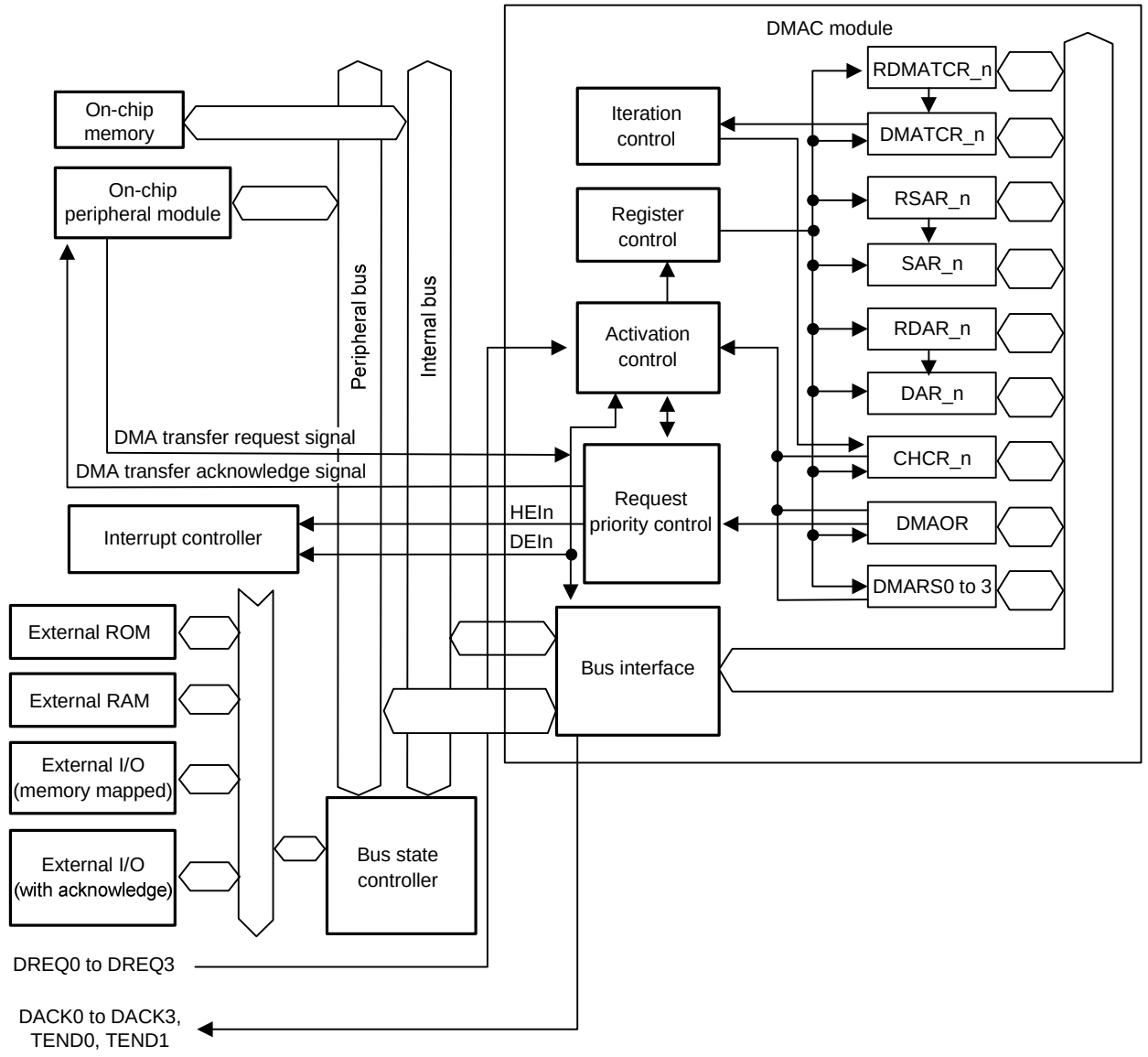


Figure 3 Example of DMA Transfer Using Burst Mode (Dual Address, DREQ Low Level Detection)



RDMATCR: DMA reload transfer count register
DMATCR: DMA transfer count register
RSAR: DMA reload source address register
SAR: DMA source address register
RDAR: DMA reload destination address register
DAR: DMA destination address register
CHCR: DMA channel control register
DMAOR: DMA operation register
DMARS0 to DMARS3: DMA extension resource selectors 0 to 3
HEIn: DMA transfer half-complete interrupt request to CPU
DEIn: DMA transfer end interrupt request to CPU
n: 0, 1, 2, 3, 4, 5, 6, 7

Figure 4 Block Diagram of DMAC

2.2 Sample Program Operation

Table 5 lists the settings for the sample program. Figure 5 illustrates the operation of the program.

Table 5 Sample Program Settings

Function	Item	Setting	
SCIF	Operating mode	Asynchronous	
	Data length	8 bits	
	Parity	None	
	Stop bits	1 stop bit	
	Clock source	Pϕ clock (50 MHz)	
	Interrupts	Transmit FIFO data empty interrupt (TXI), receive FIFO data full interrupt (RXI)	
	Baud rate	19,200 bps	
DMAC	Channel	CH0	CH1
	Transfer activation source	On-chip peripheral module request mode (TXI3 in SCIF_3)	On-chip peripheral module request mode (RXI3 in SCIF_3)
	Transfer data length	One byte	One byte
	Transfer count	32	32
	Transfer source address	H'00010000 (on-chip flash memory)	H'00010000 (on-chip flash memory)
	Transfer destination address	H'FFF88000 (on-chip RAM)	
	Addressing mode	Dual address mode	Dual address mode
	Bus mode	Cycle steal mode	Cycle steal mode
	Priority	Channel priority fixed mode	Channel priority fixed mode
	Interrupt request	DMAC stops when data transfer ends	DMAC stops when data transfer ends

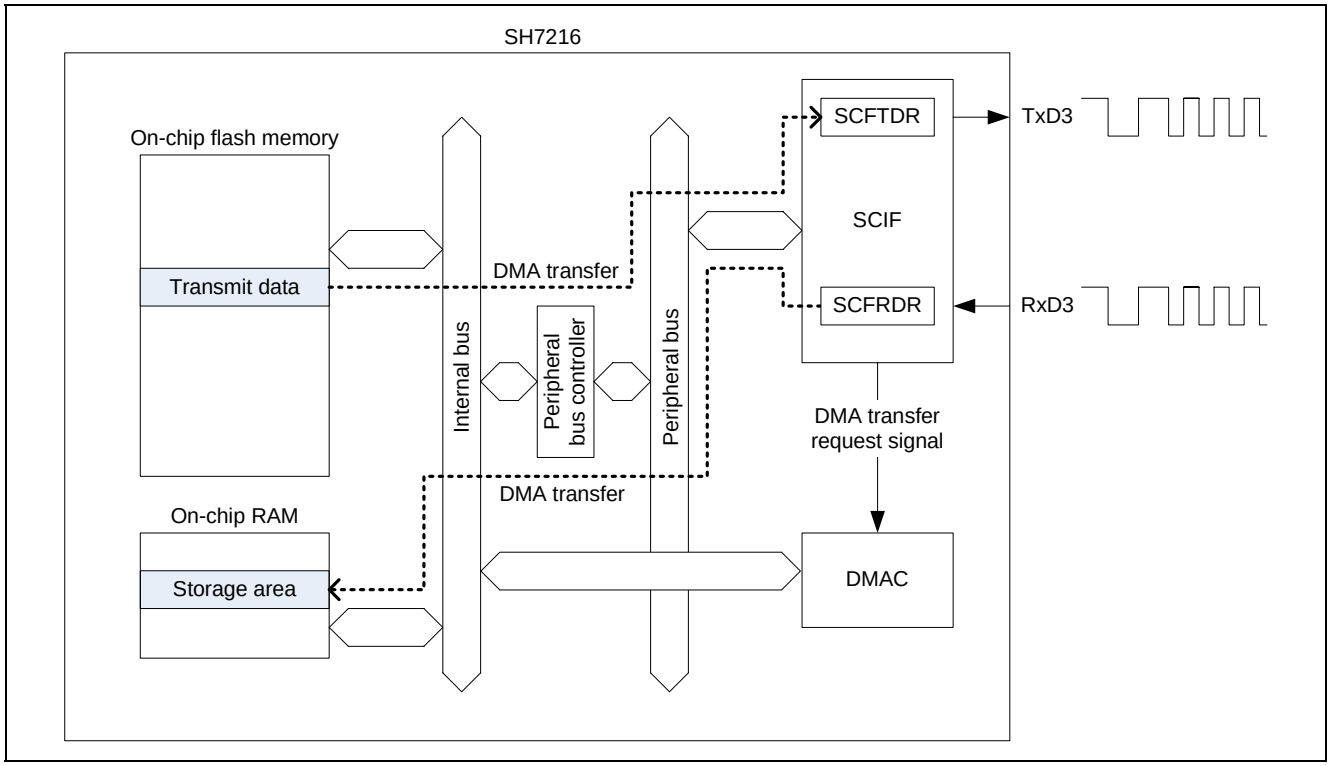


Figure 5 Illustration of Program Operation

2.3 Setting Procedure for Functions Used

The procedure for making initial settings for the functions used by the sample program is described below.

Figure 6 shows the processing sequence of the sample program, figure 7 shows the setting sequence for canceling module standby, figure 8 shows the setting sequence for the pin configuration controller, figure 9 shows the initialization sequence for DMAC and figure 11 shows the SCIF initialization sequence.

Figure 12 shows the processing sequence of the SCIF transmit interrupt handler, figure 13 shows the processing sequence of the SCIF receive interrupt handler, and figure 14 shows the processing sequence of the receive error interrupt handler.

For details on the settings of each register, see the *SH7216 Group Hardware Manual*.

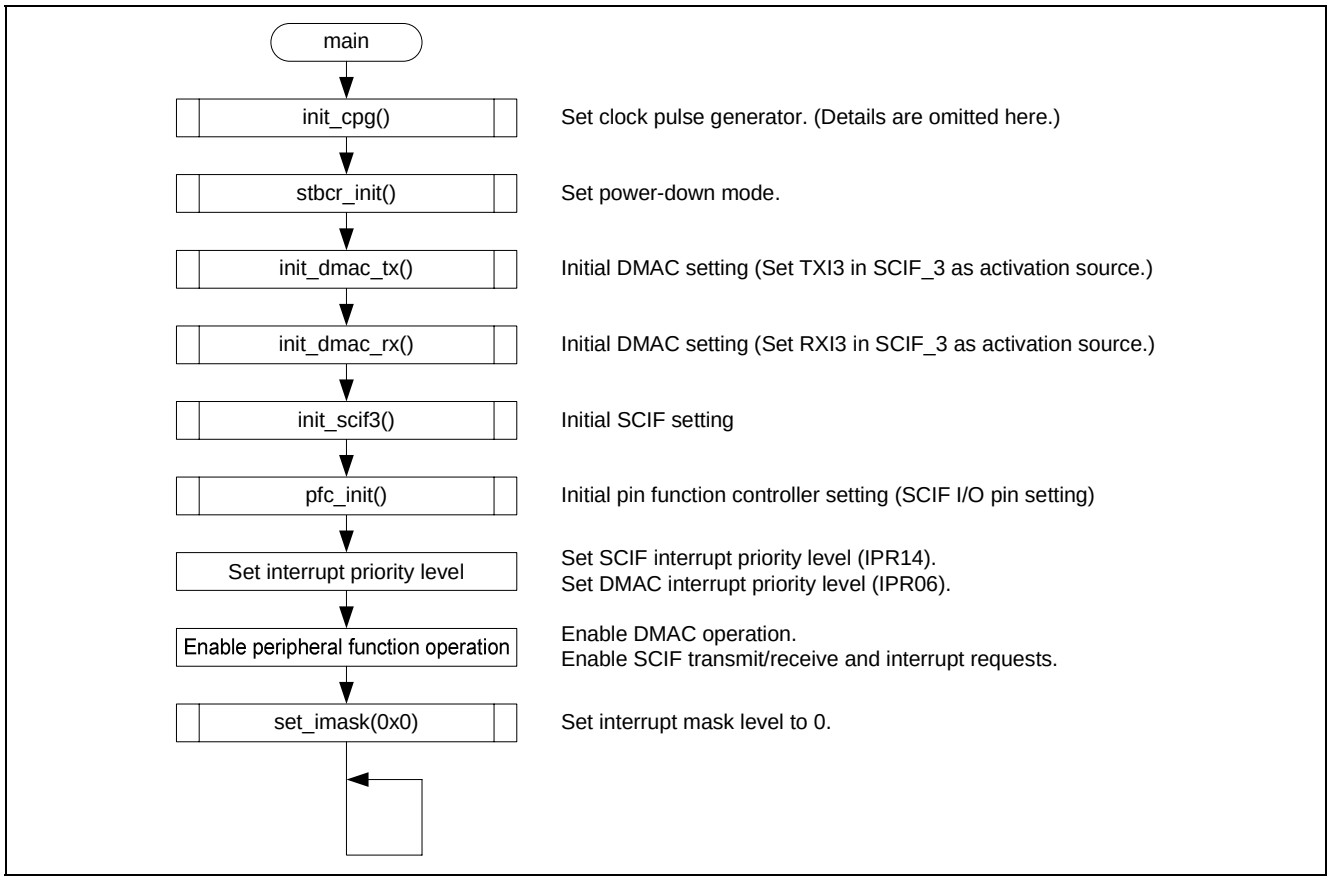


Figure 6 Sample Program Processing Sequence

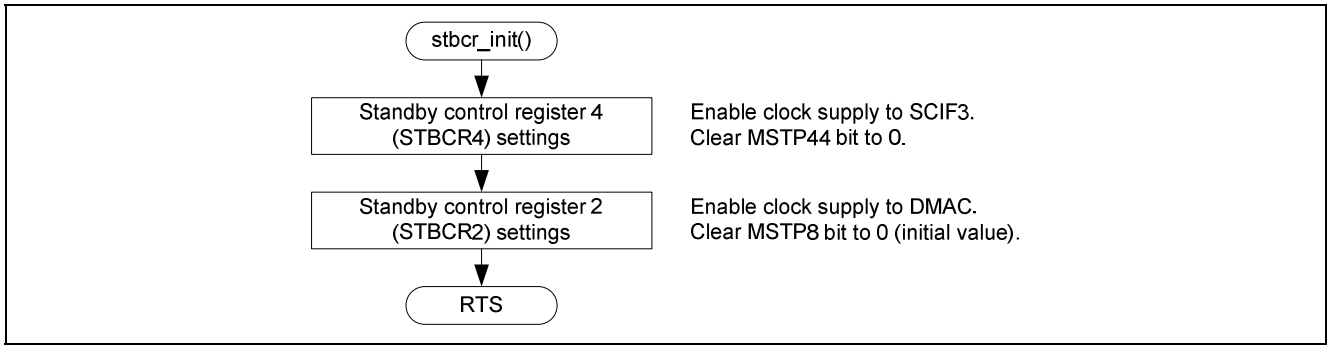


Figure 7 Setting Sequence for Canceling Module Standby

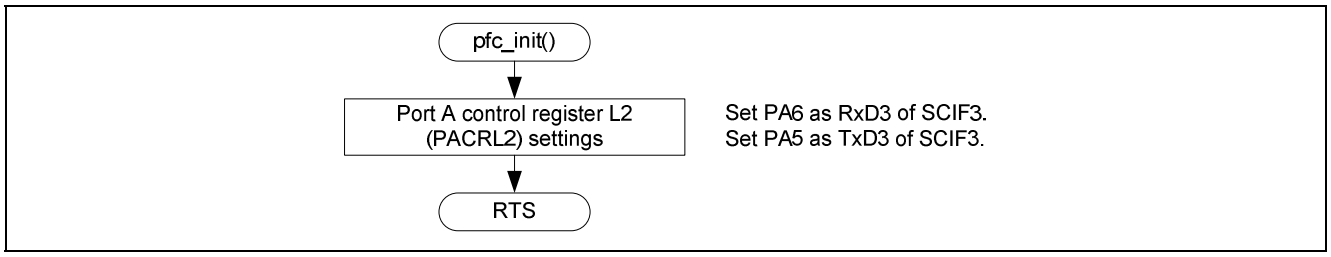


Figure 8 Pin Configuration Controller Setting Sequence

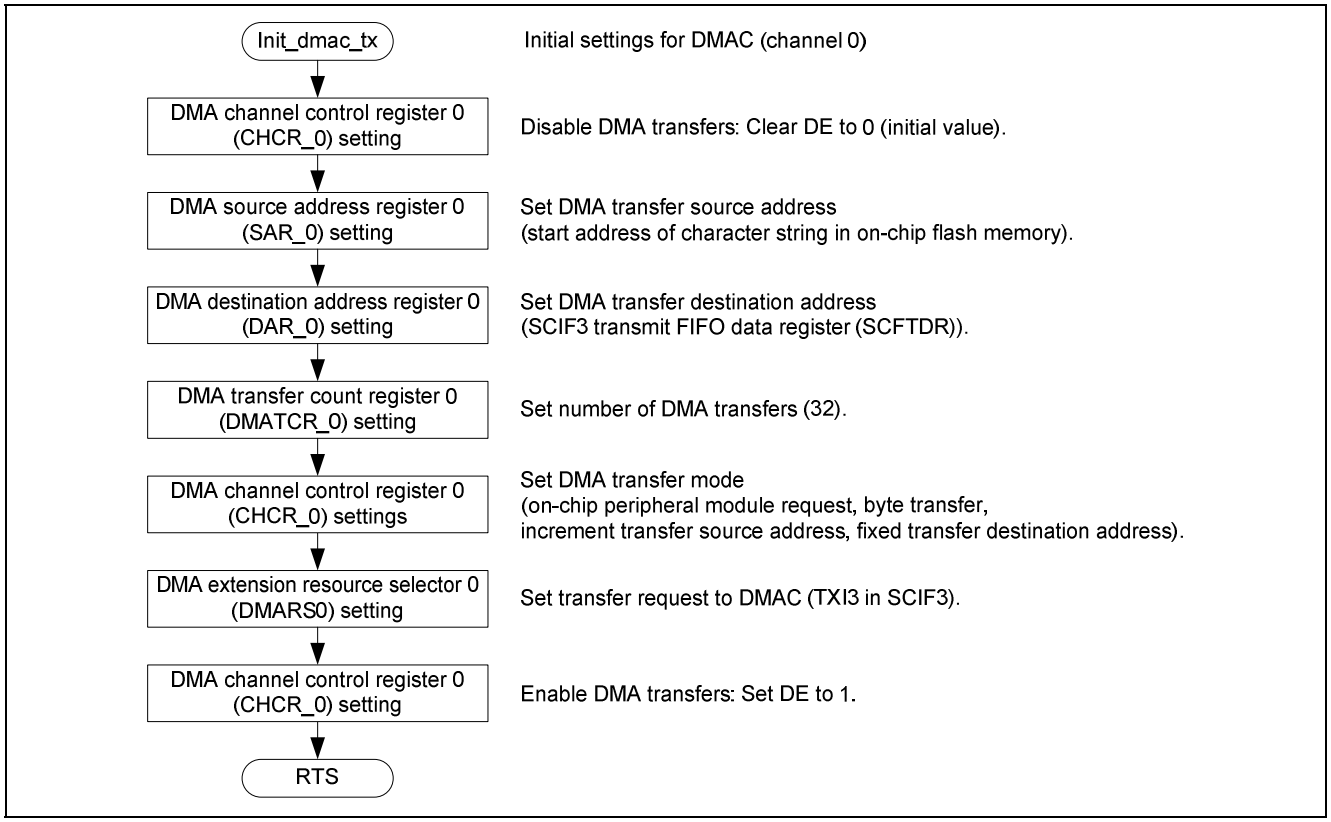


Figure 9 DMAC Channel 0 Initialization Sequence

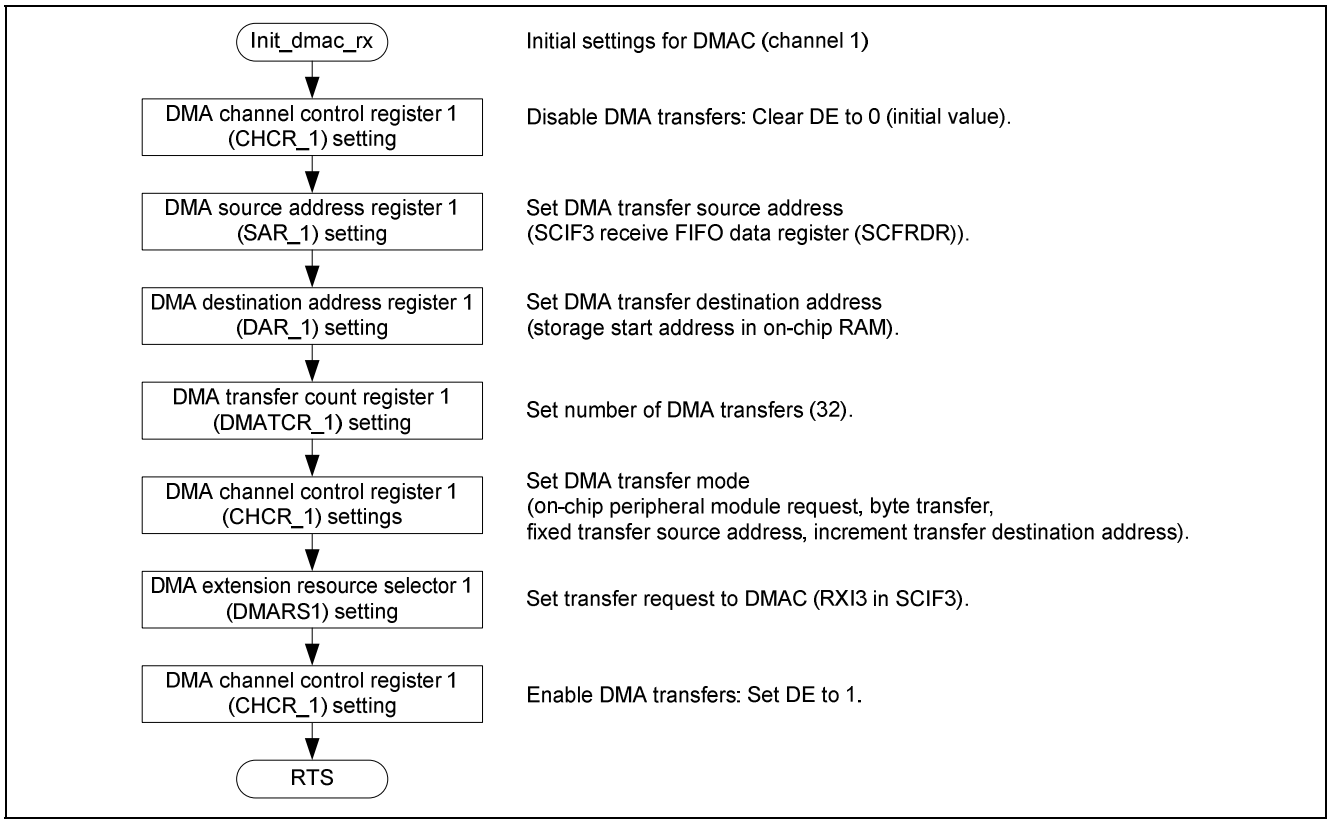


Figure 10 DMAC Channel 1 Initialization Sequence

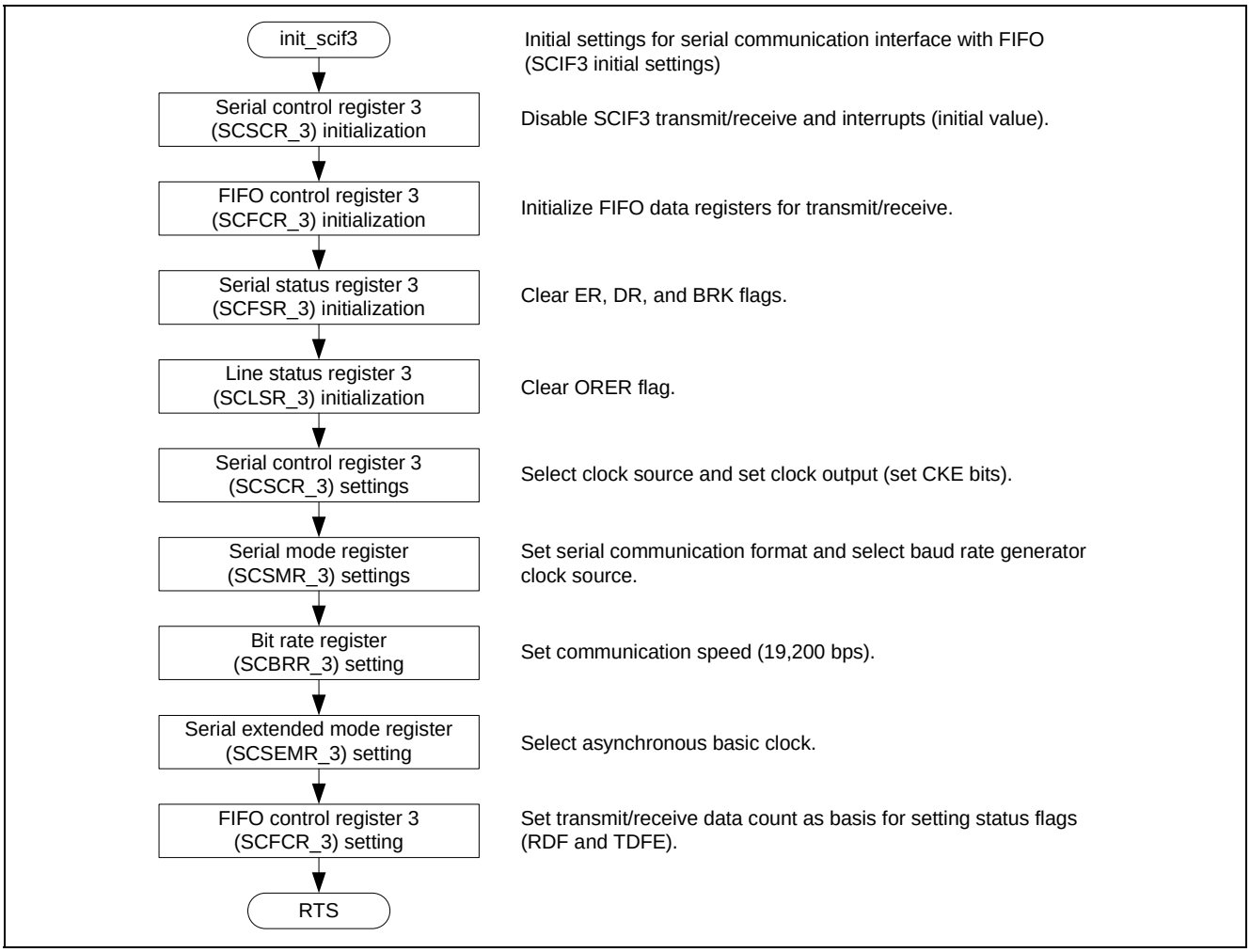


Figure 11 SCIF Initialization Sequence

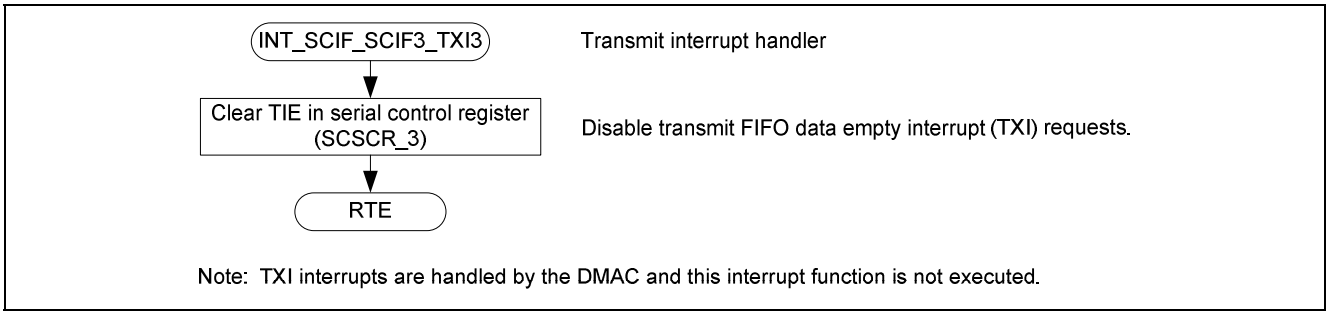


Figure 12 Processing Sequence of SCIF Transmit Interrupt Handler

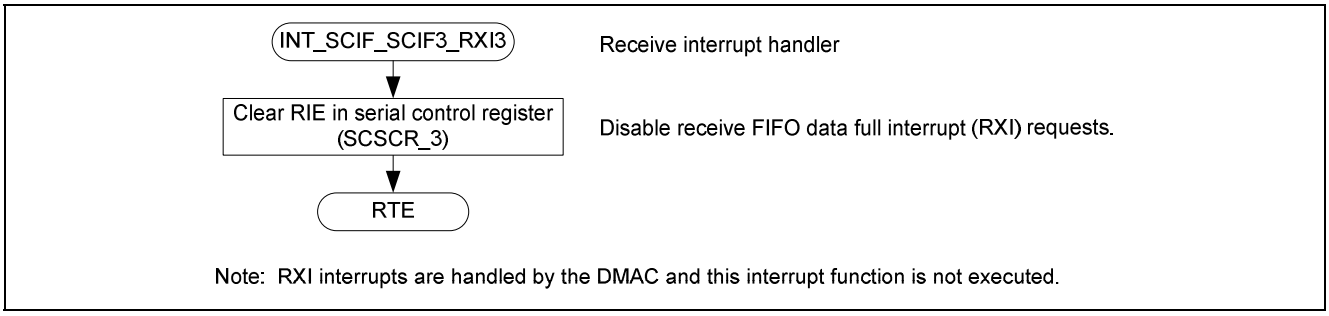


Figure 13 Processing Sequence of SCIF Receive Interrupt Handler

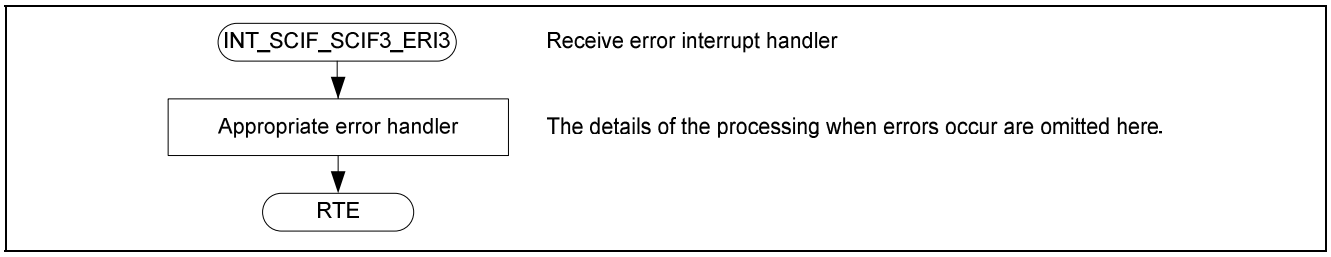


Figure 14 Processing Sequence of SCIF Receive Error Interrupt Handler

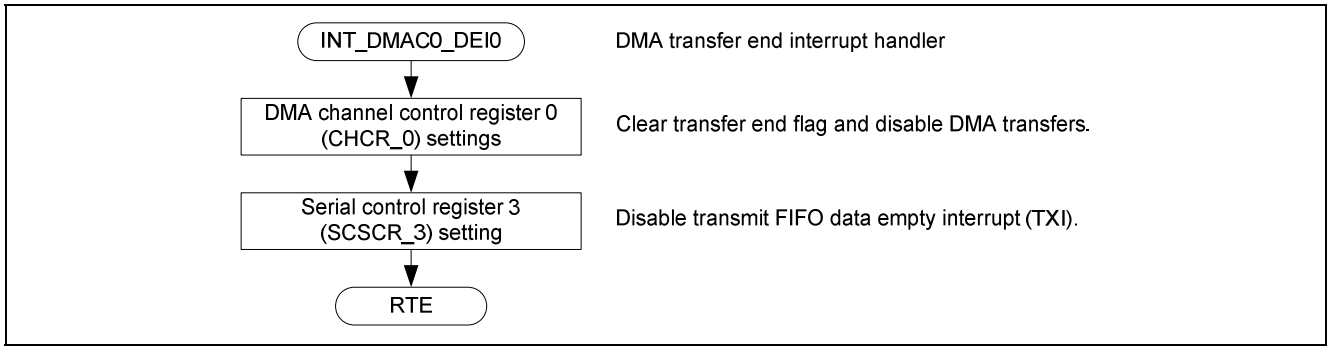


Figure 15 Processing Sequence of DMAC Channel 0 Interrupt Handler

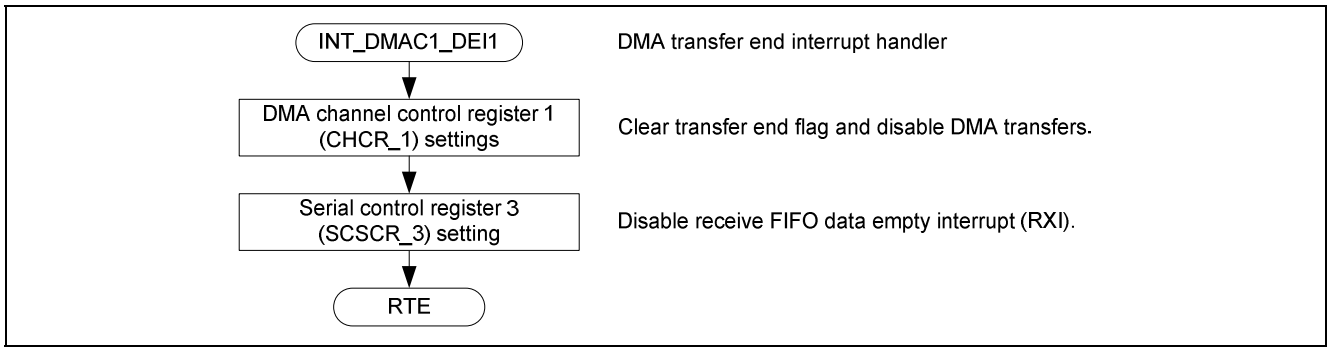


Figure 16 Processing Sequence of DMAC Channel 1 Interrupt Handler

2.4 Register Settings for Sample Program

The register setting values used in the sample program are described below.

2.4.1 Clock Pulse Generator (CPG)

Table 6 lists the clock pulse generator settings.

Table 6 Clock Pulse Generator Settings

Register	Address	Setting value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC[2:0] = B'011: ×1/8 (Bϕ) IFC[2:0] = B'000: ×1/4 (Iϕ) PFC[2:0] = B'011: ×1/8 (Pϕ)

2.4.2 Power-Down Mode

Table 7 lists the standby control register (STBCR) settings.

Table 7 Standby Control Register Settings

Register	Address	Setting value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	Clear MSTP8 to 0: DMAC operates (initial value) Other bits: Initial values
Standby control register 4 (STBCR4)	H'FFFE040C	H'E7	Clear MSTP44 to 0: SCIF3 operates Other bits: Initial values

2.4.3 Interrupt Controller (INTC)

Table 8 lists the interrupt priority register (IPR) settings.

Table 8 Interrupt Priority Register Settings

Register	Address	Setting value	Description
Interrupt priority register 06 (IPR06)	H'FFFE0C00	H'FF00	Set DMAC0 interrupt level to 15 (bits 15 to 12). Set DMAC1 interrupt level to 15 (bits 11 to 8).
Interrupt priority register 14 (IPR14)	H'FFFE0C10	H'000F	Set SCIF3 interrupt level to 15 (bits 3 to 0).

2.4.4 Direct Memory Access Controller (DMAC)

Table 9 lists the register settings for DMAC (channel 0) and table 10 for DMAC (channel 1).

Table 9 DMAC (Channel 0) Register Settings

Register	Address	Setting value	Description
DMA source address register 0 (SAR_0)	H'FFFE1000	—	Set the start address of the character string in on-chip flash memory as the DMA transfer source address.
DMA destination address register 0 (DAR_0)	H'FFFE1004	H'FFFE980C	Set the SCIF3 transmit FIFO data register (SCFTDR_3) as the DMA transfer destination address.
DMA transfer count register 0 (DMATCR_0)	H'FFFE1008	H'00000020	Set the DMA transfer count to 32. (Set the single transfer size to one byte in CHCR_0.)
DMA channel control register 0 (CHCR_0)	H'FFFE100C	H'00001804 (initial setting value)	TC = 0: 1 transfer per transfer request RLD = 0: Reload function disabled (initial value) DM[1:0] = B'00: Fixed destination address SM[1:0] = B'01: Increment source address RS[3:0] = B'1000: DMA extension resource selector TB = 0: Cycle steal mode (initial value) TS[1:0] = B'00: Transfer unit set to one byte IE = 1: Interrupt requests enabled TE: Clear to 0 at DMA transfer end interrupt. DE: Before DMAC initial settings, clear to 0 to disable DMA transfers (initial value). After DMAC initial settings, set to 1 to enable DMA transfers. Clear to 0 to disable DMA transfers at DMA transfer end interrupt.
DMA operation register (DMAOR)	H'FFFE1200	—	DME: After DMAC initial settings, set to 1 to enable DMA transfers on all channels. Clear to 0 to disable DMA transfers on all channels at DMA transfer end interrupt.
DMA extension resource selector 0 (DMARS0)	H'FFFE1300	H'xx8D	Set SCIF3 (TXI3) as activation source for channel 0.

Table 10 DMAC (Channel 1) Register Settings

Register	Address	Setting value	Description
DMA source address register 1 (SAR_1)	H'FFFE1010	—	Set the start address of the character string in on-chip flash memory as the DMA transfer source address.
DMA destination address register 1 (DAR_1)	H'FFFE1014	H'FFFE980C	Set the SCIF3 transmit FIFO data register (SCFTDR_3) as the DMA transfer destination address.
DMA transfer count register 1 (DMATCR_1)	H'FFFE1018	H'00000020	Set the DMA transfer count to 32. (Set the single transfer size in CHCR_0.)
DMA channel control register 1 (CHCR_1)	H'FFFE101C	H'00004804 (initial setting value)	TC = 0: 1 transfer per transfer request RLD = 0: Reload function disabled (initial value) DM[1:0] = B'01: Increment destination address SM[1:0] = B'00: Fixed source address RS[3:0] = B'1000: DMA extension resource selector TB = 0: Cycle steal mode (initial value) TS[1:0] = B'00: Transfer unit set to one byte IE = 1: Interrupt requests enabled TE: Clear to 0 at DMA transfer end interrupt. DE: Before DMAC initial settings, clear to 0 to disable DMA transfers (initial value). After DMAC initial settings, set to 1 to enable DMA transfers. Clear to 0 to disable DMA transfers at DMA transfer end interrupt.
DMA operation register (DMAOR)	H'FFFE1200	—	DME: After DMAC initial settings, set to 1 to enable DMA transfers on all channels. Clear to 0 to disable DMA transfers on all channels at DMA transfer end interrupt.
DMA extension resource selector 0 (DMARS0)	H'FFFE1300	H'8Exx	Set SCIF3 (RXI3) as activation source for channel 1.

2.4.5 Serial Communication Interface with FIFO (SCIF)

Table 11 lists the SCIF register settings.

Table 11 SCIF register settings

Register	Address	Setting value	Description
Serial control register 3 (SCSCR_3)	H'FFFE9808	H'0000	Initial value TIE = 0: Transmit FIFO data empty interrupt (TXI) requests disabled RIE = 0: Receive FIFO data full interrupt (RXI) requests and receive error interrupt (ERI) request requests disabled TE = 0: Transmit operation disabled RE = 0: Receive operation disabled
			When making settings Asynchronous mode CEK[1:0] = B'00: Internal clock/SCK pin set as input pin
		H'00F8	When transmit/receive enabled TIE = 1: Transmit FIFO data empty interrupt (TXI) requests enabled RIE = 1: Receive FIFO data full interrupt (RXI) requests and receive error interrupt (ERI) requests enabled TE = 1: Transmit operation enabled RE = 1: Receive operation enabled
		H'0078	When transmit/receive ends TIE = 0: Transmit FIFO data empty interrupt (TXI) requests disabled RIE = 1: Receive FIFO data full interrupt (RXI) requests disabled
FIFO control register 3 (SCFCR_3)	H'FFFE9818	H'0006	Initial settings RTRG = 0: Specified receive trigger count (1) TTRG = 0: Specified transmit trigger count (8) TFRST = 1: SCFTDR resets enabled RFRST = 1: SCFRDR resets enabled
		H'0030	Initial settings RTRG = 0: Specified receive trigger count (1) TTRG = 3: Specified transmit trigger count (16) TFRST = 0: SCFTDR resets disabled RFRST = 0: SCFRDR resets disabled
Serial status register 3 (SCFSR_3)	H'FFFE9810	H'0060	Initial settings TDRE = 1: Transmit data register empty flag TEND = 1: Transmit end flag
Line status register 3 (SCLSR_3)	H'FFFE9824	H'0000	Initial settings ORER = 0: Overrun error flag
Serial mode register 3 (SCSMR_3)	H'FFFE9800	H'0000	C/A = 0: Asynchronous mode CHR = 0: 8-bit data PE = 0: Add parity bit, disable checking STOP = 0: 1 stop bit CKS[1:0] = B'00: Pϕ clock
Bit rate register 3 (SCBBR_3)	H'FFFE9804	D'80	Asynchronous mode 19,200 bps (50 MHz)

3. Reference Documents

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual
  SH7216 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.27.10	—	First edition issued
1.01	Jun.25.10	—	Modifications to source project due to change in FRQCR setting method

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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