SH7216 Group

MTU2 PWM Output (PWM mode 1)

R01AN0722EJ0100
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Introduction

This application note describes a sample program for outputting a single-phase PWM waveform by using pulse width modulation (PWM) mode 1 of the SH7216's multi-function timer pulse unit 2 (MTU2).

Target Device

SH7216

Contents

1. Preface 2
2. Description of Sample Application 4
3. Documents for Reference 14

1. Preface

1.1 Specifications

The sample program described in this application note uses a PWM mode function (PWM mode 1) of multi-function timer pulse unit 2 (MTU2) to output a single-phase PWM waveform. Figure 1 shows the configuration.

- Channel 3 of MTU2 is set to PWM mode 1.
- The PWM waveform output pin is TIOC3A.
- The PWM waveform active level is set to high, with high-level output at TGRB compare-match and low-level output at TGRA compare-match.*[1]
- The carrier cycle is set to 400 µsec.
- TCNT is cleared at TGRA compare-match.
- TGRA and TGRC perform buffered operation in which data is transferred from TGRC to TGRA when TCNT is cleared each carrier cycle (= TCNT clear cycle).
- TGRB and TGRD perform buffered operation in which data is transferred from TGRD to TGRB when TCNT is cleared, according to the PWM duty.
- An interrupt (TGIA_3 interrupt) is generated each time TCNT is cleared, and the interrupt handler updates the PWM duty in TGRD.

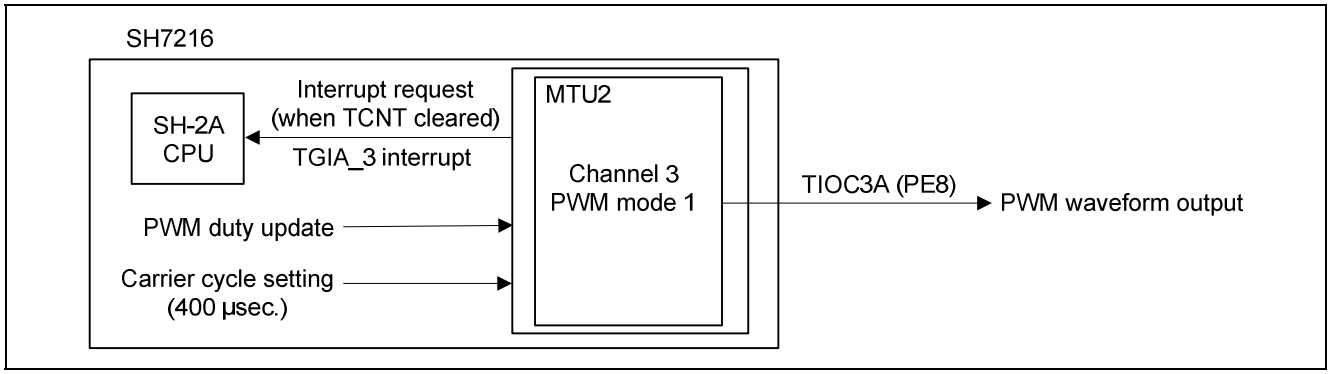

Figure 1 Single-Phase PWM Waveform Output (PWM Mode 1)

Note: 1. When the output duty is set to 100%, high-level output is produced at both TGRB compare-match and TGRA compare-match.

1.2 Module Used

Channel 3 of multi-function timer pulse unit 2 (MTU2)

1.3 Applicable Conditions

MCU:	SH7216 [R5F72167]
Operating frequencies:	Internal clock: Iϕ = 200 MHz
	Bus clock: Bϕ = 50 MHz
	Peripheral clock: Pϕ = 50 MHz
	MTU2S clock: Mϕ = 100 MHz
	AD clock: Aϕ = 50 MHz
MCU operating mode:	Single-chip mode
Integrated development environment:	Renesas Electronics High-performance Embedded Workshop, Ver.4.08.00.011
C compiler:	Renesas Electronics SuperH RISC engine Family
	C/C++ Compiler Package, Ver.9.04, Release00
Compile options:	High-performance Embedded Workshop default settings
	(-cpu=sh2afpu -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Notes

Application notes related to this application note are listed below. Refer to them in conjunction with this application note.

- SH7216 Group MTU2 Asymmetric Complementary PWM Output (Complementary PWM Mode) (R01AN0672EJ0100)
- SH7216 Group MTU2 Three-Phase Complementary PWM Output Function (Complementary PWM Mode) (REJ06B1017)
- SH7216 Group MTU2 Three-Phase Sine Wave PWM Output (Complementary PWM Mode) (R01AN0157EJ)
- SH7216 Group MTU2 Positive/Negative Three-Phase PWM Output Function (Reset-Synchronized PWM Mode) (R01AN0035EJ0100)

2. Description of Sample Application

In this sample application, PWM mode 1 of multi-function timer pulse unit 2 (MTU2) is used.

For details of PWM mode 1 of MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in *SH7216 Group User's Manual: Hardware* (R01UH0230EJ0300).

2.1 Operation of Sample Program

2.1.1 Settings for Operation of Sample Program

In the sample program, channel 3 of multi-function timer pulse unit 2 (MTU2) is set to PWM mode 1, and a PWM waveform is output from the TIOCA pin.

Table 1 lists the settings for operation in PWM mode 1.

Table 1 Settings for Operation in PWM Mode 1

Item	Description
Channels in use	Channel 3
Operating mode	PWM mode 1
Functions of pins	• TIOC3A pin: PWM waveform output The initial output is low; it changes to high at TGRB_3 compare-match and then to low at TGRA_3. However, output is high at both TGRB_3 and TGRA_3 compare-match when the duty is set to 100%.
Counter clock	12.5 MHz (Pϕ clock divided by 4)
PWM carrier cycle	400 µsec (carrier frequency: 2.5 kHz)
PWM duty transfer timing	TGRB_3 and TGRD_3 perform buffered operation in which the PWM duty value is transferred from TGRD_3 to TGRB_3 when TCNT_3 is cleared.
PWM duty	The waveform is output with a PWM duty of 70%, 30%, 100%, or 0%.
Interrupts	• TGRA_3 compare-match (TCNT_3 clear) interrupt The carrier cycle is generated by TGRA_3 compare-match.

2.1.2 Description of Operation by the Sample Program

The sample program sets the carrier cycle in TGRA_3 and the duty in TGRD_3. Then, the PWM duty setting in TGRD_3 is updated at each TGRA_3 compare-match interrupt, which occurs each carrier cycle. TGRB_3 and TGRD_3 perform buffered operation in which the PWM duty value set in TGRD_3 is transferred to TGRB_3 when MTU2 clears TCNT_3.

The output from TIOC3A is driven high when a TGRB_3 compare-match interrupt occurs, and the output from TIOC3A is driven low when a TGRA_3 compare-match interrupt occurs.

The sample program repeatedly outputs a PWM waveform with PWM duty of 70%, 70%, 0%, 30%, 70%, 70%, 100%, and 30% from the TIOC3A pin.

Figure 2 illustrates PWM waveform output with PWM duty of 70%, 70%, 0%, and 30% (timepoints t0, t1, t2, t3, and t4), and figure 3 illustrates PWM waveform output with PWM duty of 70%, 70%, 0%, and 30% (timepoints t4, t5, t6, t7, and t8). In this case the MTU2 operating clock frequency is 12.5 MHz, the carrier cycle is 400 µsec. (carrier frequency: 2.5 kHz), and the setting value of TGRA_3 is H'1388 (equivalent to carrier cycle).

- Timepoint t0 (= timepoint t8)
  TGRD_3 is set to H'5DC ((100 – 70)% of carrier cycle), and a PWM waveform is output with PWM duty of 70% from t1 to t2. TIORH_3 is set to H'21 so that the output is driven high at TGRB_3 compare-match and low at TGRA_3 compare-match.
- Timepoint t1
  TGRB_3 is set to H'1389 (carrier cycle + 1), and a PWM waveform is output with PWM duty of 0% (solid off) from t2 to t3. No TGRB_3 compare-match occurs.
- Timepoint t2
  TGRD_3 is set to H'DAC ((100 – 30)% of carrier cycle), and a PWM waveform is output with PWM duty of 30% from t3 to t4.
- Timepoint t3
  TGRD_3 is set to H'5DC ((100 – 70)% of carrier cycle), and a PWM waveform is output with PWM duty of 70% from t4 to t5.
- Timepoint t4
  TGRD_3 is set to H'5DC ((100 – 70)% of carrier cycle), and a PWM waveform is output with PWM duty of 70% from t5 to t6.
- Timepoint t5
  TGRD_3 is set to H'0 ((100 – 100)% of carrier cycle), and TIORH_3 is set to H'22 so that the output is driven high at both TGRB_3 and TGRA_3 compare-match. A PWM waveform is output with PWM duty of 100% (solid on) from t6 to t7.
- Timepoint t6
  TGRD_3 is set to H'DAC ((100 – 30)% of carrier cycle) and the TIORH_3 setting returns to H'21 at timepoint t6 so that the output is driven high at TGRB_3 compare-match and low at TGRA_3 compare-match. A PWM waveform is output with PWM duty of 30% from t7 to t8.
- Timepoint t7
  TGRD_3 is set to H'5DC ((100 – 70)% of carrier cycle), and a PWM waveform is output with PWM duty of 70% from t0 to t1.

Carrier frequency: 2.5 kHz (carrier cycle: 400 µs),
TGRA value: H'1388 (=5,000), MTU2 operating clock: 12.5 MHz (= Pϕ / 4),
TGRD → TGRB when TCNT cleared

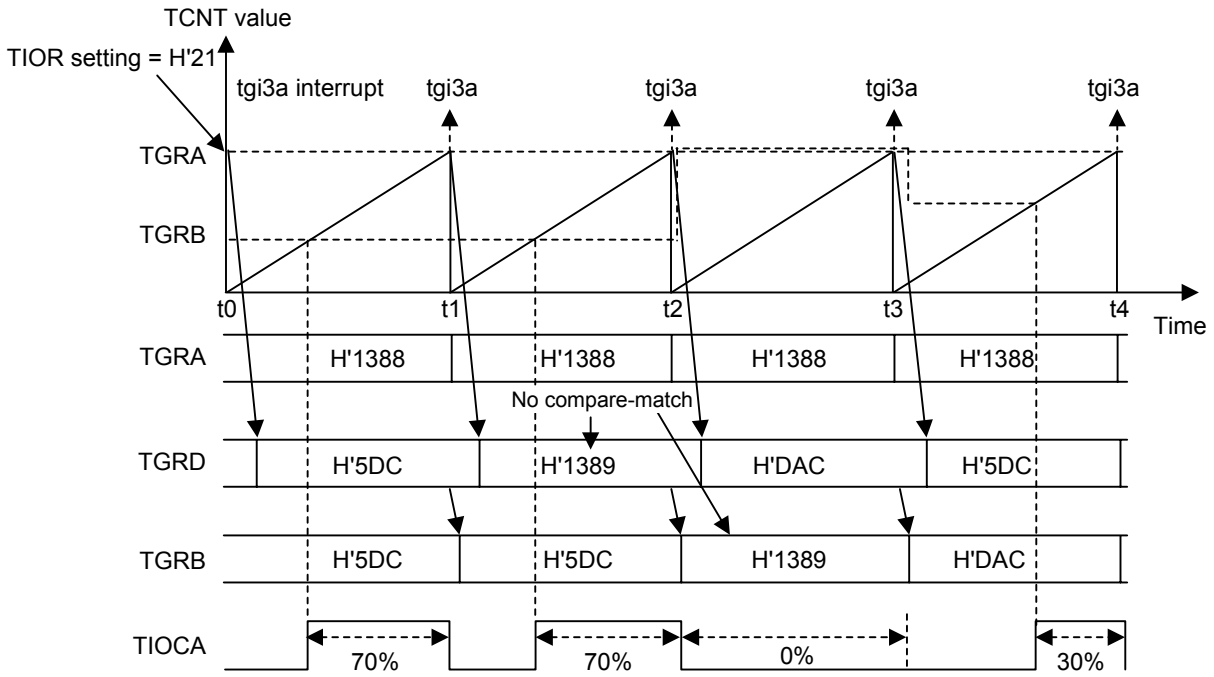

Figure 2 PWM Output Waveform (70%, 70%, 0%, 30%)

Carrier frequency: 2.5 kHz (carrier cycle: 400 µs),
TGRA value: H'1388 (=5,000), MTU2 operating clock: 12.5 MHz (= Pϕ / 4),
TGRD → TGRB when TCNT cleared

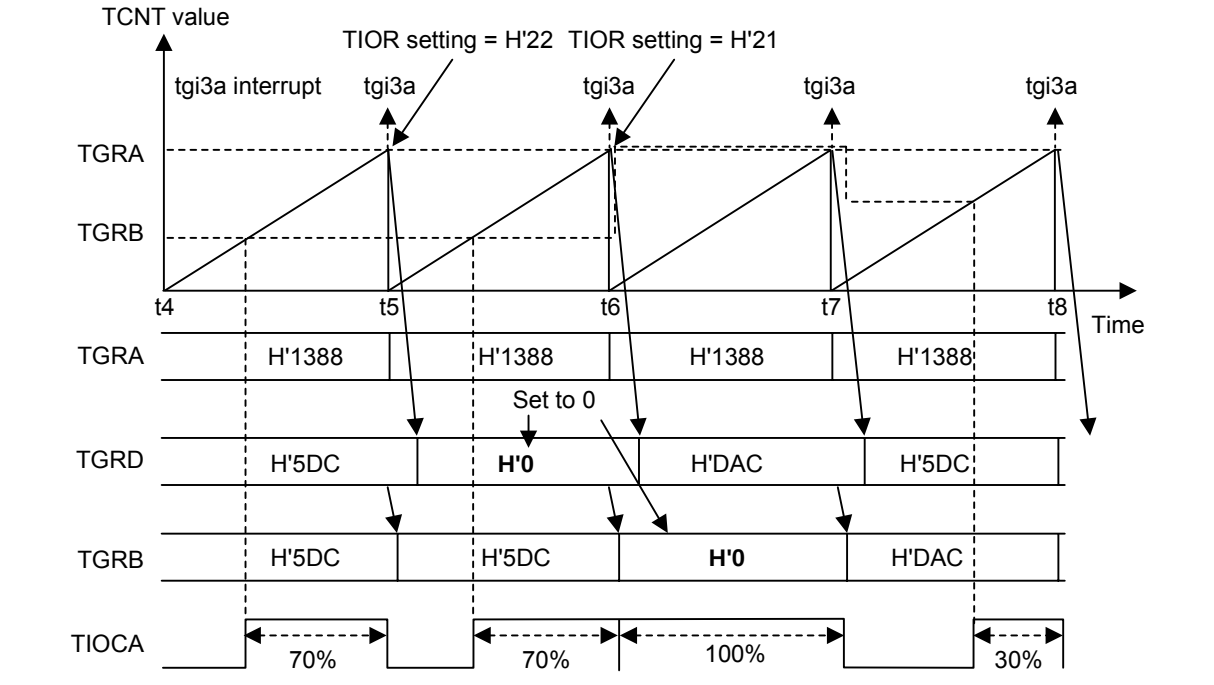

Figure 3 PWM Output Waveform (70%, 70%, 100%, 30%)

2.2 Configuration of Sample Program

2.2.1 Description of Functions

Table 2 lists the functions used in the sample program.

Table 2 Functions Used

Function	Description
main()	Main function Makes initial settings for each module and makes timer start settings for multi-function timer pulse unit 2 (MTU2).
stbcr_init ()	Standby setting Cancels MTU2 module standby.
mtu2_init()	MTU2 (channel 3) initial settings Makes PWM mode 1 and buffer operation settings. Makes initial carrier cycle and PWM duty settings. Makes initial PWM waveform output settings. Makes PWM duty transfer timing settings.
pfc_init()	Pin function controller (PFC) initial settings Sets the PE8 pin to the MTU2 TIOC3A pin function. Sets the PE8 pin to output.
int_mtu2_tgi3a()	MTU2 (channel 3) TGRA_3 compare-match interrupt handler Clears the TGFA_3 interrupt flag. Increments the int_count variable. Specifies high-level output at both TGRB_3 and TGRA_3 compare-match for output with PWM duty of 100%. Specifies high-level output at TGRB_3 compare-match and low-level output at TGRA_3 compare-match for output with PWM duty of other than 100%. An interrupt is occurred every PWM carrier cycle (400 µs).

2.2.2 Variables and Constants Used

Table 3 lists the variables and constants used in the sample program.

Table 3 Variables and Constants Used

Variable	Description	Used by Function
int_count	This is an index that indicates the PWM duty setting value. It takes an integer value between 0 and 7.	int_mtu2_tgi3a()
pul_pwm_duty[]	The PWM duty setting value. Each element corresponds to a duty of 70%, 30%, 100%, or 0%, as shown below. [0] H'05DC (70% duty) [1] H'05DC (70% duty) [2] H'1389 (0% duty) [3] H'0DAC (30% duty) [4] H'05DC (70% duty) [5] H'05DC (70% duty) [6] H'0000 (100% duty) [7] H'0DAC (30% duty)	int_mtu2_tgi3a()

2.3 Setting Procedure for Module Used

The processing sequences of the sample program are shown below.

2.3.1 Main Function

Figure 4 shows the processing sequence of the main function.

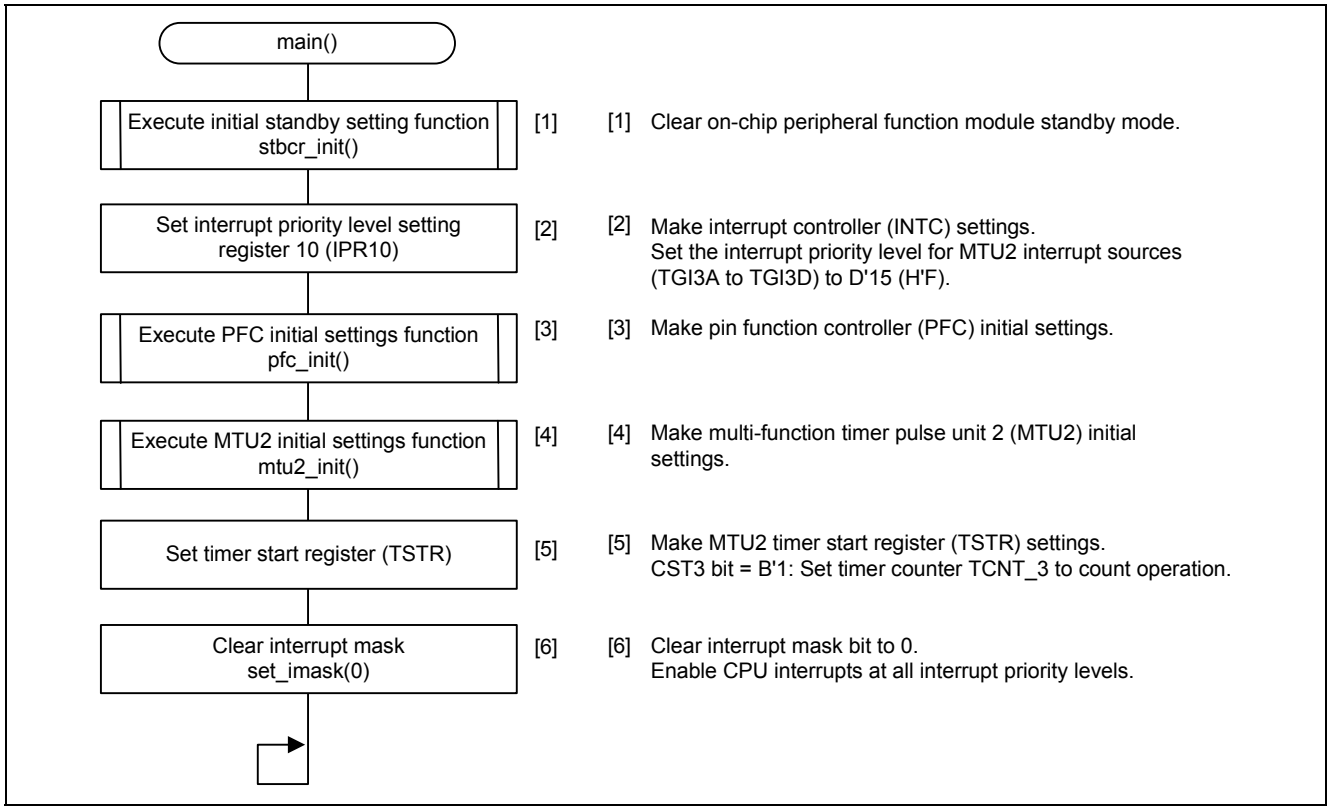

Figure 4 Processing by Function main

2.3.2 Initial Settings for Standby Controller

Figure 5 shows the processing sequence for making initial settings to the standby controller.

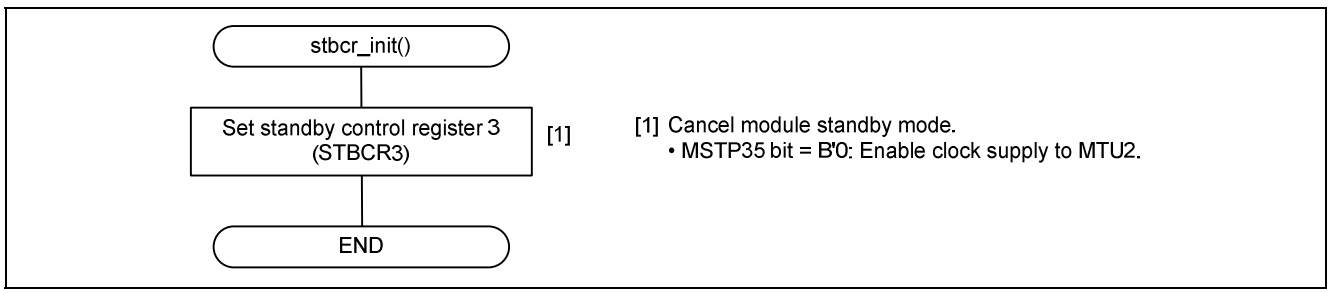

Figure 5 Initial Settings for Standby Controller

2.3.3 Initial Settings for Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 6 shows the processing sequence for making initial settings to multi-function timer pulse unit 2 (MTU2). Channel 3 is set to PWM mode 1.

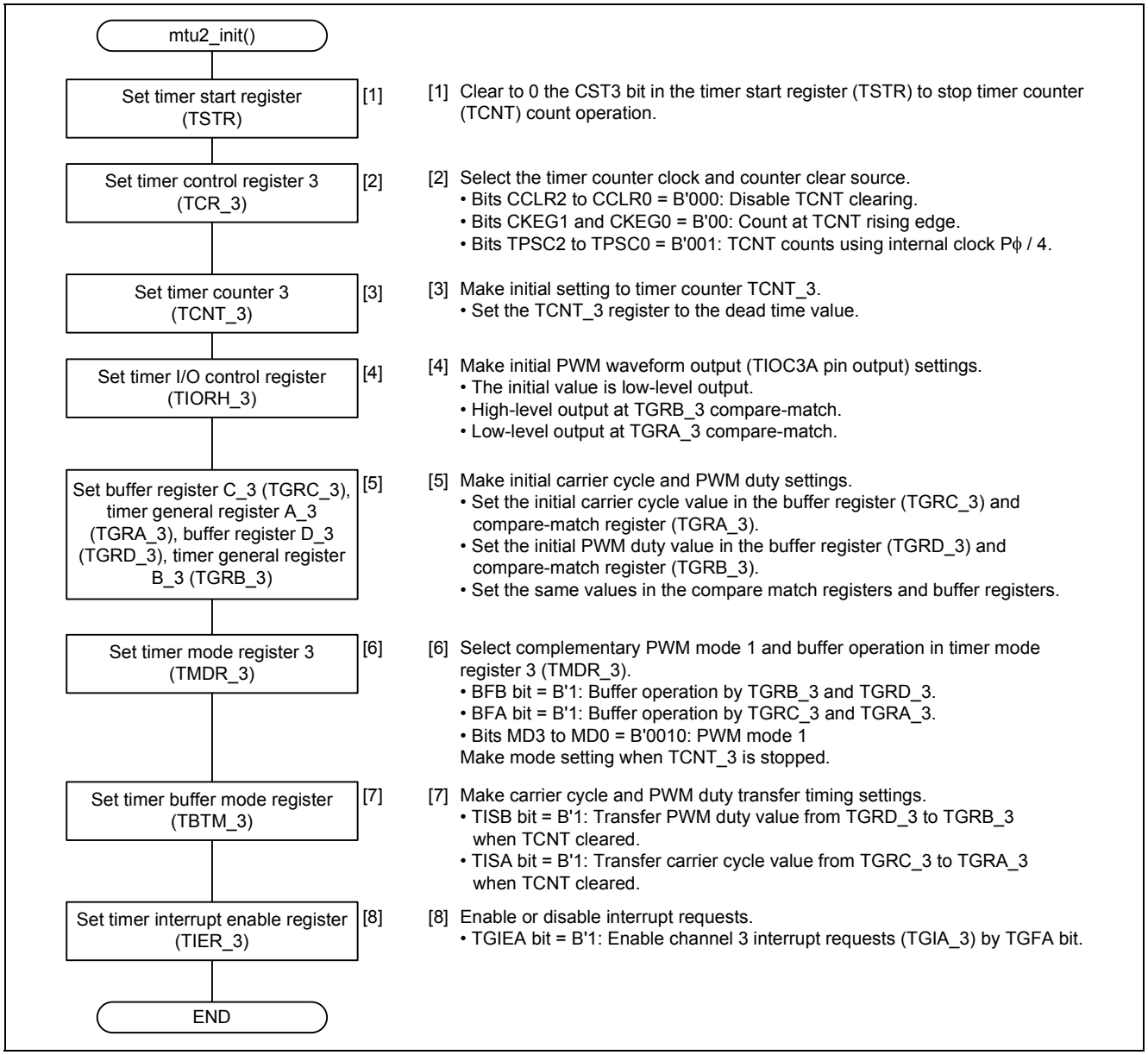

Figure 6 Initial Settings for Multi-Function Timer Pulse Unit 2 (MTU2)

2.3.4 Initial Settings for Pin Function Controller (PFC)

Figure 7 shows the processing sequence for making initial settings to the pin function controller (PFC).

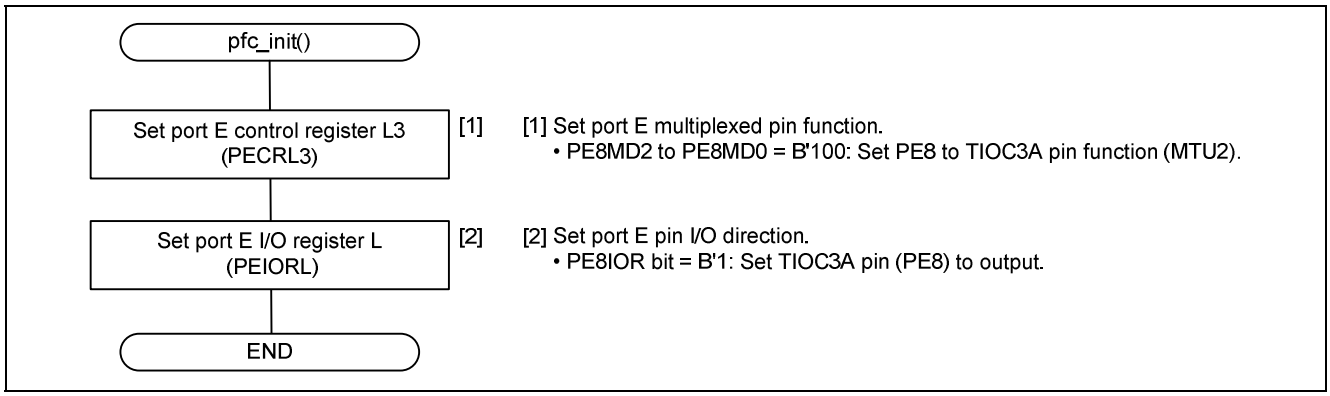

Figure 7 Initial Settings for Pin Function Controller (PFC)

2.3.5 Compare-Match Interrupt Handler

Figure 8 shows the processing sequence of the handler for the MTU2 compare-match interrupt (TGRA_3).

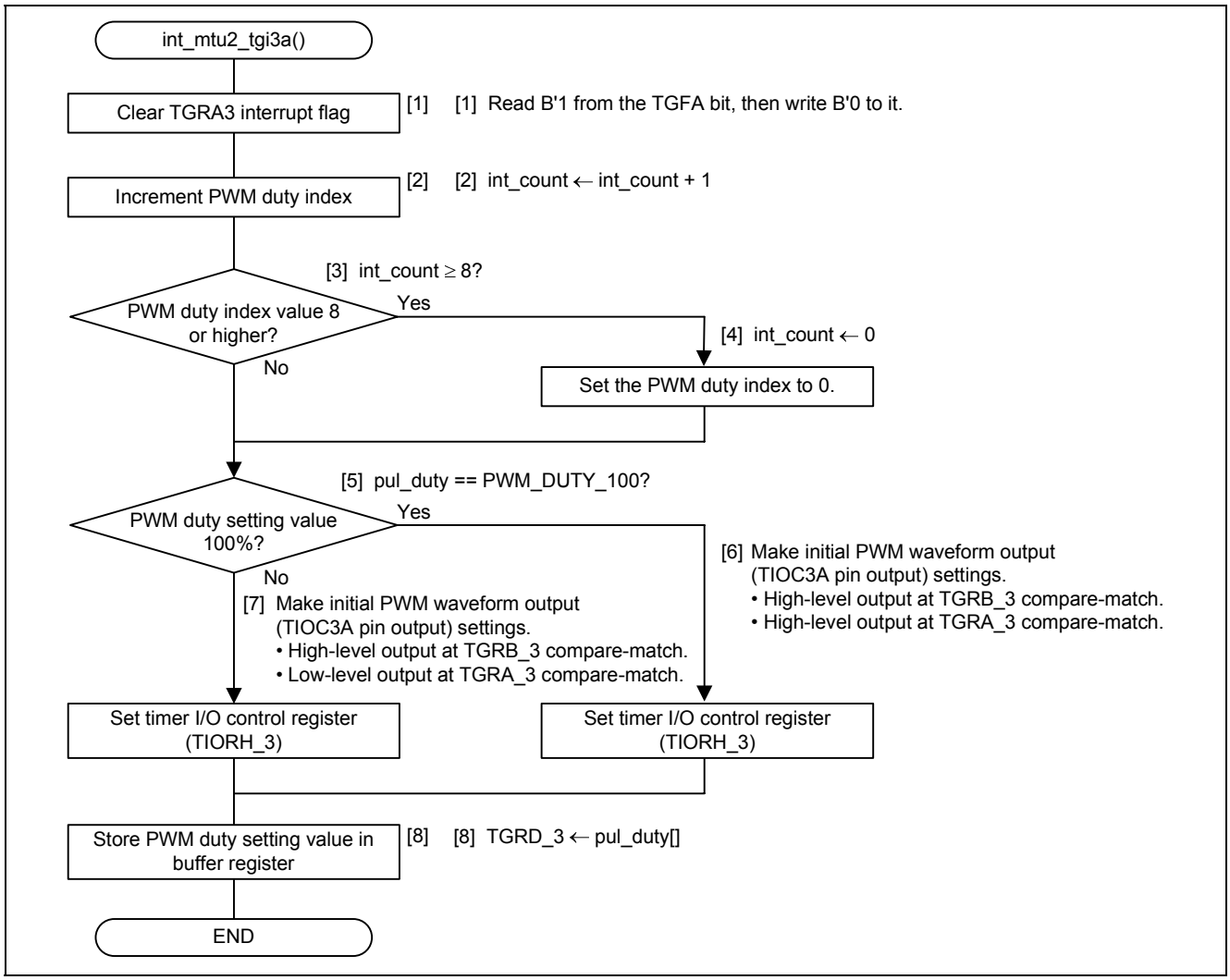

Figure 8 MTU2 Compare-Match Interrupt (TGRA_3) Handler

2.4 Register Settings in Sample Program

The register settings used in the sample program are described below.

2.4.1 Clock Pulse Generator (CPG)

Table 4 lists the register settings for the clock pulse generator (CPG).

Table 4 Clock Pulse Generator (CPG)

Register	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0303	Specifies the clock output settings and operating frequency multiplication ratios. • STC2 to STC0 = B'011: Bus clock (Bϕ) × 1/4 • IFC2 to IFC0 = B'000: Internal clock (Iϕ) × 1 • PFC2 to PFC0 = B'011: Peripheral clock (Pϕ) × 1/4

2.4.2 Power-Down Mode

Table 5 shows the register settings for power-down (low-power) mode.

Table 5 Power-Down Mode

Register	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE0408	H'5E	Specifies the operation settings for individual modules. • HIZ = B'0: Maintain pin state in software standby mode. • MSTP36 = B'1: Stop clock supply to MTU2S. • MSTP35 = B'0: MTU2 operation enabled. • MSTP34 = B'1: Reserved bit • MSTP33 = B'1: Stop clock supply to IIC3. • MSTP32 = B'1: Stop clock supply to ADC. • MSTP31 = B'1: Reserved bit • MSTP30 = B'0: Flash memory operation enabled.

2.4.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 6 lists the register settings for multi-function timer pulse unit 2 (MTU2).

Table 6 Multi-Function Timer Pulse Unit 2 (MTU2)

Register	Address	Setting	Description
Timer control register 3 (TCR_3)	H'FFFE4200	H'21	TCNT control settings • CCLR2 to CCLR0 = B'001: Clear TCNT at TGRA_3 compare-match. • CKEG1 to CKEG0 = B'00: Count at rising edge. • TPSC2 to TPSC0 = B'001: TCNT counts using internal clock Pϕ / 4.
Timer I/O Control Register H_3 (TIORH_3)	H'FFFE4204	H'21 or H'22	Sets TIOC3A output. Initial output level: Low 1. When PWM duty is other than 100% — IOB3 to IOB0 = B'0010: High-level output at TGRB_3 compare-match — IOA3 to IOA0 = B'0001: Low-level output at TGRB_3 compare-match 2. When PWM duty is 100% — IOB3 to IOB0 = B'0010: High-level output at TGRB_3 compare-match — IOA3 to IOA0 = B'0010: High-level output at TGRB_3 compare-match
Timer counter 3 (TCNT_3)	H'FFFE4210	H'00	16-bit counter Set initial value to H'0000.
Timer general register A_3 (TGRA_3)	H'FFFE4218	H'1388	Sets the carrier cycle. Set to H'1388 (= 5000), which corresponds to 400 µsec.
Timer general register C_3 (TGRC_3)	H'FFFE4224		TGRA_3 buffer register Set to same value as TGRA_3 register.
Timer general register B_3 (TGRB_3)	H'FFFE421A	H'0 to H'1389	Sets the PWM duty. 1. When PWM duty is other than 0% Set to H'1389 (= carrier cycle + 1). 2. When PWM duty is 0% Set to H'1388* (100% – PWM duty %).
Timer general register D_3 (TGRD_3)	H'FFFE4226		TGRB_3 buffer register Set initial setting to same value as TGRB_3 register. PWM duty value updates are set in this register.
Timer mode register 3 (TMDR_3)	H'FFFE4202	H'32	Sets the operating mode (channel 3). • BFB = B'1: Buffer operation by TGRB and TGRD • BFA = B'1: Buffer operation by TGRA and TGRC • MD3 to MD0 = B'0010: PWM mode 1
Timer buffer operation transfer mode register 3 (TBTM_3)	H'FFFE4238	H'03	Sets the timing of transfers from the buffer registers to the timer general registers. • TTSB = B'1: Transfer value from TGRD_3 to TGRB_3 when TCNT is cleared. • TTSA = B'1: Transfer value from TGRC_3 to TGRA_3 when TCNT is cleared.

Register	Address	Setting	Description
Timer interrupt enable register 3 (TIER_3)	H'FFFE4208	H'01	Enables or disables interrupt requests. • TGIEA = B'1: Enable interrupt request (TGIA) trigged by TGFA bit.
Timer start register (TSTR)	H'FFFE4280	H'40	Enables or disables TCNT operation for channels 0 to 4. • CST3 = B'1: Enable TCNT_3 count operation. Disable count operation for TCNT_2, TCNT_1, and TCNT_0.

2.4.4 Interrupt Controller (INTC)

Table 7 lists the register settings for the interrupt controller (INTC).

Table 7 Interrupt Controller (INTC)

Register	Address	Setting	Description
Interrupt priority level setting register 10 (IPR10)	H'FFFE0C08	H'00F0	Sets interrupt priority levels (level 0 to 15). • Bits 15 to 12 = B'0000: MTU2 (TGIA_2 and TGIB_2) interrupt level = 0 • Bits 11 to 8 = B'0000: MTU2 (TCIV_2 and TCIU_2) interrupt level = 0 • Bits 7 to 4 = B'1111: MTU2 (TGIA_3 to TGID_3) interrupt level = 15 • Bits 3 to 0 = B'0000: MTU2 (TCIV_3) interrupt level = 0 The TGIA_3 interrupt is used by the sample program.

2.4.5 Pin Function Controller (PFC)

Table 8 lists the register settings for the pin function controller (PFC).

Table 8 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port E control register L3 (PECRL3)	H'FFFE3A12	H'0004	Sets port E multiplexed pin functions. • PE11MD2 to PE11MD0 = B'000: Set PE11 to PE11 I/O (port). • PE10MD2 to PE10MD0 = B'000: Set PE10 to PE10 I/O (port). • PE9MD2 to PE9MD0 = B'000: Set PE9 to PE9 I/O (port). • PE8MD2 to PE8MD0 = B'100: Set PE8 to TIOC3A I/O (MTU2)
Port E I/O register L (PEIORL)	H'FFFE3A06	H'0100	Sets port E pin I/O directions. • PE8IOR = B'1: Set PE8 (TIOC3A) as an output pin. Set all the others to B'0: All input pins.

3. Documents for Reference

- Hardware Manual
  SH7216 Group Hardware Manual [R01UH0230EJ0300]
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Software Manual
  SH-2A/SH2A-FPU Software Manual [REJ09B0051]
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Aug.22.11	—	First edition issued

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
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   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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