SH7216 Group

MTU2 Phase Counting Mode 1 Output Function (Phase Counting Mode 1)

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Introduction

This application note describes example settings for processing two-phase encoder pulse (with Z-phase input) input signals using the phase counting mode of multi-function timer pulse unit 2 (MTU2).

Target Device

SH7216

Contents

1. Introduction 2
2. Description of Application Example 4
3. Documents for Reference 22

1. Introduction

1.1 Specifications

In this application example, phase counting mode (phase counting mode 1), a function of channel 1 of multi-function timer pulse unit 2 (MTU2) channel 1, is used to count the number of two-phase encoder (A-phase and B-phase) pulses with counter reset (Z-phase). In addition, the count value of a two-phase encoder with a 1 ms period is captured as the period timer for channel 0. Figure 1 illustrates the configuration.

1. A-phase and B-phase signals from the two-phase encoder are input to MTU2 channel 1 via the TCLKA and TCLKB pins, respectively, and the number of two-phase encoder 4× pulses is counted.
2. The two-phase encoder Z-phase signal is input to channel 1 via the TIOC1A pin. The TIOC1A pin is set to rising-edge signal detection (input-capture), and the channel 1 counter is cleared to 0 when signal detection occurs.
3. MTU2 channel 0 is set as a compare-match timer with a 1 ms period. The compare-match signal it generates is used as an input-capture activation source by channel 1 to capture the count value of the encoder.
4. The input-capture function of MTU2 channel 0 is used to capture the edge intervals of the A-phase and B-phase pulse signals of the two-phase encoder.

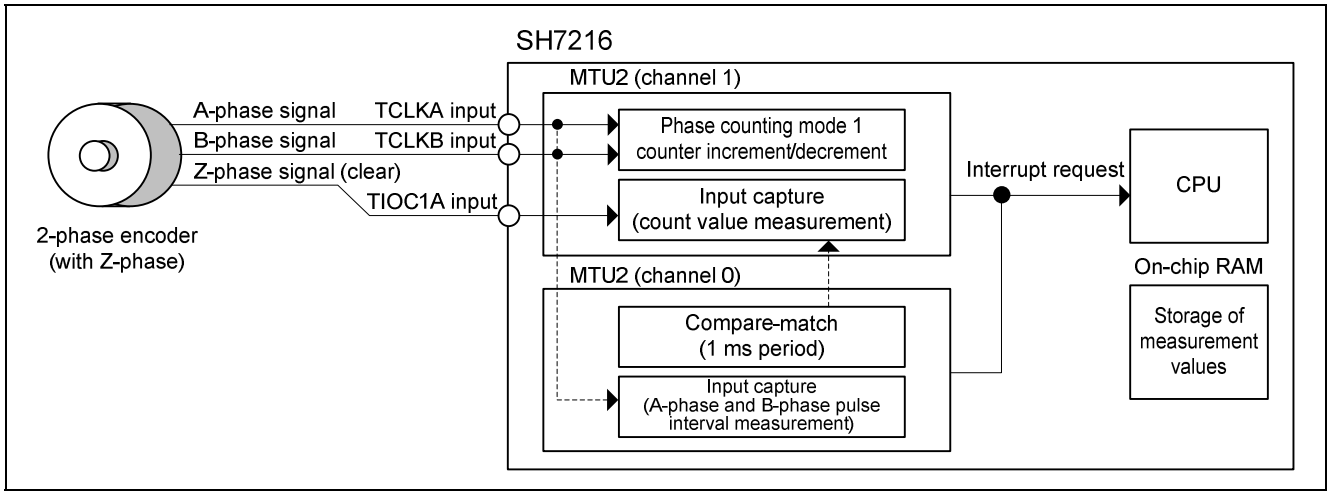


Figure 1 Two-Phase Encoder Pulse Detection (Phase Counting Mode 1)

1.2 Functions Used

Multi-function timer pulse unit 2 (MTU2) channels 0 and 1

1.3 Applicable Conditions

MCU	SH7216 [R5F72167]
Operating frequencies	Internal clock: Iϕ = 200 MHz Bus clock: Bϕ = 50 MHz Peripheral clock: Pϕ = 25 MHz MTU2S clock: Mϕ = 100 MHz AD clock: Aϕ = 50 MHz
MCU operating mode	Single-chip mode
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.07.00.007
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03, Release 02
Compile options	High-performance Embedded Workshop default settings (-cpu = sh2afpu -include = "$(WORKSPDIR)\inc" -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath - errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 - del_vacant_loop = 0 -struct_alloc = 1 - nologo)

2. Description of Application Example

This application example uses the phase counting mode of channel 1 of multi-function timer pulse unit 2 (MTU2).

2.1 Overview of Functions Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Multi-function timer pulse unit 2 (MTU2) comprises six 16-bit timer channels. Each channel has a variety of settings, including a compare-match function and input-capture function. By setting channels 3 and 4 to complementary PWM mode or reset-synchronized mode, six-line PWM output control is possible.

For details of MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the *SH7216 Group Hardware Manual* (REJ09B0543).

Table 1 shows an overview of multi-function timer pulse unit 2 (MTU2). Figure 2 is a block diagram of MTU2.

Table 1 Overview of Multi-Function Timer Pulse Unit 2 (MTU2)

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clocks	8 counter input clocks selectable per channel (4 clocks for channel 5)
Operation of channels 0 to 4	• Compare-match based waveform output, input-capture function, counter clear operation, simultaneous writing to multiple timer counters (TCNT), compare-match/input-capture based simultaneous clearing • Register input/output synchronized with counter, max. 12-phase PWM output by combining synchronous operation modes
A/D converter triggers	• Ability to generate conversion start trigger for A/D converter • In complementary PWM mode, ability to skip counter peak/trough interrupts or A/D converter conversion start triggers
Buffer operation	Ability to specify register buffer operation for channels 0, 3, and 4
Operating modes	• Ability to specify PWM mode for channels 0 to 4 • Ability to specify phase counting mode independently for channels 1 and 2 • Ability to specify a total of 6 lines of PWM waveform output, three-phase positive and negative output using complementary PWM mode and reset-synchronized PWM mode, by using linked operation of channels 3 and 4
Interrupt requests	28 interrupt sources (compare-match, input-capture interrupt, etc.)
Other	• Cascade connection operation • High-speed access using internal 16-bit bus • Support for automatic transfer of register data • Ability to specify module standby mode • Support for dead time compensation counter function using channel 5

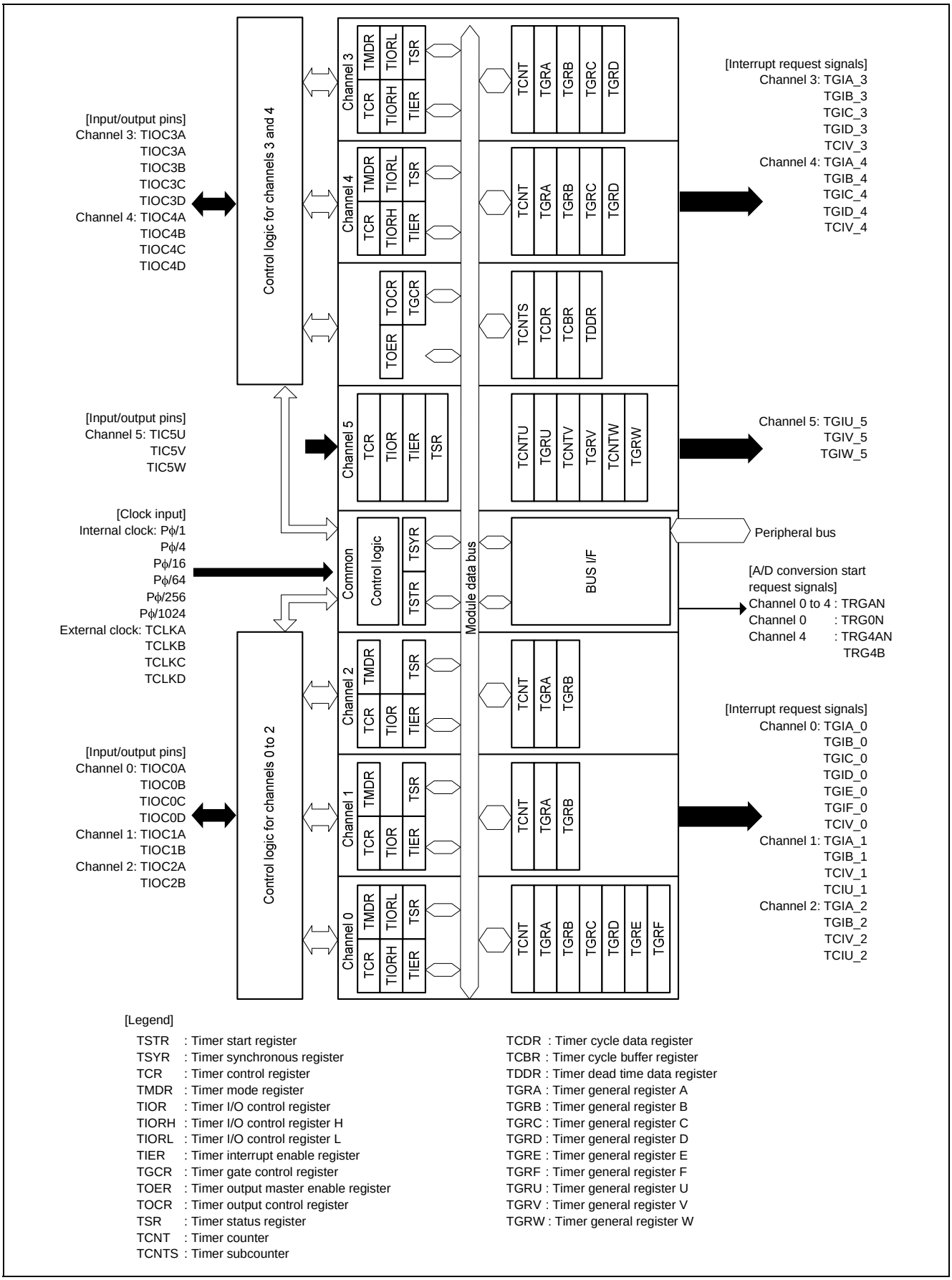


Figure 2 Block Diagram of MTU2

2.1.2 Phase Counting Mode

In phase counting mode, the phase difference between two external clock inputs (TCLKA and TCLKB pins or TCLKC and TCLKD pins) is detected, and timer counter TCNT is incremented or decremented accordingly.

Any one of four operating modes (phase counting mode 1, phase counting mode 2, phase counting mode 3, and phase counting mode 4) can be selected as the count condition for the timer counter in phase counting mode.

For details of phase counting mode, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the *SH7216 Group Hardware Manual* (REJ09B0543).

Figure 3 shows an operation in phase counting mode 1 as used in the application example. Table 2 lists the timer counter TCNT increment/decrement conditions in phase counting mode 1.

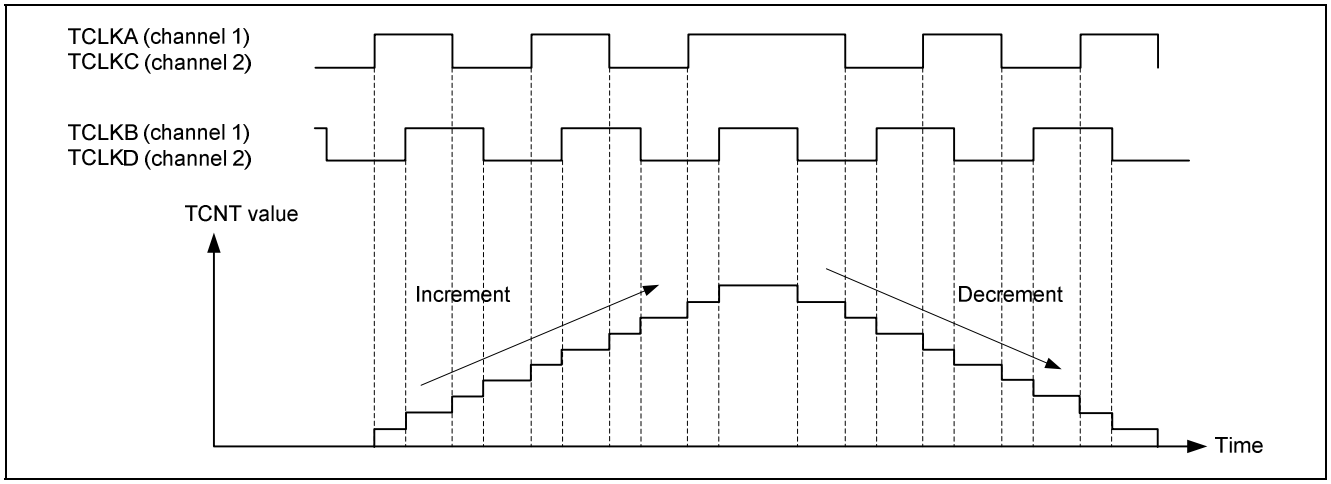


Figure 3 Phase Counting Mode 1 Operation Example (Channels 1 and 2)

Table 2 Increment/Decrement Conditions in Phase Counting Mode 1

TCLKA Pin (Channel 1) TCLKC Pin (Channel 2)	TCLKB Pin (Channel 1) TCLKD Pin (Channel 2)	TCNT Count Operation
High level	↑: Rising edge	Increment
Low level	↓: Falling edge	
↑: Rising edge	Low level	
↓: Falling edge	High level	
High level	↓: Falling edge	Decrement
Low level	↑: Rising edge	
↑: Rising edge	High level	
↓: Falling edge	Low level	

2.2 Operation of Reference Program

2.2.1 Reference Program Operation Settings

In the application example, channels 1 and channel 0 of multi-function timer pulse unit 2 (MTU2) operate alternately in coordinated fashion to count the pulse signals from a two-phase encoder of the type used by servo motors, etc., and the value is captured once every 1 ms. This enables calculation of the rotational position and speed of the motor.

Table 3 lists the setting conditions of the reference program. Figure 4 shows the timer configuration used by the reference program.

Table 3 Settings of Multi-Function Timer Pulse Unit 2 (MTU2)

Item	Description
Channels used	Channels 0 and 1
Operating mode	(1) Channel 1: Phase counting mode 1 (2) Channel 0: Normal operation (compare-match timer with 1 ms period)
Pin functions	• TCLKA input pin: Two-phase encoder A-phase pulse input (channel 1) • TCLKB input pin: Two-phase encoder B-phase pulse input (channel 1) • TIOC1A input pin: Encoder Z-phase (clear signal) input (channel 1)
Counter clock	(1) Channel 1: External clock pins (TCLKA, TCLKB) (2) Channel 0: Internal clock, 50 MHz (Pϕ/1, Pϕ = 50 MHz)
Interrupt	(1) Channel 1: • TGRA input-capture interrupt • TGRB input-capture interrupt • Timer counter underflow/overflow interrupt (2) Channel 0: • TGRB input-capture interrupt

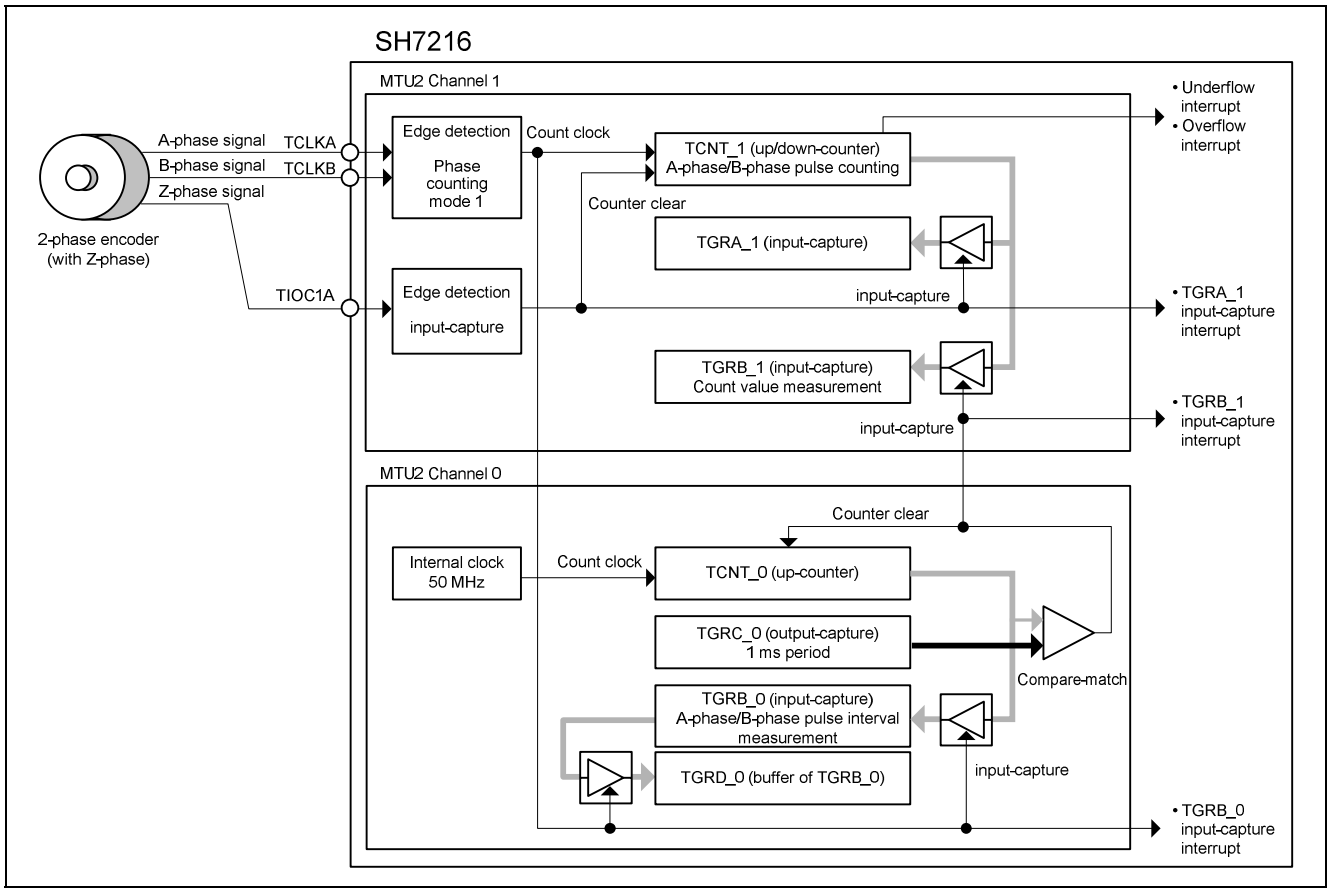


Figure 4 Configuration of MTU2 Channels 1 and 0

2.2.2 Description of Reference Program Operation

Figure 5 illustrates the operation timing of the reference program.

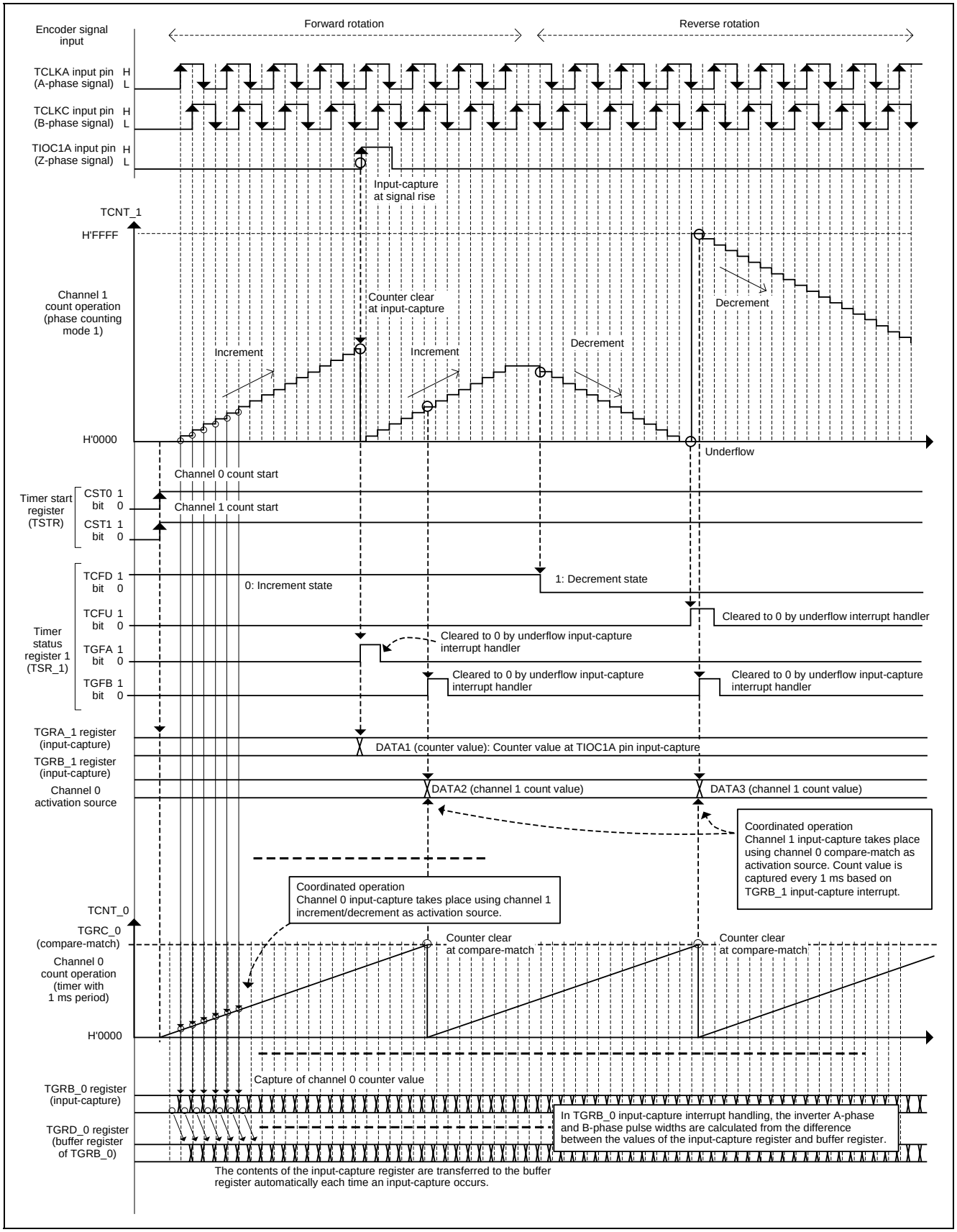


Figure 5 Two-Phase Encoder Signal Detection Operation

MTU2 channel 1 is set to phase counting mode 1, and pins TCLKA and TCLKB are connected to the A-phase and B-phase pulse signals from an external two-phase encoder. The TIOC1A pin is connected to the Z-phase signal from the two-phase encoder. The phase difference between the A-phase and B-phase pulse signals is detected and timer counter TCNT_1 is incremented or decremented. In addition, the TGRA_1 and TGRB_1 registers of channel 1 are set to the input-capture function.

- When the TIOC1A input pin rising edge signal is detected, the value of timer counter TCNT_1 is captured to the TGRA_1 register. At the same time, timer counter TCNT_1 is cleared. At this point, a TGRA input-capture interrupt is issued.
- The count value of timer counter TCNT_1 is captured to the TGRB_1 register once every 1 ms. At this point, a TGRB input-capture interrupt is issued. The input-capture activation source is a compare-match generated every 1 ms by channel 0. Two-phase encoder position information with a 1 ms period is obtained from the TGRB_1 register value.

MTU2 channel 0 is set to the compare-match function with the TGRC_0 register and is used as a 1 ms period timer. The TGRB_0 register of channel 0 is set to the input-capture function. In addition, the TGRD_0 and TGRB_0 registers are set as buffer registers.

- Timer counter TCNT_0 is cleared when a compare-match with the TGRC_0 register occurs. These compare-matches occur with a period of 1 ms and function as an input-capture (TGRB_1 register) activation source for channel 1.
- The TGRB_0 register is set to the input-capture function, and it captures the channel 0 counter value each time a 4× pulse is generated by the two-phase encoder. The input-capture activation source is the counter input clock of channel 1. A TGRB input-capture interrupt is generated at each channel 1 count.
- The TGRD_0 register is set to operate as a buffer for the TGRB_0 register. Each time a TGRB_0 register input-capture occurs, the value of the TGRB_0 register is transferred to the TGRD_0 register. The TGRB input-capture interrupt handler obtains the difference between the values of the TGRB_0 register and TGRD_0 register and calculates the 4× pulse width of the two-phase encoder.

2.3 Reference Program Configuration

2.3.1 Functions

Table 4 lists the principal functions used by the reference program.

Table 4 Functions

Function	Description
main()	Main function Makes initial settings functions for the various modules and starts multi-function timer pulse unit 2 (MTU2) timers.
stbcr_init()	Releases MTU2 from module standby.
mtu2_init()	MTU2 (channels 0 and 1) initial settings Sets channel 1 to phase counting mode 1. Sets channel 0 to 1 ms period timer operation.
pfc_init()	Pin function controller (PFC) initial settings Sets MTU2-related pins to timer pin function.
int_mtu2_tgia1()	MTU2 (channel 1) TGRA_1 input-capture interrupt handler Performs two-phase encoder Z-phase rising edge processing and captures the count value when the counter is cleared.
int_mtu2_tgib1()	MTU2 (channel 1) TGRB_1 input-capture interrupt handler When the interrupt is generated every 1 ms, the handler obtains the two-phase encoder position information (count value).
int_mtu2_tcfv1()	MTU2 (channel 1) counter overflow interrupt handler
int_mtu2_tcfu1()	MTU2 (channel 1) counter underflow interrupt handler
int_mtu2_tgib0()	MTU2 (channel 0) TGRB_0 input-capture interrupt handler Calculates the pulse interval of the two-phase encoder A-phase and B-phase.

2.3.2 Variables

Table 5 lists the variables used in the reference program.

Table 5 Variables

Variable Name	Description	Functions Used
TGRA1_data	MTU2 channel 1 TGRA register input-capture value. The value is the timer counter value at the rising edge of the two-phase encoder Z-phase.	int_mtu2_tgia1()
TGRB1_data_old	Stores the previous MTU2 channel 1 TGRB register input-capture value.	int_mtu2_tgib1()
TGRB1_data_diff	The difference between the MTU2 channel 1 TGRB register input-capture value and the previous input-capture value (TGRB1_data_old). This represents the increase in the count of the two-phase encoder over a 1 ms period.	int_mtu2_tgib1()
Under_over_flow_cnt	Overflow/underflow count of MTU2 channel 1 TCNT counter	int_mtu2_tcfv1() int_mtu2_tcfu1()
TGRD0_B0_data_diff	The edge interval between the A-phase and B-phase signals of the two-phase encoder. This value is the difference between the MTU2 channel 0 TGRB register (input-capture) value and the buffer register TGRD value (the previous value of the TGRB register).	int_mtu2_tgib0()

2.4 Function Setting Procedures

The processing sequences of the reference program are shown below.

2.4.1 Main Function

Figure 6 shows the processing sequence of the main function.

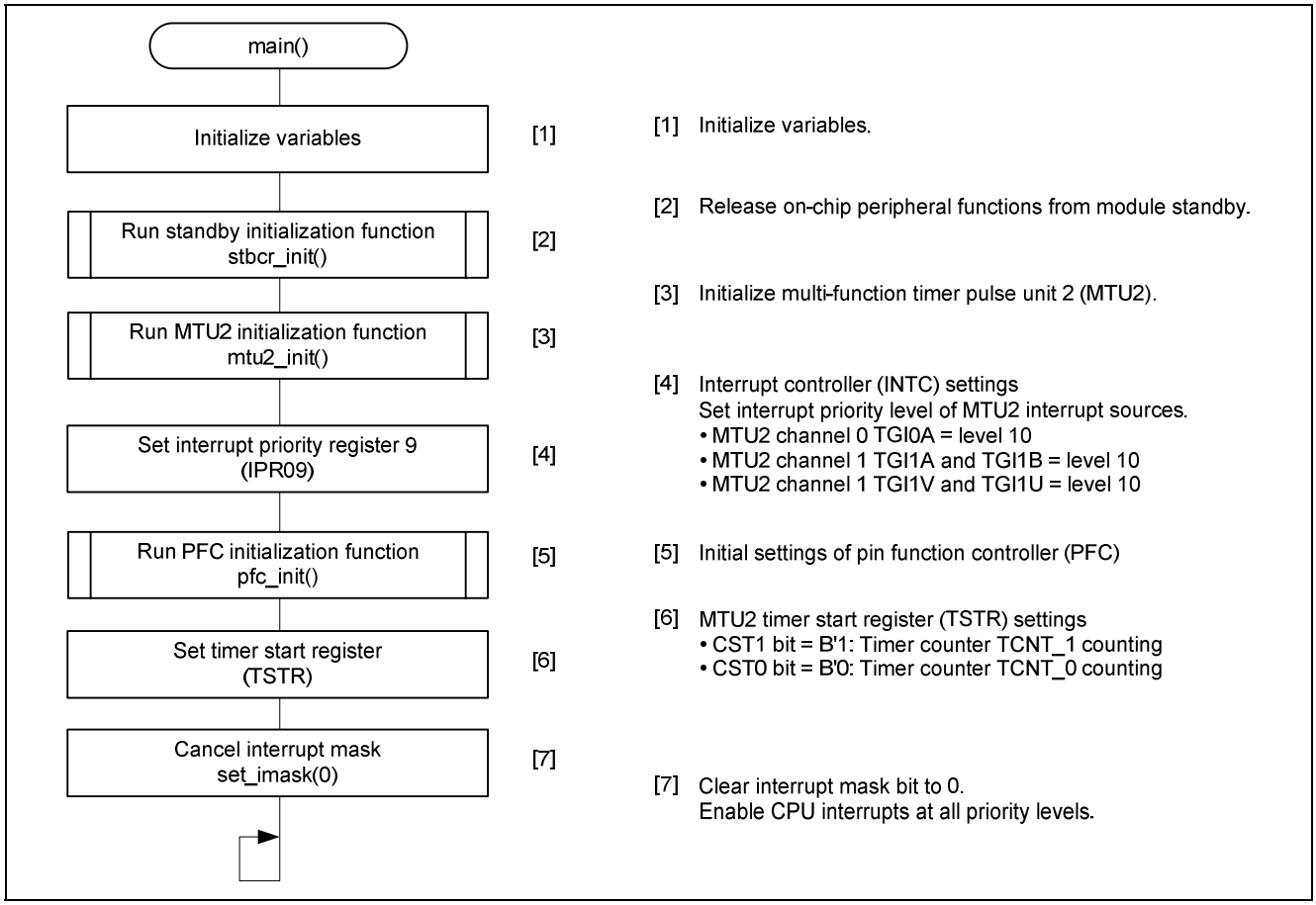


Figure 6 Processing of Main Function

2.4.2 Canceling Module Standby

Figure 7 shows the processing sequence for canceling module standby.

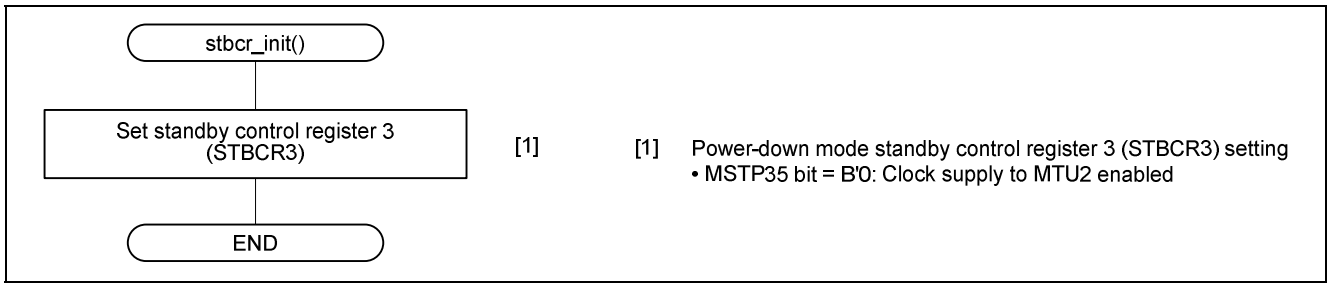
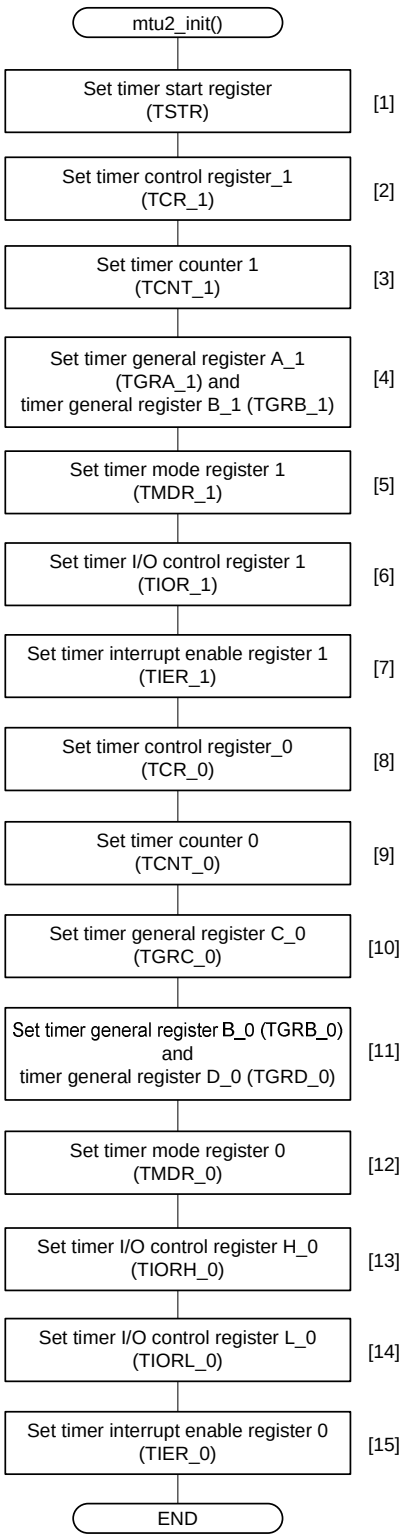


Figure 7 Canceling Module Standby

2.4.3 Multi-Function Timer Pulse Unit 2 (MTU2) Settings

Figure 8 shows the processing sequence for making initial settings for multi-function timer pulse unit 2 (MTU2).



[1] Stop count operation for MTU2 channels 0 to 4.

[2] Channel 1 timer counter clock and timer counter clearing source selection
- Bits CCLR[2:0] = B'000: TCNT clearing prohibited
- Bits CKEG[1:0] = B'00: TCNT counts at rising edge*
- Bits TPSC[2:0] = B'000: TCNT counts on internal clock Pϕ/1*

Note: * In phase counting mode, these bits are ignored and the phase counting mode settings take precedence. The external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the settings of bits TPSC2 to TPSC0 and CKEG1 and CKEG0 in TCR.

[3] Clear timer counter TCNT_1 to 0.

[4] Clear registers TGRA_1 and TGRB_1 to 0.
- Registers TGRA_1 and TGRB_1 operate as input-capture registers.

[5] Select the operating mode of channel 1.
- Bits MD3 to MD0 = B'0100: Phase counting mode 1 selected

[6] Operation settings of registers TGRA_1 and TGRB_1
- Bits IOB3 to IOB0 = B'1100: TGRB_1 is set as an input-capture register and executes input-capture at channel 0 TGRC_0 compare-match.
- Bits IOA3 to IOA0 = B'1000: TGRA_1 is set as an input-capture register and executes input-capture at rising edge of TIOC1A input pin.

[7] Channel 1 interrupt request enable/disable settings
- Bit TGIEU = B'1: Counter underflow interrupt request enabled
- Bit TGIEV = B'1: Counter overflow interrupt request enabled
- Bit TGIEB = B'1: Triggering of interrupt request (TGIB_1) by TGFB enabled
- Bit TGIEA = B'1: Triggering of interrupt request (TGIA_1) by TGFA enabled

[8] Channel 0 timer counter clock and timer counter clearing source selection
- Bits CCLR[2:0] = B'101: TCNT cleared at TGRC compare-match
- Bits CKEG[1:0] = B'00: TCNT counts at rising edge
- Bits TPSC[2:0] = B'000: TCNT counts on internal clock Pϕ/1

[9] Clear timer counter TCNT_0 to 0.

[10] Initial setting of TGRC_0 register
TGRC_0 is set as a compare-match register with a period of 1 ms (D'49999 at 50 MHz)

[11] Clear registers TGRB_0 and TGRD_0 to 0.
- TGRB_0 is used as an input-capture register.
- TGRD_1 is used as a buffer register.

[12] Set channel 0 operating mode.
- BFB = B'1: TGRD register is used as buffer register.
- Bits MD[3:0] = B'0000: Normal mode

[13] Operation settings of registers TGRA_0 and TGRB_0
- Bits IOB[3:0] = B'1100: TGRB_0 is set as an input-capture register and the capture input source is channel 1 count clock TCNT_1.
- Bits IOA[3:0] = B'0000 (initial setting): TGRA_0 is not used.

[14] Operation settings of registers TGRC_0 and TGRD_0
- Bits IOD[3:0] = B'0000 (initial setting): TGRD_0 is set as a buffer register.
- Bits IOC[3:0] = B'0000: TGRC_0 is set as an output-compare register.

[15] Channel 0 interrupt request enable/disable settings
- Bit TGIEB = B'1: Triggering of interrupt request (TGIB_1) by TGFB enabled

Figure 8 Initial Settings of Multi-Function Timer Pulse Unit 2 (MTU2)

2.4.4 Pin Function Controller (PFC) Settings

Figure 9 shows the processing sequence for making pin function controller (PFC) settings.

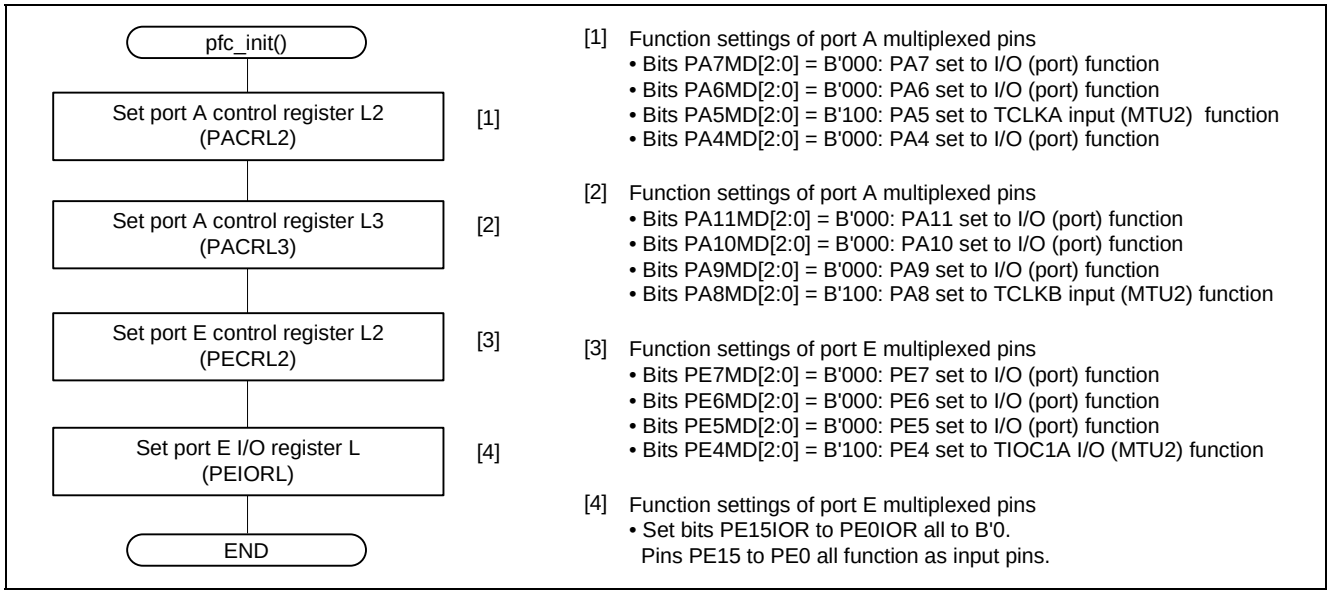


Figure 9 Pin Function Controller (PFC) Settings

2.4.5 Channel 1 Input-Capture (TGRA_1) Interrupt

Figure 10 shows the processing sequence of the MTU2 channel 1 input-capture interrupt (TRRA_1) handler. The interrupt is generated at the rising edge of the Z-phase signal from the two-phase encoder.

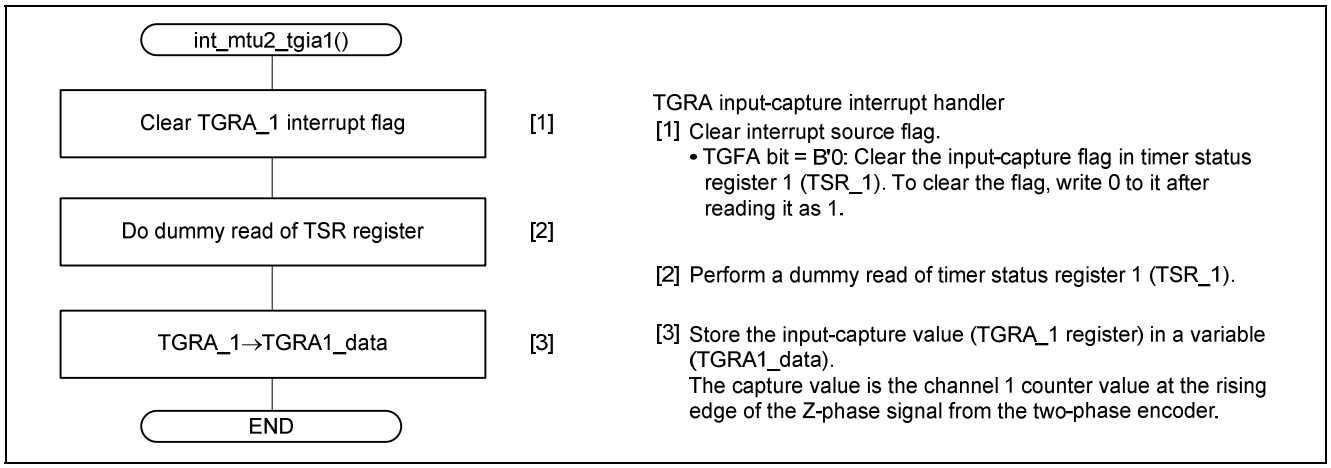


Figure 10 MTU2 Channel 1 Input-Capture (TGRA_1) Interrupt Handler

2.4.6 MTU2 Channel 1 Input-Capture (TGRB_1) Interrupt

Figure 11 shows the processing sequence of the MTU2 channel 1 input-capture interrupt (TRRB_1) handler. The interrupt is generated every 1 ms.

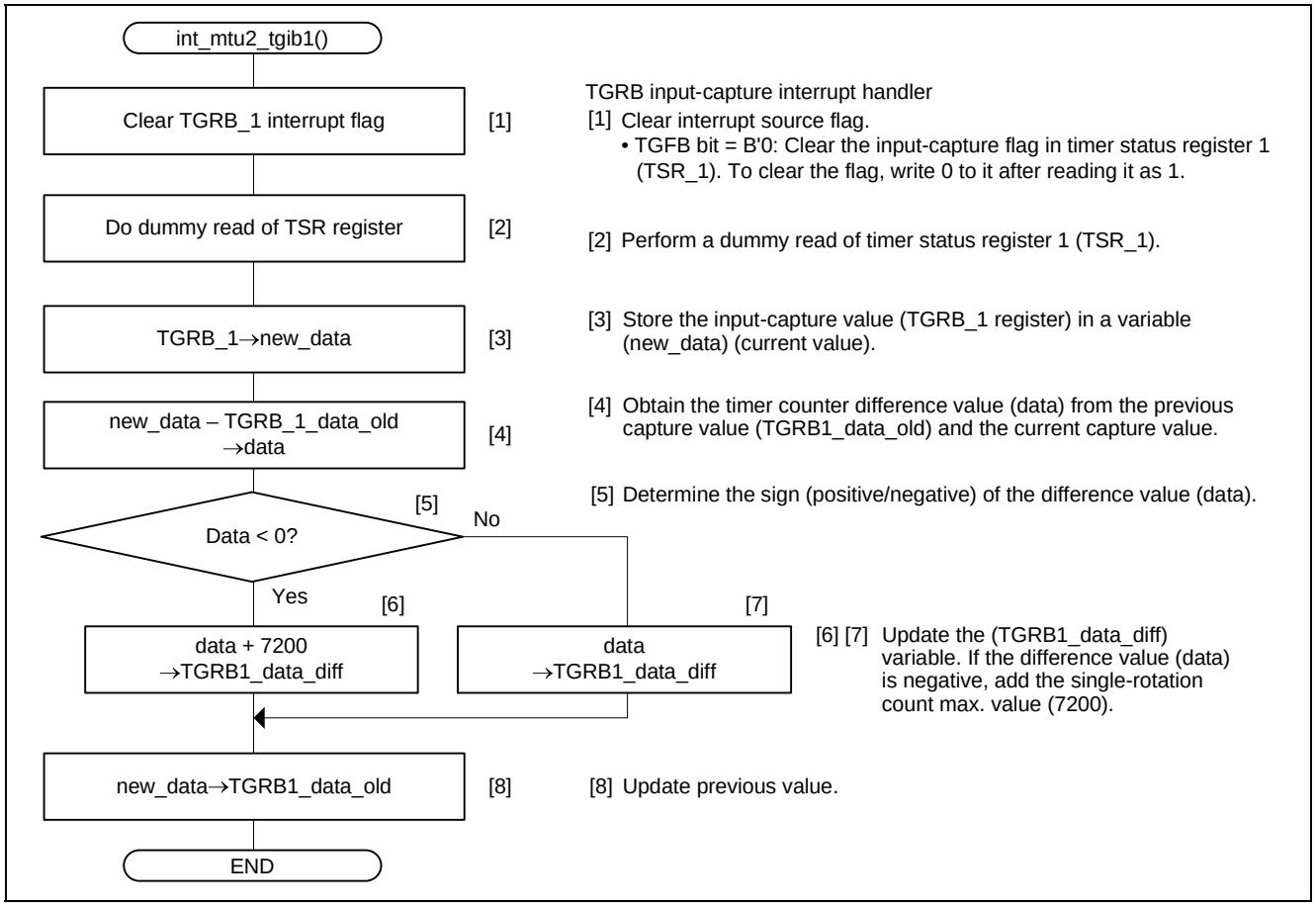


Figure 11 MTU2 Channel 1 Input-Capture (TGRB_1) Interrupt Handler

2.4.7 MTU2 Channel 1 Overflow Interrupt

Figure 12 shows the processing sequence of the MTU2 channel 1 overflow interrupt handler.

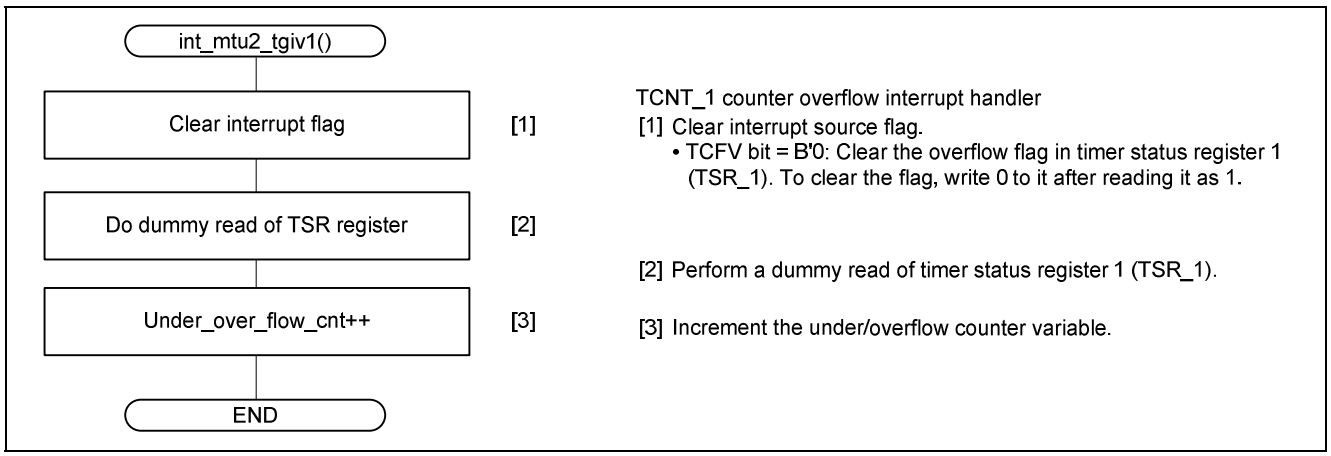


Figure 12 MTU2 Channel 1 Overflow Interrupt Handler

2.4.8 MTU2 Channel 1 Underflow Interrupt

Figure 13 shows the processing sequence of the MTU2 channel 1 underflow interrupt handler.

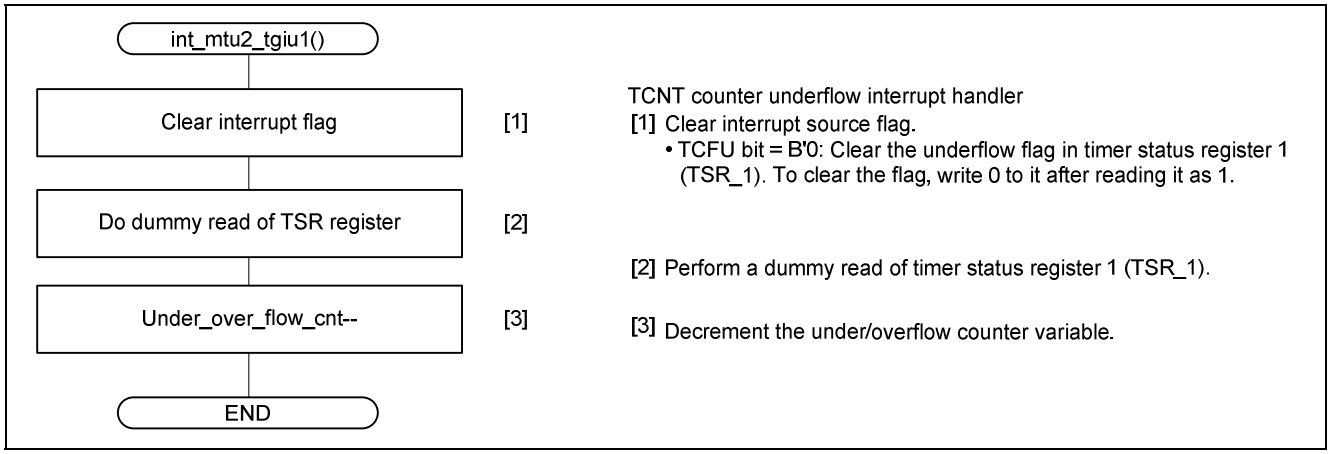


Figure 13 MTU2 Channel 1 Underflow Interrupt Handler

2.4.9 MTU2 Channel 0 Input-Capture (TGRB_0) Interrupt

Figure 14 shows the processing sequence of the MTU2 channel 0 input-capture (TGRB_0) interrupt handler. The interrupt is generated every channel 1 count cycle. It is used to calculate the edge interval between the two-phase encoder A-phase and B-phase signals.

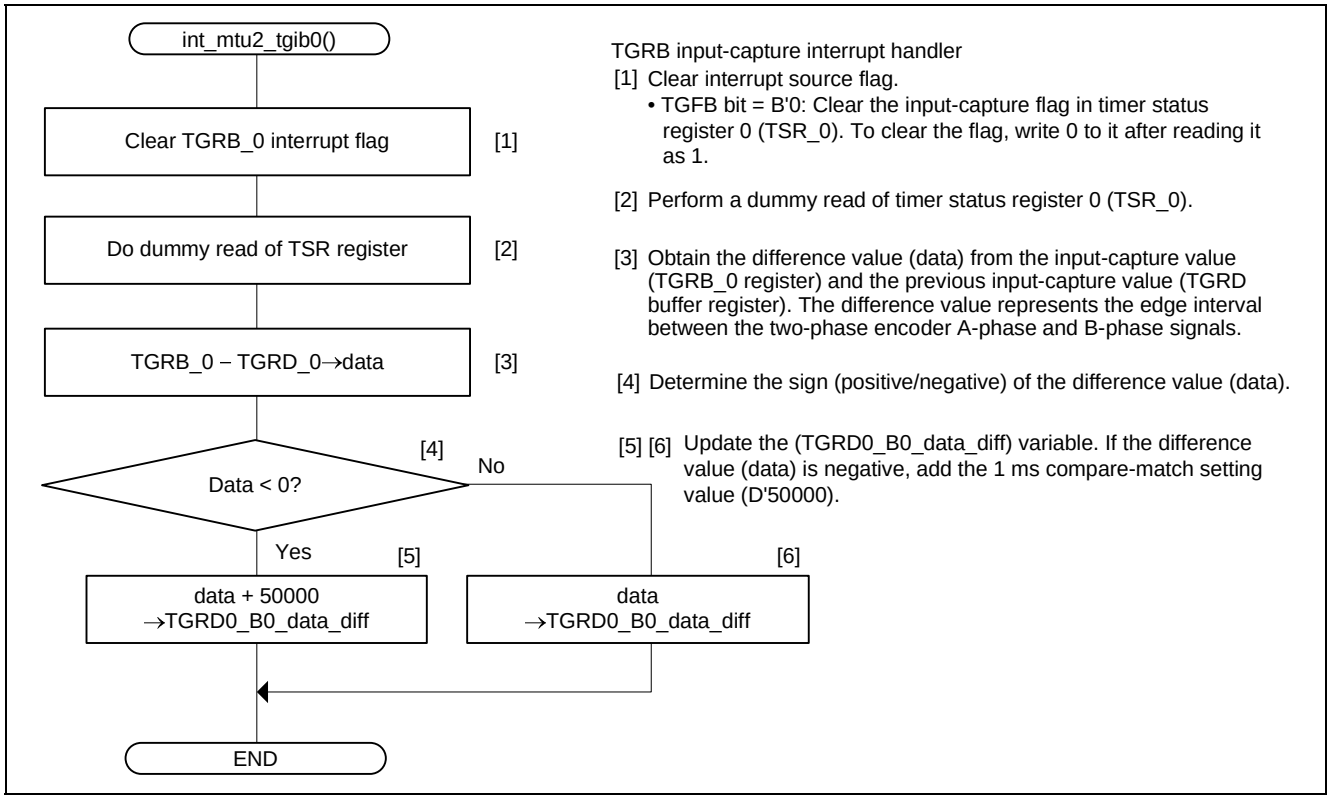


Figure 14 MTU2 Channel 0 Input-Capture (TGRB_0) Interrupt Handler

2.5 Reference Program Register Settings

The register setting values used in the reference program are described below.

2.5.1 Clock Pulse Generator (CPG)

Table 6 lists the register settings of the clock pulse generator.

Table 6 Clock Pulse Generator (CPG)

Register	Address	Setting Value	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0303	Specifies operation frequency division ratios. • STC[2:0] = B'011: Bus clock (Bϕ) division ratio: ×1/4 • IFC[2:0] = B'000: Internal clock (Iϕ) division ratio: ×1 • PFC[2:0] = B'011: Peripheral clock (Pϕ) division ratio: ×1/4

2.5.2 Power-Down Modes

Table 7 lists the register settings related to the power-down modes.

Table 7 Power-Down Modes

Register	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFE 0408	H'5E	Controls the operation of individual modules in power-down modes • HIZ = B'0: Pin states maintained in software standby • MSTP36 = B'1: Clock supply to MTU2S stopped • MSTP35 = B'0: MTU2 operating • MSTP34 = B'1: Clock supply to POE2 stopped • MSTP33 = B'1: Clock supply to IIC3 stopped • MSTP32 = B'1: Clock supply to ADC0 stopped • MSTP30 = B'0: Flash memory operating

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 8 lists the register settings of multi-function timer pulse unit 2 (MTU2).

Table 8 Multi-Function Timer Pulse Unit 2 (MTU2)

Register	Address	Setting Value	Description
Timer control register 1 (TCR_1)	H'FFFE 4380	H'20	Channel 1 TCNT control settings • CCLR[2:0] = B'001: TCNT cleared at TGRA input-capture • CKEG[1:0] = B'00: TCNT counts at rising edge • TPSC[2:0] = B'000: TCNT counts on internal clock Pϕ/1 Note: In phase counting mode, bits TPSC2 to TPSC0 and CKEG1 and CKEG0 are ignored and the phase counting mode settings take precedence. The external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of their settings.
Timer counter 1 (TCNT_1)	H'FFFE 4386	H'0000	16-bit counter Clear to 0.
Timer general register A_1 (TGRA_1)	H'FFFE 4388	H'0000	Used as input-capture register. Clear to 0.
Timer general register B_1 (TGRB_1)	H'FFFE 438A	H'0000	Used as input-capture register. Clear to 0.
Timer mode register 1 (TMDR_1)	H'FFFE 4381	H'04	Sets the operating mode. • MD3 to MD0 = B'0100: Phase counting mode 1
Timer I/O control register 1 (TIOR_1)	H'FFFE 4382	H'C8	TGR register operation settings • IOB[3:0] = B'1100: TGRB_1 register performs input-capture at channel 0 TGRC_0 compare-match. • IOA[3:0] = B'1000: TGRA_1 register performs input-capture at rising edge.
Timer interrupt enable register 1 (TIER_1)	H'FFFE 4384	H'33	Controls interrupt request enable/disable. • TTGE = B'0: Generation of A/D converter start request disabled • TCIEU = B'1: Triggering of underflow interrupt request (TCIU) by TCFU enabled • TCIEV = B'1: Triggering of overflow interrupt request (TCIV) by TCFV enabled • TGIEB = B'1: Triggering of interrupt request (TGIB) by TGFB enabled • TGIEA = B'1: Triggering of interrupt request (TGIA) by TGFA enabled

Register	Address	Setting Value	Description
Timer control register 0 (TCR_0)	H'FFFE 4300	H'A0	Channel 0 TCNT control settings • CCLR[2:0] = B'101: TCNT cleared at TGRC compare-match • CKEG[1:0] = B'00: TCNT counts at rising edge • TPSC[2:0] = B'000: TCNT counts on internal clock Pϕ
Timer counter 0 (TCNT_0)	H'FFFE 4306	H'0000	16-bit counter Clear to 0.
Timer general register A_0 (TGRA_0)	H'FFFE 4308	—	Not used in this application example.
Timer general register B_0 (TGRB_0)	H'FFFE 430A	H'0000	Used as input-capture register. Clear to 0.
Timer general register C_0 (TGRC_0)	H'FFFE 430C	D'49999	Used as compare-match register. Set the compare-match period to 1 ms. (1 ms / 20 ns [at 50 MHz]) – 1 = D'50000 – 1 = D'49999
Timer general register D_0 (TGRD_0)	H'FFFE 430E	H'0000	Used as buffer register for TGRB_0. Clear to 0.
Timer mode register 0 (TMDR_0)	H'FFFE 4301	H'20	Sets the operating mode. • BFE = B'0: TGRE_0 and TGRF_0 normal operation • BFB = B'1: TGRB and TGRD buffer operation • BFA = B'0: TGRA and TGRC normal operation • MD3 to MD0 = B'0000: Operating mode is normal operation.
Timer I/O control register H_0 (TIORH_0)	H'FFFE 4302	H'C0	TGR register operation settings • IOB[3:0] = B'1100: TGRB_1 is set as input-capture register. Capture input source is channel 1 count clock, and TCNT_1 increments/decrements at input-capture. • IOA[3:0] = B'0000: TGRA_0 is set as output-compare register.
Timer I/O control register L_0 (TIORL_0)	H'FFFE 4303	H'00	TGR register operation settings • IOD[3:0] = B'0000: TGRD_0 is set as output-compare register. • IOC[3:0] = B'0000: TGRC_0 is set as output-compare register.

Register	Address	Setting Value	Description
Timer interrupt enable register 0 (TIER_0)	H'FFFE 4304	H'02	Controls interrupt request enable/disable. • TTGE = B'0: Generation of A/D converter start request disabled • TCIEV = B'0: Triggering of overflow interrupt request (TCIV) by TCFV bit disabled • TGIED = B'0: Triggering of interrupt request (TGID) by TGFD disabled • TGIEC = B'0: Triggering of interrupt request (TGIC) by TGFC disabled • TGIEB = B'1: Triggering of interrupt request (TGIB) by TGFB enabled • TGIEA = B'0: Triggering of interrupt request (TGIA) by TGFA disabled
Timer start register (TSTR)	H'FFFE 4280	H'03	TCNT operate/stop selection for channels 0 to 4 • CST1 = B'1: TCNT_1 count operation • CST0 = B'1: TCNT_0 count operation

2.5.4 Interrupt Controller (INTC)

Table 9 lists the register settings of the interrupt controller (INTC).

Table 9 Interrupt Controller (INTC)

Register	Address	Setting Value	Description
Interrupt priority register 9 (IPR09)	H'FFFE 0C06	H'A0AA	Interrupt priority (level 0 to 15) setting • Bits 15 to 12 = B'1010: MTU0 (TGI0A to TGI0D) interrupt level = 10 • Bits 11 to 8 = B'0000: MTU0 (TCI0V, TGI0E, and TGI0F) interrupt level = 0 • Bits 7 to 4 = B'1010: MTU1 (TGI1A and TGI1B) interrupt level = 10 • Bits 3 to 0 = B'1010: MTU1 (TCI1V and TGI1U) interrupt level = 10

2.5.5 Pin Function Controller (PFC)

Table 10 lists the register settings of the pin function controller (PFC).

Table 10 Pin Function Controller (PFC)

Register	Address	Setting Value	Description
Port A control register L2 (PACRL2)	H'FFFE 3814	H'0040	Port A multiplex pin function settings The initial setting values are as follows. • PA7MD[2:0] = B'000: PA7 functions as PA7 I/O (Port). • PA6MD[2:0] = B'000: PA6 functions as PA6 I/O (Port). • PA5MD[2:0] = B'100: PA5 functions as TCLKA input (MTU2). • PA4MD[2:0] = B'000: PA4 functions as PA4 I/O (Port).
Port A control register L3 (PACRL3)	H'FFFE 3812	H'0004	Port A multiplex pin function settings The initial setting values are as follows. • PA11MD[2:0] = B'000: PA11 functions as PA11 I/O (Port). • PA10MD[2:0] = B'000: PA10 functions as PA10 I/O (Port). • PA9MD[2:0] = B'000: PA9 functions as PA9 I/O (Port). • PA8MD[2:0] = B'100: PA8 functions as TCLKB input (MTU2).
Port E control register L2 (PECRL2)	H'FFFE 3A14	H'0004	Port E multiplex pin function settings The initial setting values are as follows. • PE7MD[2:0] = B'000: PE7 functions as PE7 I/O (Port). • PE6MD[2:0] = B'000: PE6 functions as PE6 I/O (Port). • PE5MD[2:0] = B'000: PE5 functions as PE5 I/O (Port). • PE4MD[2:0] = B'100: PE4 functions as TIOC1A I/O (MTU2).
Port E I/O register L (PEIORL)	H'FFFE 3A06	H'0000	Port E pin I/O direction settings • PE15IOR to PE0IOR all set to B'0: PE15 to PE0 all function as input pins.

3. Documents for Reference

- Hardware Manual
  SH7216 Group Hardware Manual [REJ09B0543]
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Software Manual
  SH-2A/SH2A-FPU Software Manual [REJ09B0051]
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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