SH7216 Group

Hardware Design Guide

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Summary

This application note contains tips on designing a system using the SH7216. As a technical reference it will help the designer avoid common mistakes and get their product up and running when doing their first SH2A design.

Target Device

SH7216 MCU

Contents

1. Power Supplies 2
2. Reset 4
3. Oscillator 7
4. MCU Operating Modes 9
5. Handling of Pins 12
6. On-Chip Resource Access 20
7. Endianness 20
8. Power-down Modes 21
9. RCAN-ET External Circuit Example 26
10. Ethernet PHY-LSI Interface 27
11. References 31

1. Power Supplies

1.1 Power Supplies

The SH7216 has digital power supplies and analog power supplies, and includes the following pins.

Table 1 Digital Power Supplies

Symbol	Name	Description
V_{CL}	Internal step-down power supply	External capacitance pins for internal step-down power supply
$V_{cc}Q$	Power supply	Power supply pins 3.0 to 3.6 V
$PLLV_{CC}$	PLL power supply	Power supply for the on-chip PLL oscillator
DrV_{CC}	USB power supply	Power supply pin for the internal USB transceiver. Apply the same electric potential as the $V_{CC}Q$
V_{SS}	Ground	Ground pins 0 V
$PLLV_{SS}$	Ground for PLL	Ground pins for the on-chip PLL oscillator 0 V
DrV_{SS}	USB Ground	Ground pin for the internal USB transceiver 0 V

Note: Digital power supply voltage is between 3.0 V and 3.6 V. $PLLV_{CC}$, and DrV_{CC} must be at the same electric potential as the $V_{CC}Q$. When not using the USB module, DrV_{CC} must be at the same electric potential as the $V_{CC}Q$.

Table 2 Analog Power Supplies

Symbol	Name	Description
AV_{CC}	Analog power supply	Power supply pin for the A/D converter 4.5 to 5.5 V
AV_{SS}	Analog ground	Ground pin for the A/D converter 0 V
AVREF	Analog reference power supply	Reference voltage pin for the A/D converter 4.5 V to AVcc
$AVREFV_{SS}$	Analog reference ground	Reference ground pin for the A/D converter Apply the same electric potential as the AV_{SS}

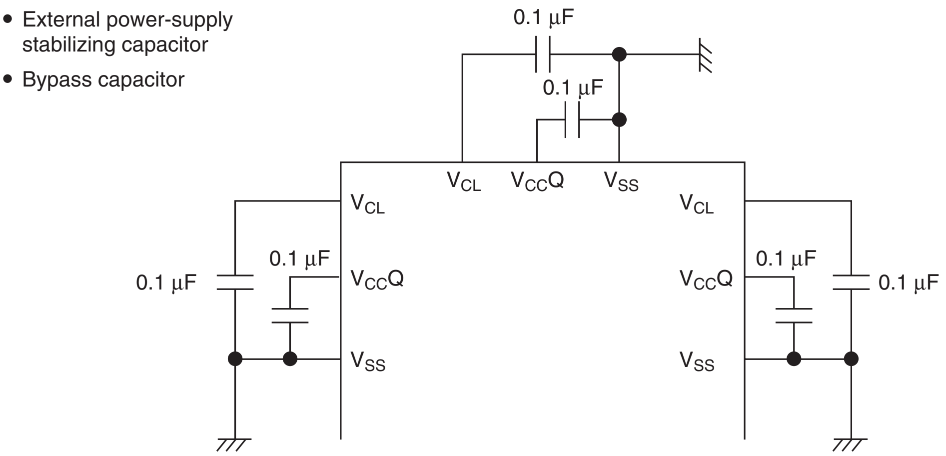
Note: Analog power supply voltage is between 4.5 V and 5.5 V. When not using the A/D converter, connect AVCC and AVREF to VCCQ, AVSS and AVREFvss to VSS, respectively.

1.2 Notes on Connecting Capacitors

The SH7216 includes an internal step-down circuit to automatically reduce the internal power supply voltage to an appropriate level. The internal supply is brought out to V_{CL} pins to allow for the connection of capacitors between the V_{CL} and V_{SS} pins to stabilize the internal voltage. Place a capacitor as close as possible between the V_{CL} pin and V_{SS}. Using a 0.01 µF multi-layer ceramic capacitor is recommended. *Do not apply any external power supply voltage to the internal stepped-down power supply (V_{CL}) pins.*

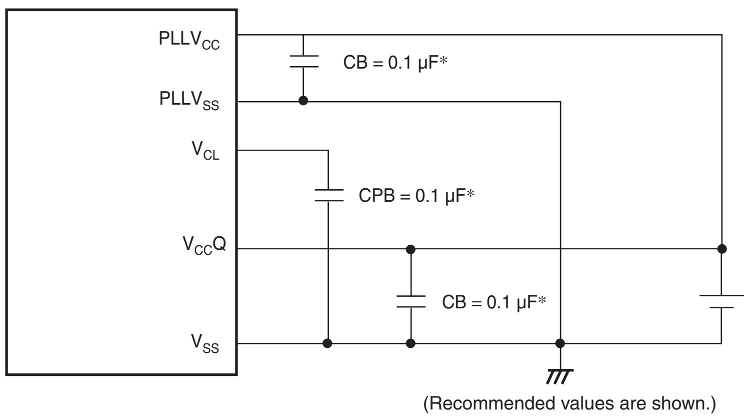
A multilayer ceramic capacitor must be installed as a bypass capacitor for each pair of power supply pins (V_{CC}Q and V_{SS} pair as well as PLLV_{CC} and PLLV_{SS} pair). Install the bypass capacitor as close as possible to the LSI power supply pins. Connect the bypass capacitor with capacitance between 0.02 and 0.33 µF, after evaluating the constant in the system.

Figure 1 shows the connection of the external capacitor. Figure 2 shows the recommended external circuit around PLL.



Note: Do not apply any power supply voltage to the VCL pin.
Use multilayer ceramic capacitors (one capacitor for each VCL pin and VCCQ pin), which should be located near the pin.
The above capacitance is a recommended value.

Figure 1 Capacitor Connection to V_{CC}Q and V_{CL}



Note: * CB and CPB are laminated ceramic capacitors.

Figure 2 Recommended External Circuit around PLL

2. Reset

2.1 Power-On/Power-Off Sequence

Turn on or off the digital power supply ($V_{CC}Q$, $PLLV_{CC}$, DrV_{CC}) and the analog power supply (AV_{CC}, AVREF) as closely together as possible.

The SH7216 enters an undefined state from when the power is turned on until the digital power supply exceeds the minimum operating voltage (3.0 V), or from when the digital power supply falls below the minimum operating voltage (3.0 V) to the voltage falls to 0 V. Figure 3 shows the power-on/power-off sequence.

Since the output pin and I/O pin states and LSI internal states are undefined during this “power-on” period, design the power supply circuit to keep that period as short as possible. In general, good power supply design will provide a smooth short rise time which will be fine. A small switcher or LDO regulator “slaved” off the 5 VDC will usually provide the proper timing on the 3.3 VDC. Complex power sequencers are normally not required.

Also, design the system so that the undefined state during the power-on/power-off states do not cause an overall malfunction failure of the system (i.e. passive pull-ups or pull-downs may be required based on your system design). An example of this might be resistors to pull the signals driving any power circuits, such as motor drive inverter, to the inactive state.

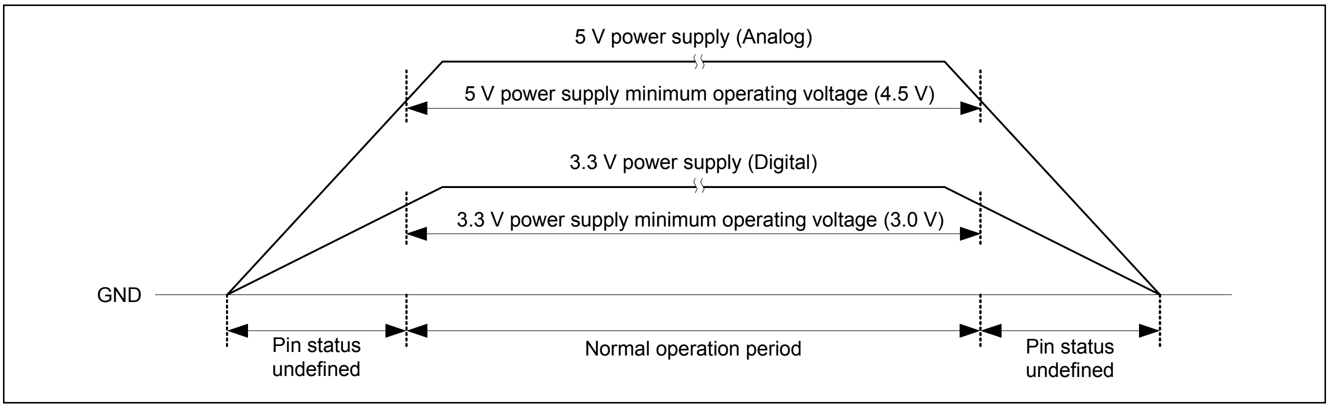


Figure 3 Power-on/Power-off Sequence

2.2 Oscillation Settling Time

When the $\overline{RES}$ pin is driven low, the SH7216 enters the power-on reset state. To make sure to reset the SH7216, the $\overline{RES}$ pin must be kept at the low level during the oscillation settling time at power-on or when exiting from software standby mode (when the clock is halted). Keep the $\overline{RES}$ pin at low level for at least 20 tcyc when setting the $\overline{RES}$ pin to low level while the clock is running.

The power-on oscillation settling time (t_{OSC1}) is 10 ms, which is specified from when the $V_{CC}Q$ exceeds the minimum operating voltage until the $\overline{RES}$ pin exceeds the V_{IH} voltage. Figure 4 shows the relation between power-on/off and clock, reset signals. This timing is easily accommodated by many "supervisor" ICs available on the market such as Renesas M51957BFP.

In the power-on reset state, the internal state of the CPU and all the on-chip peripheral registers are initialized.

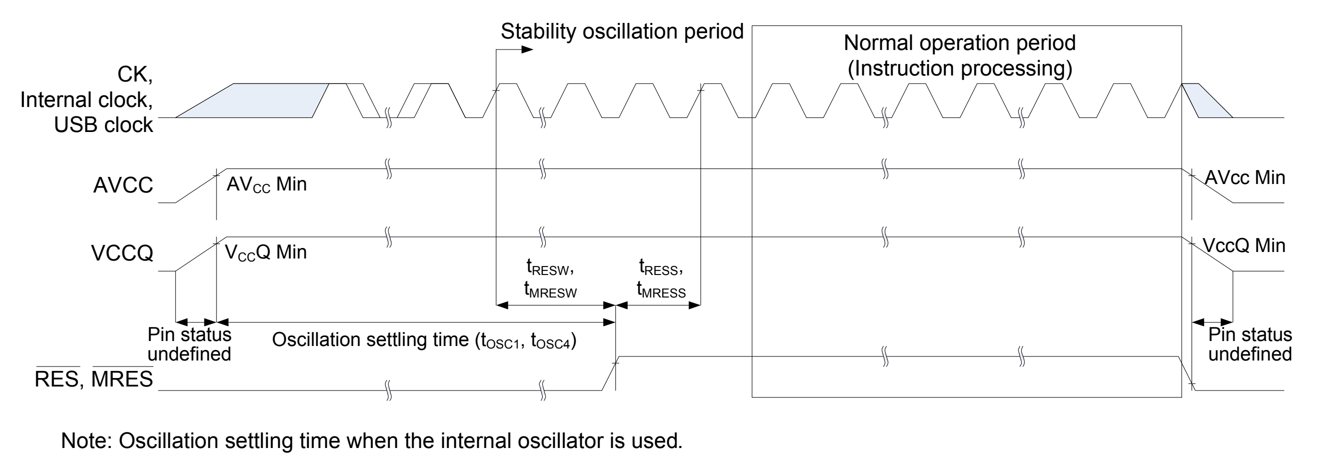


Figure 4 Relations between Power-on/off and Clock, Reset Signals

2.3 Manual Reset

The SH7216 has two reset options; power-on reset and manual reset.

When the $\overline{\text{RES}}$ pin is high and the $\overline{\text{MRES}}$ pin is driven low, the SH7216 enters the manual reset state. In order to ensure a valid manual reset the MCU, the $\overline{\text{MRES}}$ pin must be kept at the low level for at least 20 tcyc. The CPU's internal state is initialized in during manual reset state, but unlike the power-on reset, on-chip peripheral registers are not initialized other than the BN bit in the IBNR register of INTC.

In manual reset state, manual reset exception handling starts when the $\overline{\text{MRES}}$ pin is first driven low for a fixed period and then returns to high. The processing of the manual reset exception handling is same as that of the power-on reset, however, note that the exception handling vector table address to retrieve the PC and SP default value is different.

The state of pins when the manual reset is different from those of power-on reset. Input-dedicated pins are set as input, and output-dedicated pins are set as output. Multiplex pins are set as input or output, which is specified by the PFC before reset manually.

You are not required to use the manual reset ($\overline{\text{MRES}}$) pin. If you do not use it, it should be terminated properly. A common uses of the manual reset pin is a "quick restart" of the Application code (i.e. initial CPU and minimal setup code required).

2.4 Reset by WDT

When setting WDT as watchdog timer mode, and specifying the power-on reset when the WTCNT overflows, the SH7216 enters the power-on reset state when the WTCNT overflows.

When power-on reset exception processing is started by the WDT, the CPU operates as same as when the power-on reset is caused by the $\overline{\text{RES}}$ pin, however, the WRCSR register of the WDT and FRQCR register of the CPG are not initialized by the reset signal generated by the WDT. To change the power-on reset processing by $\overline{\text{RES}}$ pin and the WDT overflow, the reset factor is judged by the WOVF bit in the WRCSR register.

When the SH7216 is reset by the $\overline{\text{RES}}$ pin or the H-UDI reset assert command, and by WDT overflow at the same time, the reset by the $\overline{\text{RES}}$ pin or the H-UDI reset assert command is prior to the WDT overflow, and the WOVF bit in the WRCSR register is cleared to 0.

When setting WDT as watchdog timer mode, and specifying the manual reset when the WTCNT overflows, the SH7216 enters the manual reset state. When manual reset exception processing is started by the WDT, the CPU operates in the same way as when a manual reset was caused by the $\overline{\text{MRES}}$ pin.

When the SH7216 is reset manually (manual reset), the bus cycle is retained. When the MCU is reset manually while the bus is released or during the DMAC burst transfer, the manual reset exception handling will be held until the CPU acquires the bus. However, if the interval from when the MCU is reset manually until the end of the bus cycle is equal to or longer than 128 Pφ of the internal manual reset interval cycles, the internal manual reset source is not held but ignored. The manual reset exception handling is not executed.

If the WDTOVF signal is input to the $\overline{\text{RES}}$ pin, the SH7216 cannot be initialized correctly. Do not input the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ pin through logic circuits. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in Figure 5.

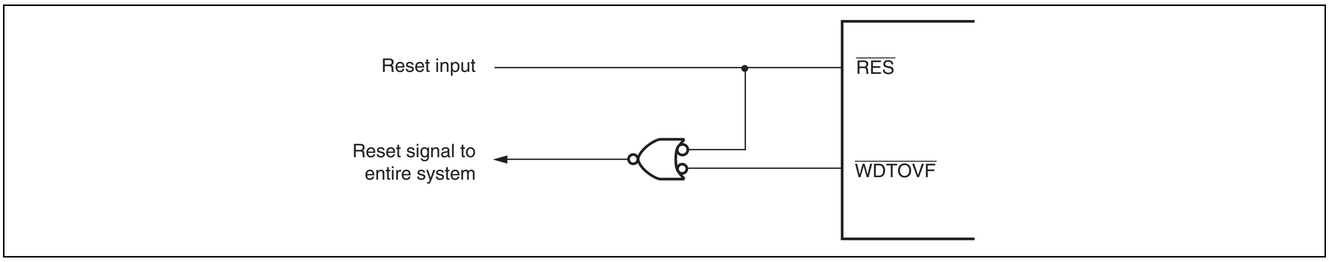


Figure 5 Example of System Reset Circuit Using WDTOVF Signal

3. Oscillator

3.1 Connecting a Crystal Resonator

Figure 6 shows the connection example of a crystal resonator as the SH7216 operation clock. Use the 0 Ω damping resistor (R_d). Use a crystal resonator with frequency between 10 and 12.5 MHz.

As the characteristics of the oscillation circuit depend on the oscillator, built-in PLL and board characteristics, it is recommended to consult the crystal resonator manufacturer on the constants of C_{L1} and C_{L2}.

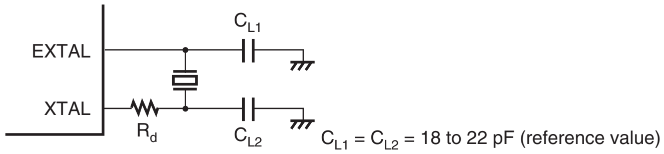
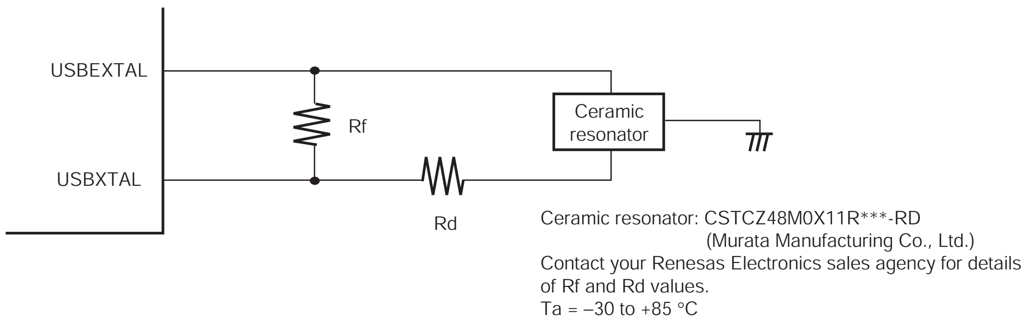


Figure 6 Example of Crystal Resonator Connection

3.2 USB Operating Clock

Figure 7 shows a connection example of a ceramic resonator as the USB operating clock. Install the 48 MHz resonator to USBEXTAL and USBXTAL to use these signals as the USB clocks.



Note: *** represents a three-digit alphanumeric which express " Individual Specification". Since the frequency for USB requires high accuracy, the official product name will be decided to match the frequency after evaluation of oscillation on the board that is actually to be used. Please contact your Renesas Electronics sales agency.

Figure 7 Example of Connecting a Ceramic Resonator

It is possible to run the CPU and the USB module from the same clock source possibly reducing EMI sources and cost. When using the system clock as the USB clock, connect the USBEXTAL as low level, leave the USBXTAL as open, and connect 12 MHz resonator with EXTAL and XTAL as shown in the right side of Figure 8.

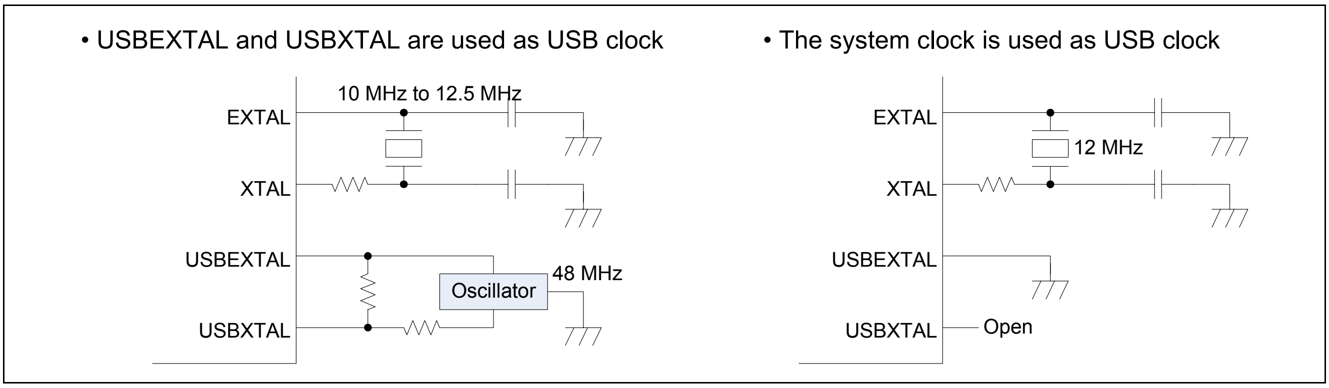


Figure 8 Selecting the USB operating clock, Resonator Connection and Frequency

3.3 Selecting the USB Boot Mode Clock

The SH7216 supports USB boot mode to program the FLASH memory from the externally-connected host via the USB. The internal clock hardware must select the proper clock for the USB Boot mode software to operate properly. This is done using Port B bit 14 (PB14).

When using USBEXTAL and USBXTAL as USB clock, set the PB14 to low level. When using the system clock as USB clock, set the PB14 to high level.

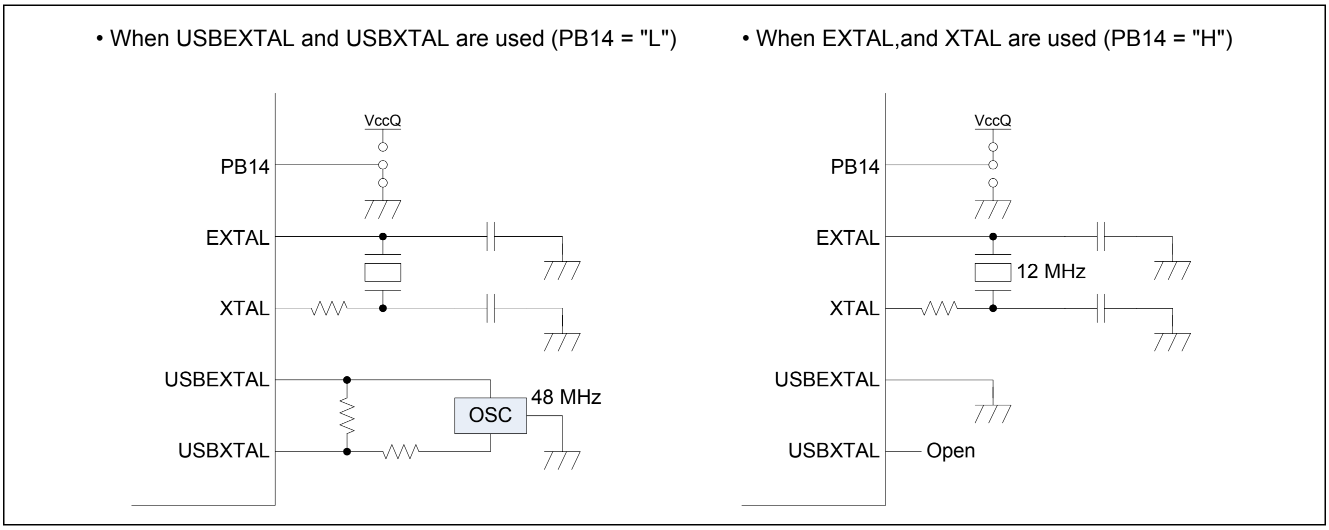


Figure 9 USB supply clock and PB14 setting in USB Boot Mode

4. MCU Operating Modes

4.1 Mode Pin Setting

The SH7216 has four MCU operating modes and three on-chip flash memory programming modes. The operating mode is determined by setting combination of FWE, MD1, and MD0 pins.

Table 3 shows the setting combinations; do not set these pins other than the combinations shown in the table below.

The MCU operating mode can be selected from MCU extension modes 0 to 2 and single chip mode. As the on-chip flash memory programming mode, boot mode, user boot mode, and user program mode are available.

NOTE: Mode pins MD0 and MD1 are only sampled during reset and the set-up time to reset rising must be met. FWE may be toggled during operation, for example by a "jumper pin" pin to transition from Mode 2 to Mode 6. FWE is typically used by high reliability applications to ensure only valid updates are allowed. See section 4.2.4 User Program Mode for details.

Table 3 Selection of Operating Modes

Mode Number	Pin Setting			Mode Name	Internal ROM	CS0 Space Bus Width
	FWE	MD1	MD0			
Mode 0	0	0	0	MCU extension mode 0	Not active	32-bit
Mode 1	0	0	1	MCU extension mode 1	Not active	16-bit
Mode 2	0	1	0	MCU extension mode 2	Active	Set by the CS0BCR of BSC
Mode 3	0	1	1	Single chip mode	Active	—
Mode 4 (1)	1	0	0	Boot mode	Active	Set by the CS0BCR of BSC
Mode 5 (1)	1	0	1	User boot mode	Active	Set by the CS0BCR of BSC
Mode 6 (1)	1	1	0	User program mode	Active	Set by the CS0BCR of BSC
Mode 7 (1) (2)	1	1	1	USB boot mode	Active	—
Mode 7 (1) (3)	1	1	1	User program mode	Active	—

Notes 1. Programming mode for the flash memory.
2. This mode can be used when the FWE bit is set and kept as 1 after the MCU is turned ON.
3. If FWE bit is set as 0 when waking the MCU up from power-on reset, then the FWE bit is set as 1 after the MCU operating mode is set as the single chip mode, the MCU transitions to the user program mode in a single chip state.

4.2 Flash Memory Programming Modes

4.2.1 Boot Mode

The boot mode allows the engineer the ability to program or erase the user MAT and user boot MAT by transmitting control commands and programming data from the host. The on-chip SCI is used in asynchronous mode for communications between the host and the SH7216. The host must have tool to transmit control commands and program data.

When activating the SH7216 in boot mode, the program in the embedded program stored MAT is executed. This program automatically adjusts the SCI bit rate and establishes the communication by control commands between the host and the SH7216.

Figure 10 shows the system configuration in boot mode. The NMI and IRQ7 to IRQ0 interrupts are ignored in this mode, but these pins must be fixed to non-active state. Note that the AUD cannot be used in this mode.

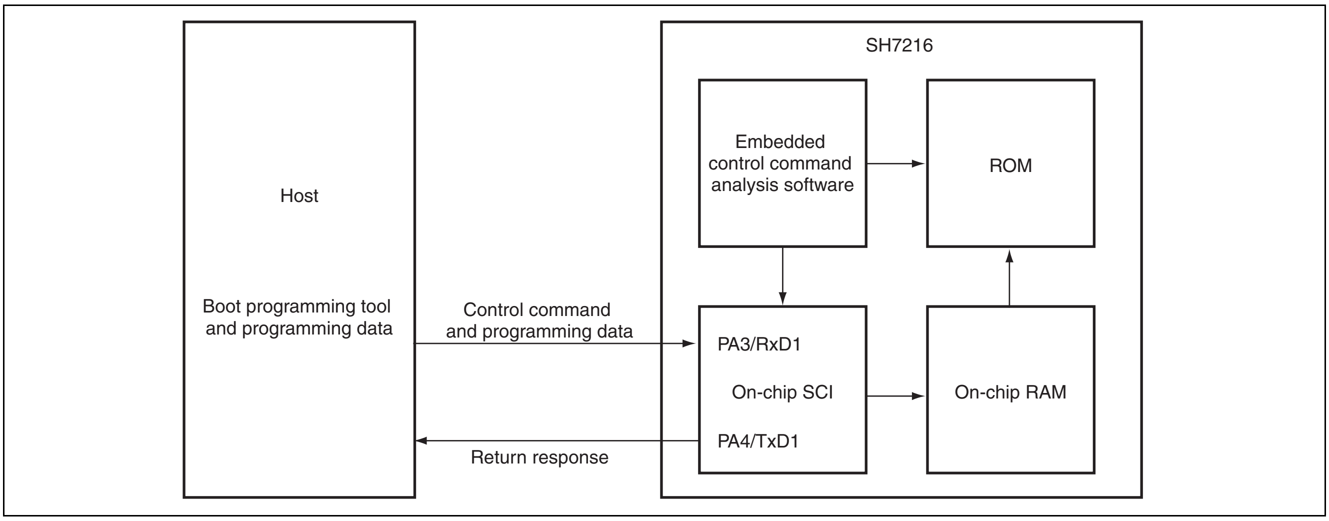


Figure 10 System Configuration in Boot Mode

4.2.2 User Boot Mode

User boot mode allows the designer to provide a "custom" boot loader for his equipment. The source of the data is irrelevant to the MCU, provided the "communication handler" fits with the FLASH size available in the user Boot MAT.

The "users" boot code simply issues FCU commands to the FCU to program or erase the user MAT in user boot mode. Write the ROM program/erase routine in the user boot MAT by a desired communication interface and activate the SH7216 in user boot mode to use the SH7216 in user-defined boot mode. Write data in the user boot MAT in boot mode.

When activating the SH7216 in user boot mode, the program starts from the embedded program storing MAT, and transfers the FCU firmware to FCU RAM to jump to the reset vector on the User boot MAT.

The User MAT is programmed by activating the SH7216 with storing the user MAT program/erase routine in the user boot MAT, which is created by user. Execute the user MAT program/erase routine on RAM after copying to RAM. User boot MAT is set as default MAT on ROM in user boot mode, be sure to switch the MAT on ROM to the user MAT before programming. When issuing FCU commands to program/erase ROM with user boot MAT, FCU does not program or erase ROM.

4.2.3 USB Boot Mode

The boot mode allows the engineer the ability to program or erase the user MAT and user boot MAT by transmitting control commands and programming data from the host using the USB connection. This is convenient for design which requires the equipment to support a USB device connection. The USB boot mode needs programming data on the host side and a tool to send control commands and programming data. Figure 11 shows the system configuration in USB boot mode. All interrupt requests generated in USB boot mode are ignored. No interrupt requests should be generated on the system side.

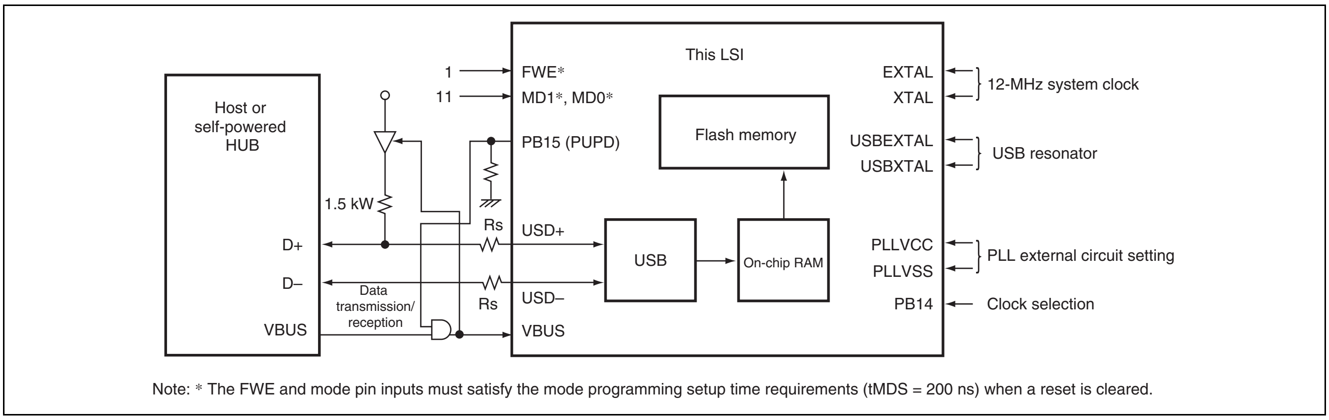


Figure 11 USB Boot Mode Connection

4.2.4 User Program Mode

Issue FCU commands to the FCU to program or erase the user MAT in user program mode. Unlike other flash memory programming modes, the MCU transitions from user program mode to user mode only by FWE pin setting (not via reset state).

Allocate the ROM program/erase routine by user-defined communication interface on the user MAT, and set FWE pin as high to transition to user program mode. In user program mode, the program transfers the FCU firmware to the FCU RAM, and communicates with the host via a desired interface to program or erase ROM. Copy the ROM program/erase routine created by user on RAM and execute the routine.

5. Handling of Pins

5.1 ASEMD0 pin

The ASEMD0 pin selects the H-UDI related functions.

Input the signal to the ASEMD0 pin at low to use the SH7216 in ASE mode, and input the signal at high to use the MCU in product-chip mode. To connect the SH7216 with the emulator using the H-UDI related pins, set the ASEMD0 pin at low to specify ASE mode. When using the boundary scan function, set the ASEMD0 pin at high to specify product-chip mode.

Do not change the input level of the ASEMD0 pin other than the RES assertion (input low level) time. This pin is internally pulled up.

5.2 TRST pin

The TRST pin is an initialization signal input pin in user debugging interface (H-UDI).

It accepts inputs from TCK asynchronously to reset the boundary scan circuit and H-UDI at low level. This pin is internally pulled up.

When turning on the SH7216, set the TRST pin at low as the RES pin for a certain period of time, specifically for oscillation settling time, upon using or not using the boundary scan circuit and H-UDI.

Figure 12 shows the peripheral circuit example of RES and TRST.

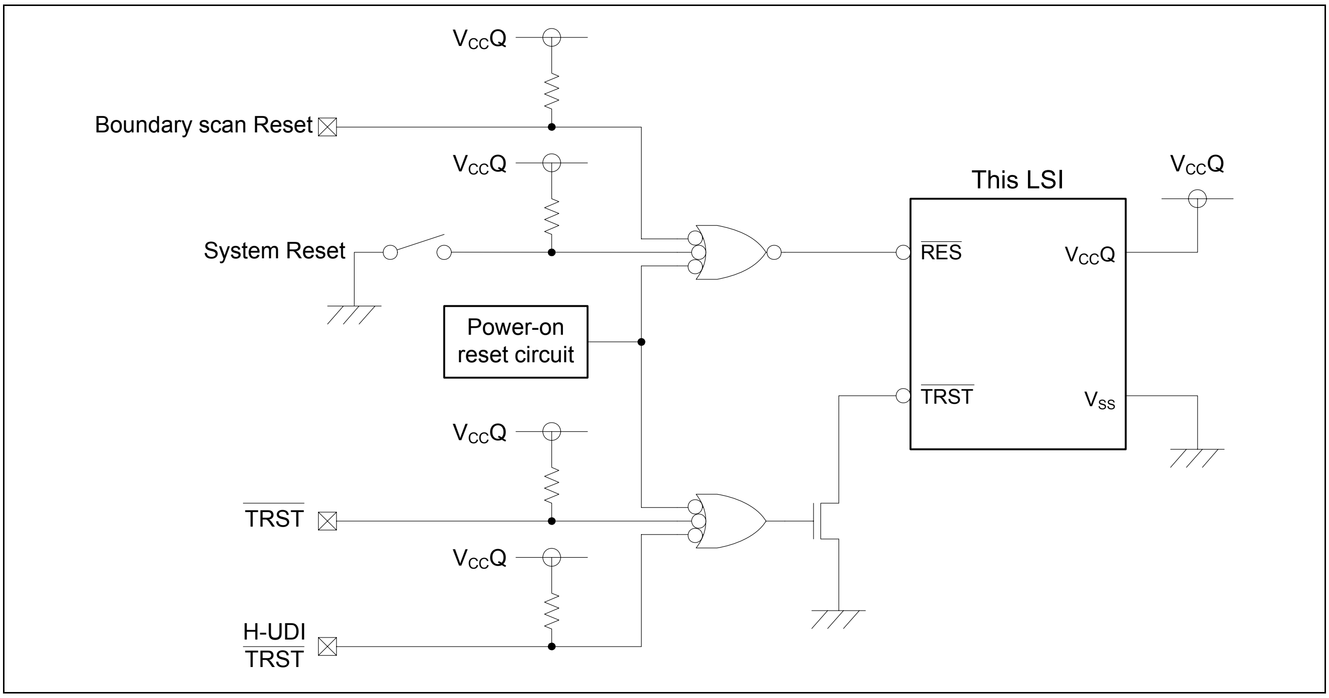
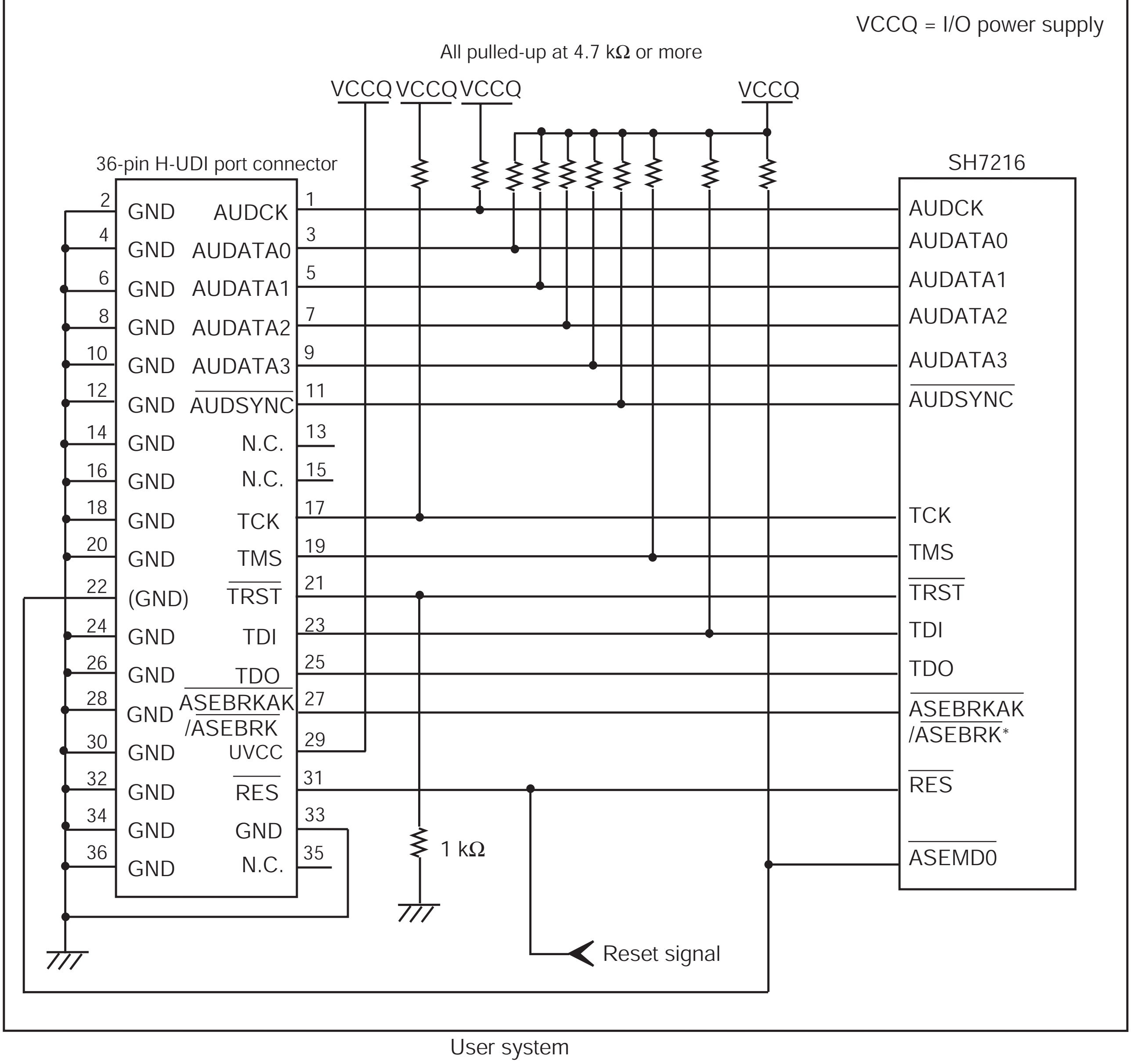


Figure 12 RES and TRST Peripheral Circuit Example

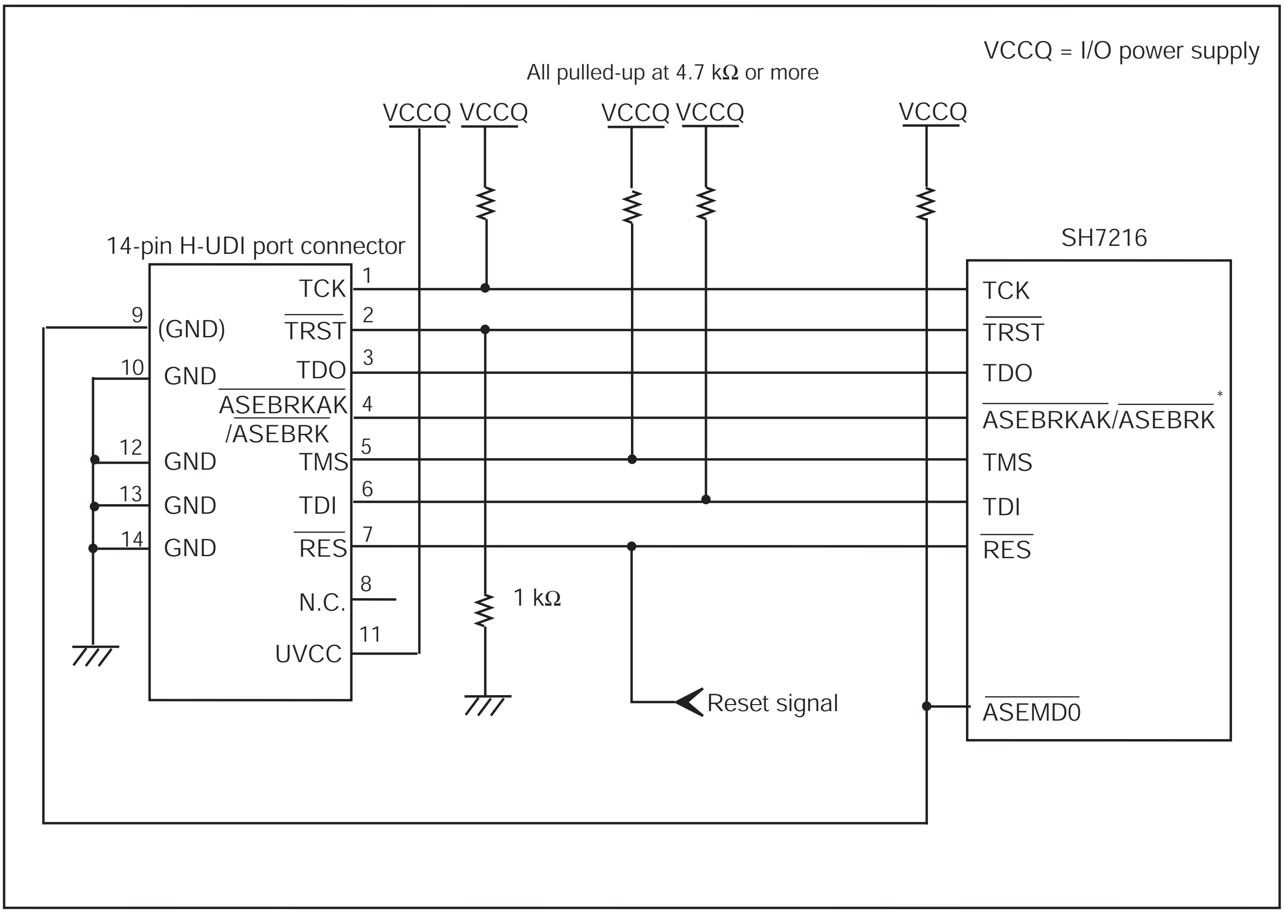
5.3 Signal Wiring to the E10A-USB and E8a Connectors

Figure 13 and Figure 14 show recommended circuits to wire the H-UDI signal when using the E10A-USB emulator. For more information, refer to the "SuperH™ Family E10A-USB Emulator Additional Document for User's Manual (Supplementary Information on Using the SH7216)".



Note:
The ASEBRKAK/ASEBRK pin (I/O pin) is multiplexed with the FWE pin (input pin). For the pin processing when the emulator is used and the user system is independently in operation, pins must be pulled up at 4.7 kΩ or more or pulled down at 100 kΩ. For the pin processing when the emulator is not used, refer to the hardware manual of the related MCU.

Figure 13 Recommended Circuit between the 36-pin H-UDI Port Connector and MCU (with E10A-USB)

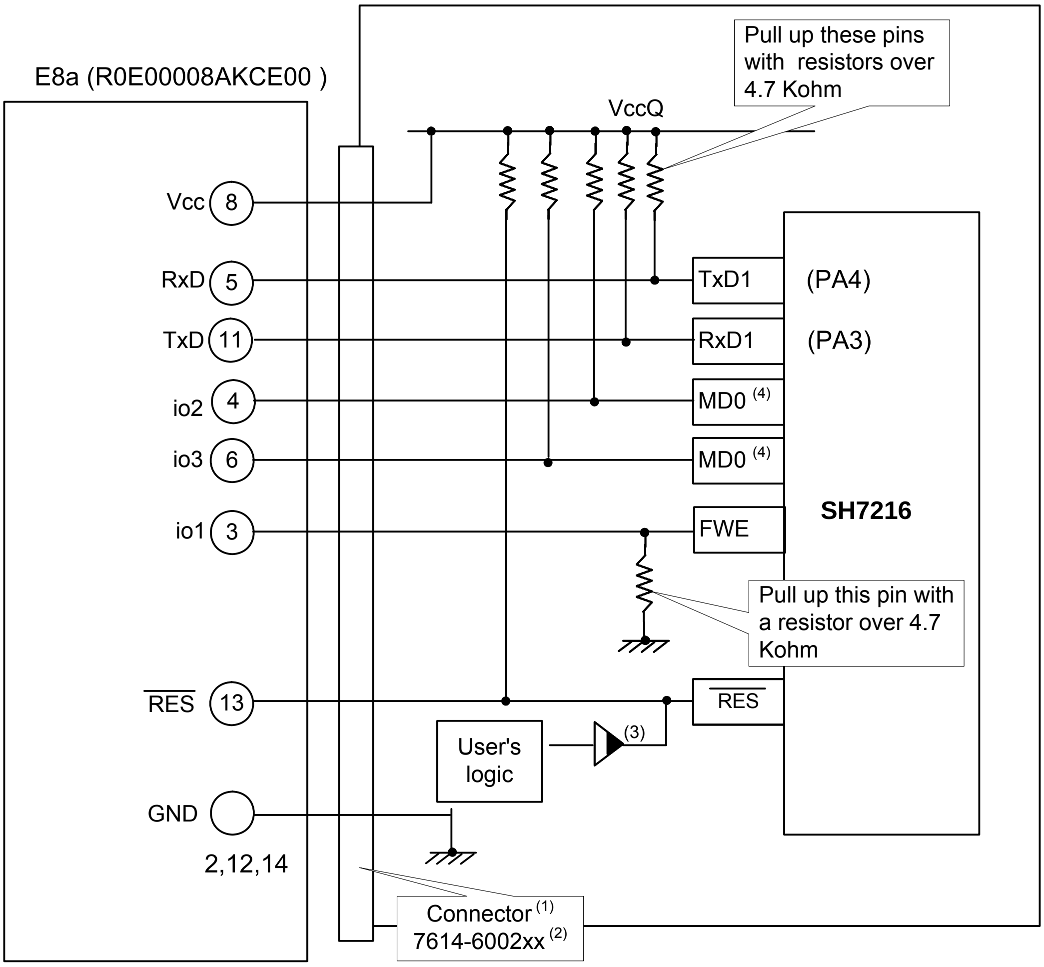


User system

Note: The ASEBRKAK/ASEBRK pin (I/O pin) is multiplexed with the FWE pin (input pin). For the pin processing when the emulator is used and the user system is independently in operation, pins must be pulled up at 4.7 kΩ or more or pulled down at 100 kΩ. For the pin processing when the emulator is not used, refer to the hardware manual of the related MCU.

Figure 14 Recommended Circuit between the 14-pin H-UDI Port Connector and MCU (with E10A-USB)

Figure 15 shows the connection example when using the flash development tool kit and E8a emulator. As pull-up and pull-down resistor values indicated in the following figure are for reference, evaluate the resistor value on user system before using.



(1) Manufacturer: Sumitomo 3M Ltd.
(2) xx indicates the plating specification.
(3) Open-collector buffer
(4) Change "MD0" and "MD1" connection from pull-up to pull-down, according to the mode.

Figure 15 SH7216 and E8a Emulator Connection

5.4 Pull-Up MOS Control

The SH7216 includes internal pull-up MOS for I/O pins other than PB12, PB13 input, data bus, MTU2S-related pins, MTU2-related pins, IIC3-related and EtherC-related pins to set ON or OFF by register setting. Multiplex pins depend on the pin function selected, otherwise, pull-up MOS is enabled.

Using the pull-up MOS to reduce the number of external pull-up resistors when designing the board. Note that the pull-up MOS is OFF during the power-on reset and until it is enabled by register setting after the MCU is woke up from the reset state. To avoid this state, install pull-up or pull-down resistors as appropriate.

5.5 POE Pin

The SH7216 has POE (port output enable) function to set the large-current and MTU2 ch0 pins to output high-impedance by $\overline{\mathrm{POE0}}$ to $\overline{\mathrm{POE4}}$, and $\overline{\mathrm{POE8}}$ pins. To use the POE function, input signals at high level to the large-current and MTU2 ch0 pins before setting $\overline{\mathrm{POE0}}$ to $\overline{\mathrm{POE4}}$,, and $\overline{\mathrm{POE8}}$ pins to input PEO by the PFC.

5.6 Analog Pins

5.6.1 Notes on Designing Board

Analog pins AN0 to AN7 are only for the input, applicable when using as PF0 to PF7 ports.

Place the digital circuit and analog circuit as far as possible on the board. Analog circuits signals must be wired prior to digital circuit signals, and avoid intersecting with or being close to the digital circuit signals. Failure to do so may result in the malfunction of analog circuit and adversely affecting the A/D conversion values.

Isolate analog input signals (AN0 to AN7), analog reference voltage (AVREF), analog power supply (AV_{CC}), and analog ground (AV_{SS}) from the digital circuit. AV_{SS} must be connected on a stable digital ground (V_{SS}) on board.

5.6.2 Analog Pin Protection Circuit

As shown in Figure 16, connect the protection circuit between AV_{CC} and AV_{SS} to prevent damage due to an abnormal voltage, such as an excessive surge at analog input pins (AN0 to AN7) and analog reference voltage (AVREF). Connect the other end of the bypass capacitor (connected to AVREF) and filter capacitor (connected to ANn) to $AVREFV_{SS}$. Place the 0.1 µF capacitor as close as possible to pins. When connecting the filter capacitor as shown in Figure 16, the analog input pin (ANn) input current is averaged to cause an error. Consider the circuit constants as appropriate before deciding.

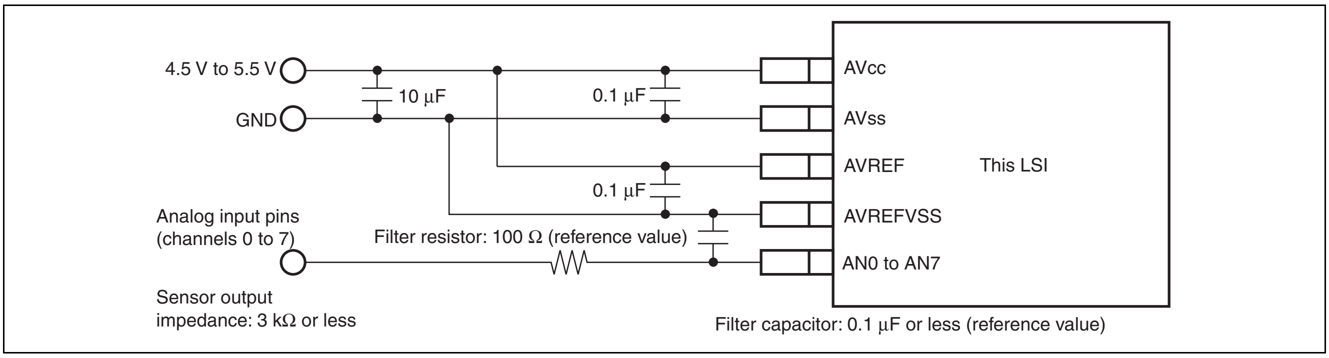


Figure 16 Analog Input Pin Protection Circuit Example

5.6.3 Permissible Signal Source Impedance

The SH7216 analog input is designed to guarantee the conversion accuracy for the input signal when its source impedance is equal to or less than 3 kΩ. This specification is to charge the input capacitance of the A/D converter sample-and-hold circuit within the sampling time. When the sensor output impedance exceeds 3 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. If a large capacitance is provided externally when converting analog to digital in single mode, the input load essentially comprise only the 10 kΩ internal input resistance, and the signal source impedance is not required. However, the SH7216 ADC includes a low-pass filter, it may not be able to handle the analog signal with a large differential coefficient (e.g., 5 mV/µs or greater). Install a low-impedance buffer when converting a high-speed analog signal or converting signals in scan mode.

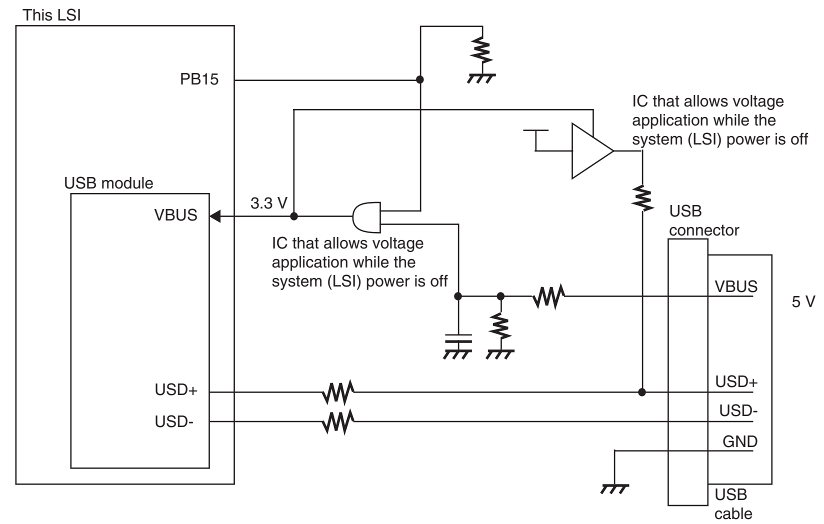
5.7 USB Pins

(1) USD+ Pull-Up Control

Control the USB+ pull-up by the general-purpose output port to delay the connection notification (such as high-priority processing or initialization) to a USB host or hub. When the USB cable is already connected to the USB host or hub and USD+ pull-up is disabled, the USD+ and USD– signals are driven low (these signals are pulled down on the host or hub) and the USB module incorrectly recognizes that it has received the USB bus reset signal from the host. Control the USD+ pull-up control signal and VBUS pin input signal by the general-purpose output port and USB cable VBUS as shown in Figure 17. (The SH7216 UDC core holds the powered state while the VBUS pin level is low regardless of the USD+ and USD− states.)

(2) Detection of an Attachment or Removal of the USB Cable

As the SH7216 controls the USB state by hardware, it requires the VBUS signal to detect an attachment or removal of the USB device. As the VBUS uses the power supply signal (VBUS) from the USB cable, the USB host or hub supplies 5 V voltage to the USB cable when the USB host or hub is connected while the USB function is not ON. Install an IC such as HD74LV1G08A, and 2G08A externally to apply voltage when the system power is OFF.



Note: This circuitry example does not guarantee the operation. When the system requires measures against external surge or ESD noise, implement measures with a compensation diode or noise canceler circuit.

Figure 17 Example of USB Function Module External Circuitry

(3) Handling of Unused USB Pins

When not using the USB, handle the unused pins as listed in Table 4.

Table 4 Handling of Unused USB Pins

Pin Name	Description
DrVCC, VCCQ	3.0 to 3.6 V
DrVSS	Connect to Vss
USB+, USD−	Open
VBUS, USBEXTAL	Connect to Vss
USBXTAL	Open

5.8 Handling of Unused Pins

Connect the unused pins to $V_{CC}Q$ or V_{SS} via resistors to fix high or low levels on the pins.

Handle port F, pins NMI, USD+, USD−, XTAL, USBEXTAL, USBXTAL, $\overline{\text{WDTOVF}}$, $\overline{\text{TRST}}$, TMS, TCK, TDO, and TDI as listed in Table 5.

Table 5 Handling of Unused Pins

Pin Name	Description
Port F	Connect and fix to AV_{CC} or AV_{SS} via a resistor
NMI	Connect to $V_{CC}Q$ via a resistor to fix to high
USD+, USD−	Open
XTAL, USBXTAL	Open
USBEXTAL	Connect to VSS
$\overline{\text{WDTOVF}}$	Open. When pull-down is required, install a resistor with 1 MΩ or bigger
$\overline{\text{TRST}}$	Fix the $\overline{\text{TRST}}$ to low. Open other pins.
TMS, TCK, TDO, TDI	Open
Other	Connect to VCCQ or VSS via a resistor to fix the level

6. On-Chip Resource Access

Table 6 shows number of cycles for access to the on-chip resources.

Table 6 Number of Cycles for Access to the On-Chip Resources

	Flash Memory	SRAM	Peripherals
Read	ROM Cache Hit: 1 $I\phi$ ROM Cache Miss: 4 $I\phi$	Pages 0 to 3: 1 $I\phi$ Pages 4 to 7: 2 $I\phi$	2 or more $P\phi$ (note)
Write	–	Pages 0 to 3: 1 $I\phi$ Pages 4 to 7: 3 $I\phi$	2 or more $P\phi$ (note)

Note: As the SH7216 includes a multilayered bus structure, each bus (C bus, I bus, and P bus) inputs or outputs data in sync with $I\phi$, $B\phi$, and $P\phi$ clock, respectively. Therefore, the number of cycles to access on-chip peripheral registers varies as follows:

Table 7 Number of Cycles to Access On-chip Peripheral Registers

	Number of access cycles	Remarks
Write	$(2+n) \times I\phi + (1+m) \times B\phi + 2 \times P\phi$	Applicable other than the FLD, E-DMAC, and EtherC
	$(2+n) \times I\phi + (1+m) \times B\phi + 3 \times P\phi$	Applicable when accessing FLD
	$(2+n) \times I\phi + 3 \times B\phi$	Applicable when accessing the E-DMAC
	$(2+n) \times I\phi + 9 \times B\phi$	Applicable when accessing the EtherC
Read	$(2+n) \times I\phi + (1+m) \times B\phi + 2 \times P\phi + (2+l) \times I\phi$	Applicable other than the FLD, E-DMAC, and EtherC
	$(2+n) \times I\phi + (1+m) \times B\phi + 3 \times P\phi + (2+l) \times I\phi$	Applicable when accessing FLD
	$(2+n) \times I\phi + 4 \times B\phi + (2+l) \times I\phi$	Applicable when accessing the E-DMAC
	$(2+n) \times I\phi + 12 \times B\phi + (2+l) \times I\phi$	Applicable when accessing the EtherC

When $I\phi:B\phi = 1:1$, n = 0 and l = 0
When $I\phi:B\phi = 2:1$, n = 1 to 0 and l = 0
When $I\phi:B\phi = 4:1$, n = 3 to 0 and l = 0, 1
When $I\phi:B\phi = 8:1$, n = 7 to 0 and l = 1
When $B\phi:P\phi = 1:1$, m = 0
When $B\phi:P\phi = 2:1$, m = 1 to 0
The above values are the number of access cycles when executing the internal ROM or internal RAM instructions. Values n and m depend on the state of the internal execution.

7. Endianness

The SH7216 supports big-endian order to store the most significant byte (MSB) at the lowest address 0, and little-endian order to store the least significant byte (LSB) at the lowest address 0. The ENDIAN bit in the CSnBCR register specifies endian when the target area (Areas 1 to 7) is not accessed. CSnBCR setting is invalid in area 0 in on-chip ROM disabled mode. In on-chip ROM enabled mode, the CSnBCR specifies the endian in areas 0 to 7.

Note that the data position and strobe signals corresponding to addresses depend on the byte order, big endian or little endian. $\overline{\text{WRH}}$ indicates address 0 in big-endian, but $\overline{\text{WRL}}$ indicates address 0 in little-endian.

Two good examples of the using the little endian support in the external data spaces are Memory Mapped devices that are Little Endian and communicating with little Endian MCUs through dual port memory.

Area 0 cannot be specified as little endian. Since the instruction fetch is mixed with the 32- and 16- bit access, it cannot be allocated to the little endian area. Always execute instructions within the big endian areas, internal or external.

8. Power-down Modes

The SH7216 has the following power-down modes and function.

1. Sleep mode
2. Software standby mode
3. Module standby function

As some peripherals and CPU stops in power-down modes, it will reduce power consumption. The SH7216 wakes up from these modes by reset or interrupt.

Table 8 States of Power-Down Modes

Power-Down Mode	Transition Conditions	State						How to Wake up the MCU
		CPG	CPU	CPU Register	Internal memory	Internal peripheral modules	External Memory	
Sleep mode	Execute SLEEP instruction when the STBY bit in the STBCR is 0	ON	OFF	States held	ON	ON	Auto-refresh	• Interrupt • Manual reset • Power-on reset • DMA address error
Software standby mode	Execute SLEEP instruction when the STBY bit in the STBCR is 1	OFF	OFF	States held	OFF (Data is retained)	OFF	Self-refresh	• NMI interrupt • IRQ interrupt • Manual reset • Power-on reset
Module standby function	Set the MSTP bits in STBCR2, STBCR3, STBCR4, STBCR5, STBCR6	ON	ON	States held	Specified module is OFF (Data is retained)	Specified module is OFF	Auto-refresh	• Clear the MSTP bit to 0 • Power-on reset (Only for H-UDI, UBC, and DMAC)

8.1 Sleep Mode

In the sleep mode, only CPU stops its operation.

When executing the SLEEP instruction while the STBY bit in the STBCR register is 0, the SH7216 transitions from the program execution state to sleep mode. The CPU stops its operation immediately after executing the SLEEP instruction; however internal register values remain unchanged, and on-chip peripherals continue to operate in sleep mode. The CK pin continues to output clock pulses during the on-chip ROM enabled/disabled external extension mode.

8.2 Software Standby Mode

The SH7216 stops its operation completely in software standby mode.

When executing the SLEEP instruction while the STBY bit in the STBCR register is 1, the SH7216 transitions from the program execution state to software standby mode. Not only the CPU, but the clock and on-chip peripherals stop operation in software standby mode. In addition, the CK pin stops outputting clock pulses in the on-chip ROM enabled/disabled external extension mode.

CPU register values are retained in software standby mode. On-chip peripherals registers listed in Table 9 are initialized and other register values are retained in software standby mode.

Table 9 Initialized Registers in Software Standby Mode

Module Name	Registers	Remarks
A/D converter (ADC)	All	
Serial Communication Interface with FIFO (SCIF)	Serial extended mode register (SCSEMR)	Other register values are retained
Watch Dog timer (WDT)	WTCNT, WRCSR	WTCSR is retained
I^2C Bus Interface 3 (IIC3)	BC [2:0] bits in the I2C bus mode register (ICMR)	Register values other than ICMR BC [2:0] bits are retained

The CPU writes data in the STBCR register in a cycle and executes the next instruction. However, it takes one or more cycles to actually write data in the register. Therefore, execute the SLEEP instruction after reading the STBCR register to reflect the write value from CPU to the STBCR in the SLEEP instruction.

The procedure to transition to software standby mode is as follows. This is to secure the clock stabilization time before supplying the clock to the SH7216.

1. Clear the TME bit in the WDT timer control register (WTCSR) to 0 to stop the WDT.
2. Set the WDT timer counter (WTCNT) to 0 and CKS [2:0] bits in the WTCSR register as appropriate to set the specified oscillation settling time.
3. Read the STBCR register after setting the STBY bit in the STBCR register to 1. Then, execute the SLEEP instruction

8.3 Module Standby Function

The module standby function stops on-chip peripherals separately.

Set the MSTP bit in the Standby control register of each module to 1 to stop supplying clock to the corresponding on-chip peripherals. The power consumption is reduced in normal mode and sleep mode by this function. Be sure to disable a module before setting it in module standby mode. Do not access the registers of a module which is in module standby mode.

When using module standby function, registers listed in Table 10 are initialized and other register values are retained.

Table 10 Initialized Registers When Using Module Standby Function

Module Name	Registers	Remarks
Serial Communication Interface (SCI)	All	
Serial Communication Interface with FIFO (SCIF)	Serial extended mode register (SCSEMR)	Other register values are retained
I^2C Bus Interface 3 (IIC3)	BC [2:0] bits in the I2C bus mode register (ICMR)	Register values other than ICMR BC [2:0] bits are retained
Multi-Function Timer Pulse Unit 2 (MTU2)	All	
Multi-Function Timer Pulse Unit 2S (MTU2S)	All	
Compare Match Timer (CMT)	All	
Renesas Serial Peripheral Interface (RSPI)	All	
Controller Area Network (RCAN-ET)	All	Other than mailboxes

8.4 Pin States in Power-down Modes

As the peripheral modules operate in sleep mode, the pin state varies according to the operation of peripheral modules.

When using module standby function for the module specified as PFC, the pins of the module whose registers to be initialized at the module standby function is configured to default state, and the pin of the module whose registers not to be initialized at the module standby function retains the state immediately before entering module standby mode.

The pin states in the software standby mode depend on the pin. The states of multiplex pin vary according to the pin setting of MD0, MD1, FWE, and the pin function specified by the PFC.

(1) External Bus Pins

Data bus D0 to D31 enters the high impedance. The states of other bus pins depend on the setting of bits HIZCKIO, HIZMEM, and HIZCNT in the CMNCR register. When these bits are 1, the pin state is output. When these bits are 0, the pin state is in high impedance. Table 11 lists the relations between bits in the CMNCR register and bus-related pins.

Table 11 Relationship between Bits in the CMNCR and Bus-related Pins

Pin Name	Bit to Specify
CK	HIZCKIO bit
A25 to A0, $\overline{\text{BS}}$, RD/$\overline{\text{WR}}$, $\overline{\text{WRxx}}$/DQMxx, $\overline{\text{AH}}$, $\overline{\text{RD}}$	HIZMEM bit
CKE, $\overline{\text{RASL}}$, $\overline{\text{CASL}}$, $\overline{\text{RASU}}$, $\overline{\text{CASU}}$	HIZCNT bit

(2) High-Current Pins

The states of the high-current pins depends on bits MZIZDH, MZIZDL, MZIZEH, and MZIZEL in the HCPCR register, and the HIZ bit in the STBCR3 register, and I/O setting of each pin. Table 12 shows the relations between control bits and the I/O setting and the pin states. Table 13 shows the relations between bits in the HCPCR register and controlled pins.

Table 12 Relations Between Each Control Bit and the I/O Setting and the Pin States

Bits setting in the HCPCR register	HIZ bit setting in the STBCR3 register	I/O setting	High-current Pin State in Software Standby Mode
0	–	–	High impedance
–	1	x	High impedance
1	0	Input	High impedance
1	0	Output	Retains the pin state

Note: –: Don't care

Table 13 Relations Between Bits in the HCPCR Register and Controlled Pins

Bits in the HCPCR Register	Controlled Pins
MZIZDL	PD10/TIOC3BS, PD11/TIOC3DS, PD12/TIOC4AS, PD13/TIOC4BS, PD14/TIOC4CS, PD15/TIOC4DS
MZIZDH	PD24/TIOC4DS, PD25/TIOC4CS, PD26/TIOC4BS, PD27/TIOC4AS, PD28/TIOC3DS, PD29/TIOC3BS
MZIZEL	PE0/TIOC4AS, PE1/TIOC4BS, PE2/TIOC4CS, PE3/TIOC4DS, PE5/TIOC3BS, PE6/TIOC3DS
MZIZEH	PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B, PE14/TIOC4C, PE15/TIOC4D

(3) Other Output Pins and I/O Pins

States of the following output pins and I/O pins depend on the HIZ bit in the STBCR3 register. When the HIZ bit is 1, pin states of the following pins are in high impedance. When the HIZ bit is 0, pin states of the following output pins and I/O pins configured as output are retained, and I/O pins configured as input are in high impedance. However, the IRQOUT pin and the REFOUT pin outputs high level signal when the HIZ bit is 0, and the I/O of the MDIO pin is retained when the HIZ bit is 0.

Table 14 shows the target pins to be controlled by the HIZ bit in the STBCR3 register, other than the high-current pins.

Table 14 Target Pins by the HIZ bit in the STBCR3 Register

STBCR3 Register	Target Pin
HIZ bit	IRQOUT, REFOUT, DACK0 to DACK3, TEND0, TEND1, SCK0 to SCK4, TXD0 to TXD4, RSPCK, SSLO, MISO, SSL, UBCTRG, CTx0, MDC, TX_EN, MII_TXD0, MII_TXD1, MII_TXD2, MII_TXD3, TX_ER, EXOUT, WOL, PA0 to PA21, PB0 to PB11, PB14, PB15, PC0 to PC15, PD0 to PD9, PD15 to PD23, PD30, PD31, PE4, PE7, PE8, PE10, TIOC0A, TIOC0B, TIOC0C, TIOC0D, TIOC1A, TIOC1B, TIOC2A, TIOC2B, TIOC3A, TIOC3C, TIOC3AS, TIOC3CS

The following pins are not affected by the register setting.

Table 15 Pins Independent from the Register Setting

Pin Name	Description
WDTOVF	Retains output state
XTAL, USBXTAL	Outputs low level signal

(4) Input Pins

Table 16 lists the states of the input pins.

Table 16 Input Pin States

Pin Name	Description
EXTAL, RES, MRES, MD0, MD1, FWE, NMI, IRQ0 to IRQ7, USBEXTAL, VBUS, USD+, USD−, RX_ER, RX_DV, TX_CLK, COL, CRS, RX_CLK, MII_RXD0, MII_RXD1, MII_RXD2, MII_RXD3	Input
BREQ, BACK, D0 to D31, DREQ0, DREQ1, TIC5U, TIC5V, TIC5W, TIC5US, TIC5VS, TIC5WS, POE0 to POE4, POE8, RXD0 to RXD4, MOSI, SCL, SDA, AN0 to AN7, ADTRG, CRx0, PB12, PB13, PF0 to PF7, LNKSTA	Hi-Z
ASEMD0	Input (or it is pulled up internally when no signal is input)

9. RCAN-ET External Circuit Example

CAN is a two wire (CAN_H and CAN_L) differential bus. To transmit the signal from the RCAN-ET to the CAN bus or transmit the signal from other MCU via the CAN bus to the RCAN-ET, a CAN transceiver must be inserted between the RCAN-ET and CAN bus to convert the signal. As the SH7216 CAN-related pins requires supply voltages at 3.3 V, a level shifter is also required to interface with the 5-V transceiver.

This section provides an example to use the HA13721RP (5-V CAN transceiver). The HA13721RP TxD pin to connect to the RCAN-ET CTx pin tolerates the supply voltage of 3.3 V, however, the HA13721RP RxD pin to connect to the RCAN-ET CRx pin only tolerates 5 V. Therefore, a level shifter from 5 V to 3.3 V has to be inserted between the HA13721RP RxD pin and the RCAN-ET CRx pin.

Figure 18 shows the RCAN-ET external circuit. Table 17 lists the electrical characteristics of the HA13721 (extract). For more information, refer to the HA13721RP/FP data sheet.

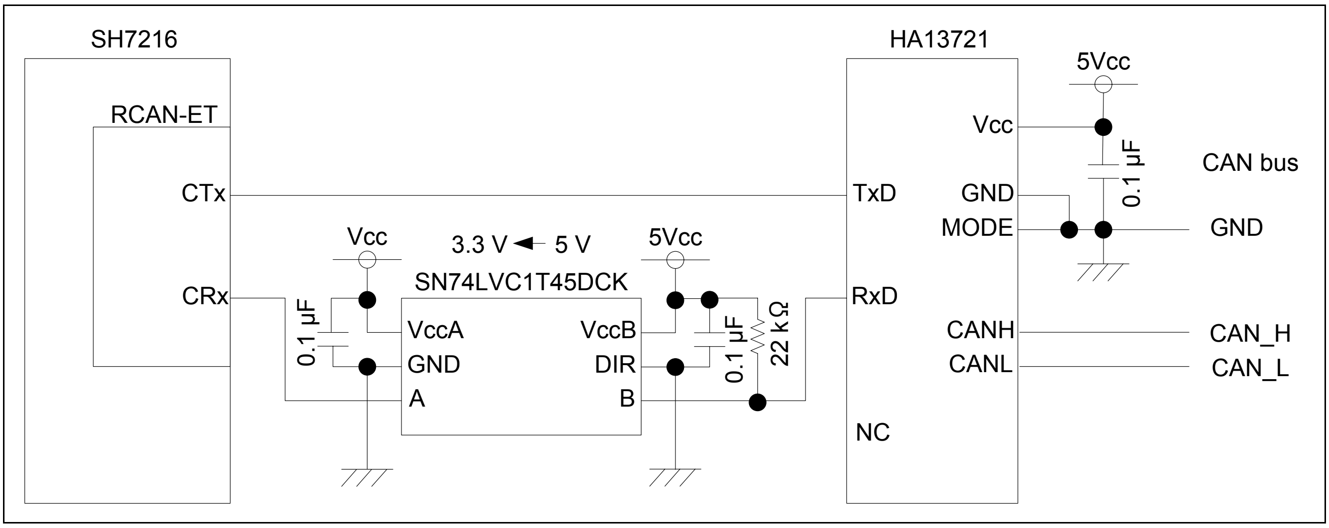


Figure 18 RCAN-ET External Circuit

Table 17 HA13721 Electrical Characteristics (Extract)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Applicable Pins
Power supply voltage	Vcc	4.5	–	5.5	V		Vcc
Input High voltage	VIH	2.4	–	Vcc+0.3	V		TxD MODE
Input Low voltage	VIL	−0.3	–	0.8	V		TxD MODE
Output High voltage	VOH	0.8Vcc	–	Vcc	V	IRxD = −100 µA	RxD
Output Low voltage	VOL	–	–	0.1Vcc	V	IRxD = 1 mA	RxD

10. Ethernet PHY-LSI Interface

10.1 Interface

10.1.1 Media Independent Interface (MII)

The Media Independent Interface (MII) is a standard interface used to connect a network controller chip (MAC) with the media interface chip (PHY). Figure 19 shows the MII signal connection.

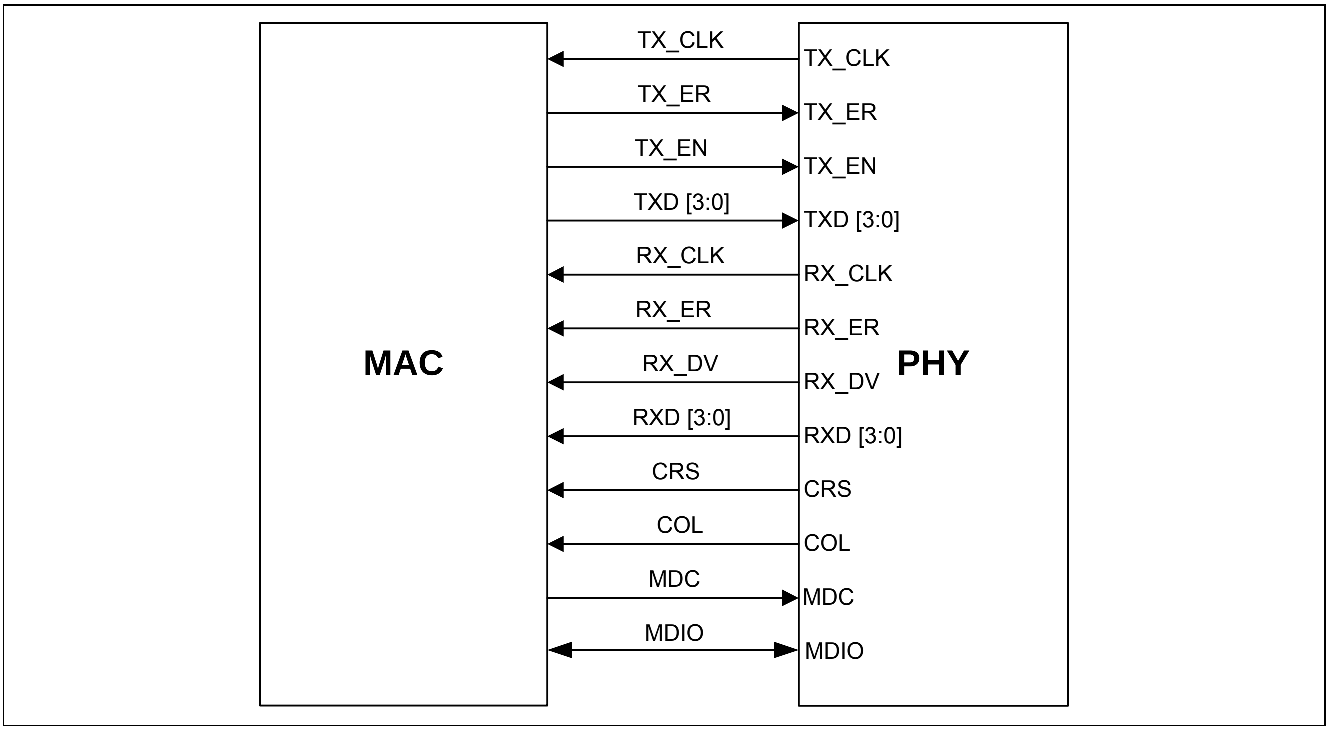


Figure 19 MII Signal Connection

10.1.2 Media Dependent Interface (MDI)

The Media Dependent Interface (MDI) is an interface used to connect the media interface chip (PHY) with the pulse transformer or RJ45 connector. Figure 20 shows the MDI signal connection.

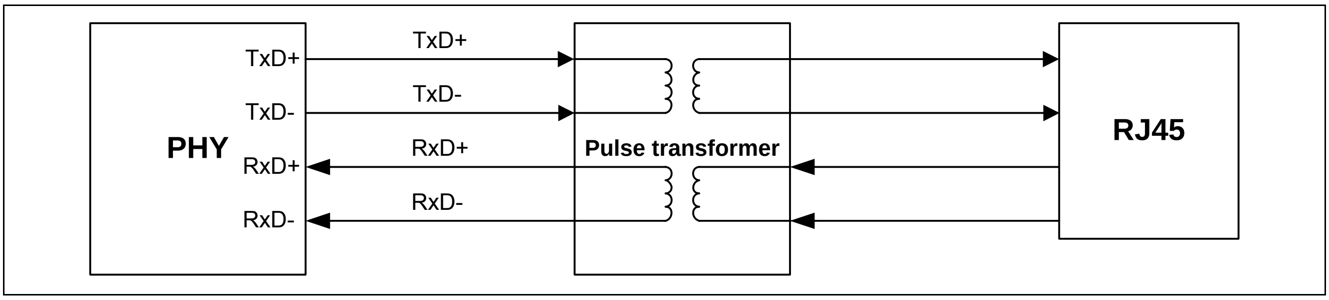


Figure 20 MDI Signal Connection

10.2 Interface Pins Functions

10.2.1 Media Independent Interface

Table 18 lists the pin functions of the Media Independent Interface (MII).

Table 18 Media Independent Interface (MII) Pin Functions

Signal Name	Function	I/O (MAC)	I/O (PHY)	Remarks
TX_CLK	Transmit clock	I	O	TX_EN, TXD [3:0] and TX_ER timing clocks 10Base-T: 2.5 MHz 100Base-TX: 25 MHz
TX_ER	Transmit error	O	I	
TX_EN	Transmit enable	O	I	
TXD0	Transmit data	O	I	
TXD1	Transmit data	O	I	
TXD2	Transmit data	O	I	
TXD3	Transmit data	O	I	RX_DV, RXD [3:0], and TX_ER timing clocks 10Base-T: 2.5 MHz 100Base-T: 25 MHz
RX_CLK	Receive clock	I	O	
RX_ER	Receive error	I	O	
RX_DV	Receive data invalid	I	O	
RXD0	Receive data	I	O	
RXD1	Receive data	I	O	
RXD2	Receive data	I	O	
RXD3	Receive data	I	O	
CRS	Carrier detection	I	O	
COL	Collision detection	I	O	
MDC	Administrative data clock	O	I	
MDIO	Administrative data I/O	I/O	I/O	

10.2.2 Media Dependent Interface (MDI)

Table 19 lists the pin functions of the Media Dependent Interface (MDI).

Table 19 Media Dependent Interface (MDI) Pin Functions

Signal Name	Function	I/O (PHY)	Remarks
TXD+	Transmit output+	O	Differential signal transmit output
TXD−	Transmit output−	O	
RXD+	Receive input+	I	Differential signal receive input
RXD−	Receive input−	I	

10.3 Transmission Line

10.3.1 MII

When designing the MII wiring pattern, note the following:

- MII transmission line must be designed as the high-frequency circuit.
- Place the MII transmission line on the layer adjacent to GND plane.
- Place the MII transmission line as short as possible.
- Do not allocate other signal lines close to the MII transmission line.
- Avoid using vias on the MII transmission line.
- MII transmission line must be wired with straight lines. If you cannot avoid doing so, the line must be bent gently in an arc or up to 135 degrees.
- Add the series resistors on all transceiver MII outputs.
- Impedance must be controlled on the MDC pin transmission line. The characteristic impedance required for the MDC pin transmission line is the differential impedance 50 Ω ± 15%. The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more information.
- Install a resistor of 1.5 kΩ ± 5% on the MDIO pin transmission line.

Figure 21 shows the guideline for the wiring corner angle. Figure 22 shows the MII layout example.

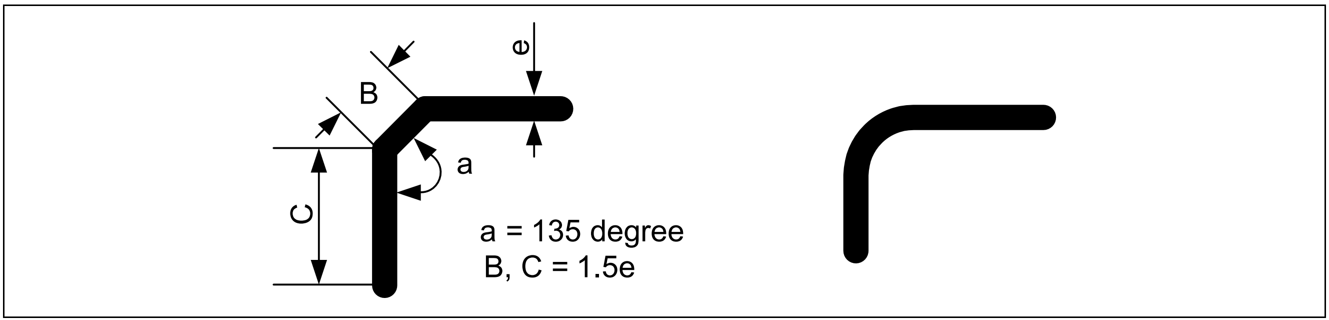


Figure 21 Wiring Corner Angle

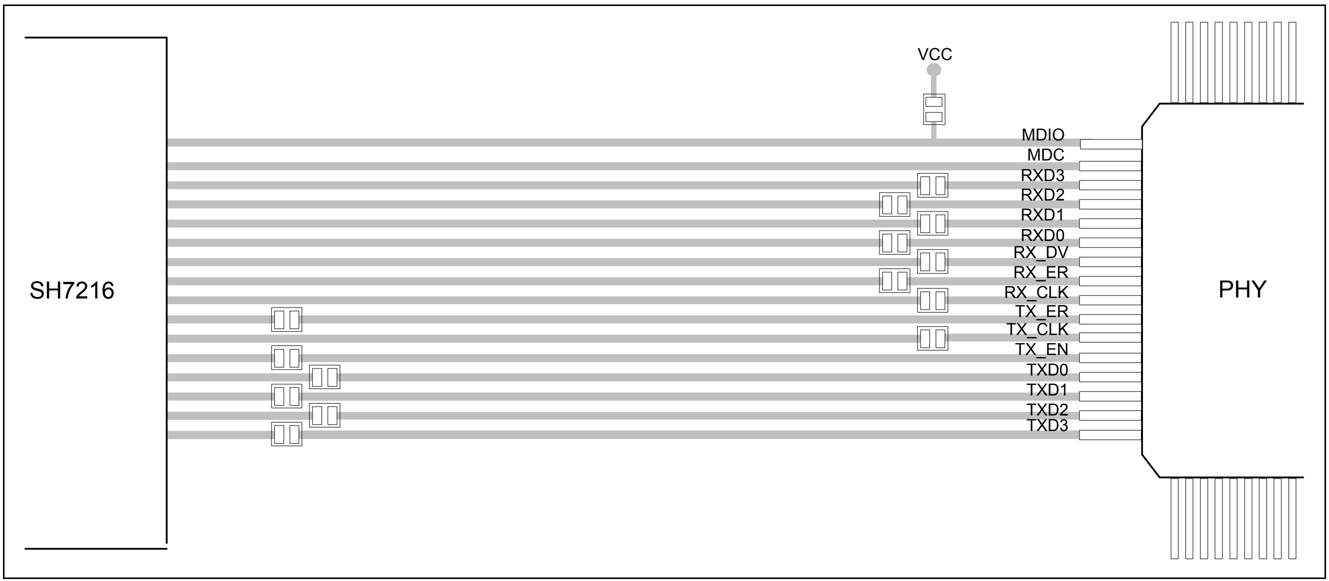


Figure 22 MII Layout

10.3.2 MDI

MDI transmission line must be designed as the high-frequency circuit. Impedance must be controlled on the line.

Refer to the datasheet of PHY when designing the wiring pattern, and termination pattern of the MDI transmission line.

10.4 Power Supply, Ground

When designing the MII power supply and ground pattern, note the following:

10.4.1 MII

- VCC and GND planes must be designed as wide as possible.
- Use low inductance, ceramic surface mount decoupling capacitors.
- As the ESR (Equivalent Series Resistor) of the aluminum electrolytic capacitor and tantalum capacitor are generally high which may affect the jitter value, these capacitors should be thoroughly designed and tested before use.
- Locate these decoupling capacitors as close as possible to the VCC and GND pins of the PHY.
- Connect the decoupling capacitor to the VCC and GND planes to achieve the lowest possible inductance.
- All decoupling capacitor and PHY VCC and GND connections should tie immediately to a VCC or GND plane via with minimum trace inductance.

10.4.2 MDI

Refer to the datasheet of PHY when designing the MDI power supply and ground pattern

11. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7214 Group, SH7216 Group Hardware User's Manual Rev. 2.00
  The latest version of the hardware user's manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jan.14.10	—	First edition issued
2.00	Sep.10.10	17	Figure 16, revised (SH7214 Group, SH7216 Group Hardware User's manual updated)
		20	Table 7, added (SH7214 Group, SH7216 Group Hardware User's manual updated)
		26	RCAN-ET external circuit example added
		27 to 30	Ethernet PHY board design guide added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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