SH7216 Group

Data Transfer Using MTU2 (Compare Match) as DTC Activation Source

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Introduction

This application note presents an example of data transfer by the DTC in which the MTU2 of the SH7216 is used as the activation source. The DTC is activated with MTU2 compare match as the source and transfers data from the on-chip flash memory (ROM) to the on-chip RAM.

Note that although the sample tasks and applications presented in this application note have been verified to work as intended, they should be checked in the actual operating environment before being put into actual use.

Target Device

SH7216

Contents

1. Introduction

1.1 Specifications

- Compare match on MTU2 channel 0 is used as the as the activation source for the DTC.
- The DTC transfers data from the on-chip flash memory (ROM) to the on-chip RAM.
- The normal data transfer mode is used.
- The data transfer size is longword and 64 transfers are performed (for a total of 256 bytes).

1.2 Functions Used

- Multi-function timer pulse unit 2 (MTU2), channel 0
- Data transfer controller (DTC), channel 0

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.06.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03.00, Release 00
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu –pic=1 –object="$(CONFIGDIR)¥$(FILELEAF).obj" -debug -gbr=auto –chgincpath –errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

2. Description of Sample Application

The sample application transfers data from the on-chip flash memory (ROM) to the on-chip RAM, using compare match on MTU2 (channel 0) as the source to activate the DTC.

2.1 Operation of Functions Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

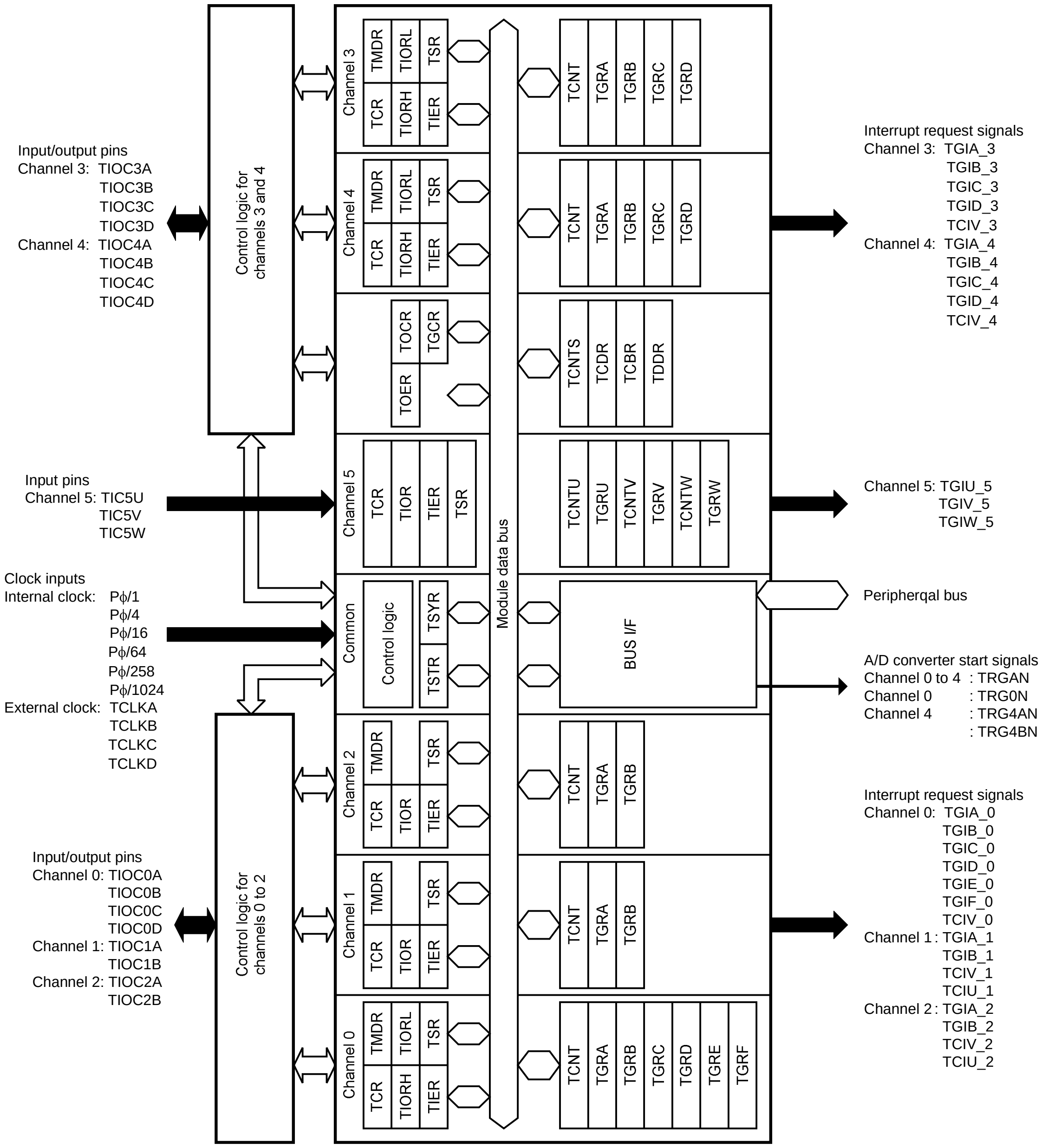
Multi-function timer pulse unit 2 (MTU2) is a multifunction timer unit that comprises six 16-bit timer channels. Each channel can be set to perform functions such as compare match and input capture. Channels 0 to 4 support waveform output using compare match, an input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clearing by compare match or input capture, simultaneous I/O to and from registers using synchronized counter operation, and up to 12-phase PWM output in combination with synchronous operation.

For details of the MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the *SH7216 Group Hardware Manual*.

Table 1 shows an outline of multi-function timer pulse unit 2 (MTU2). Figure 1 is a block diagram of MTU2.

Table 1 MTU2 Outline

Item	Description
Channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clocks	Selectable among eight counter input clocks for each channel (four counter input clocks for channel 5)
Operations of channels 0 to 5	• Waveform output using compare match, input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clearing by compare match or input capture • Simultaneous I/O to and from registers using synchronized counter operation, up to 12-phase PWM output in combination with synchronous operation.
A/D converter triggers	• Ability to generate A/D converter start triggers • Support for generation of interrupts at counter crest and trough as well as skipping of A/D converter start triggers in complementary PWM mode
Buffer operation	Support for register buffer settings for channels 0, 3, and 4
Operating modes	• PWM mode setting support for channels 0 to 4 • Independent phase counting mode setting support for channels 1 and 2 • Support for a total of six PWM waveform outputs consisting of three-phase positive and negative waveform outputs using complementary PWM mode or reset synchronous PWM mode and linked operation of channels 3 and 4
Interrupt requests	28 interrupt sources (compare match and input capture interrupts, etc.)
Other	• Operation with cascade connections • High-speed access via internal 16-bit bus • Automatic transfer of register data • Module standby mode • Dead time compensation counter function on channel 5



[Legend]

TSTR: Timer start register
TSYR: Timer synchronous register
TCR: Timer control register
TMDR: Timer mode register
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TGCR: Timer gate control register
TOER: Timer output master enable register
TOCR: Timer output control register
TSR: Timer status register
TCNT: Timer counter
TCNTS: Timer subcounter
TCDR: Timer cycle data register
TCBR: Timer cycle buffer register
TDDR: Timer dead time data register
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W

Figure 1 MTU2 Block Diagram

2.1.2 Data Transfer Controller (DTC)

Three transfer modes are supported: normal, repeat, and block. Data transfer can be performed using a number of channels specified by the user by storing transfer information in the data area. When the DTC is activated, it reads the transfer information from the data area, performs the data transfer, and then writes back the transfer information after the data transfer completes.

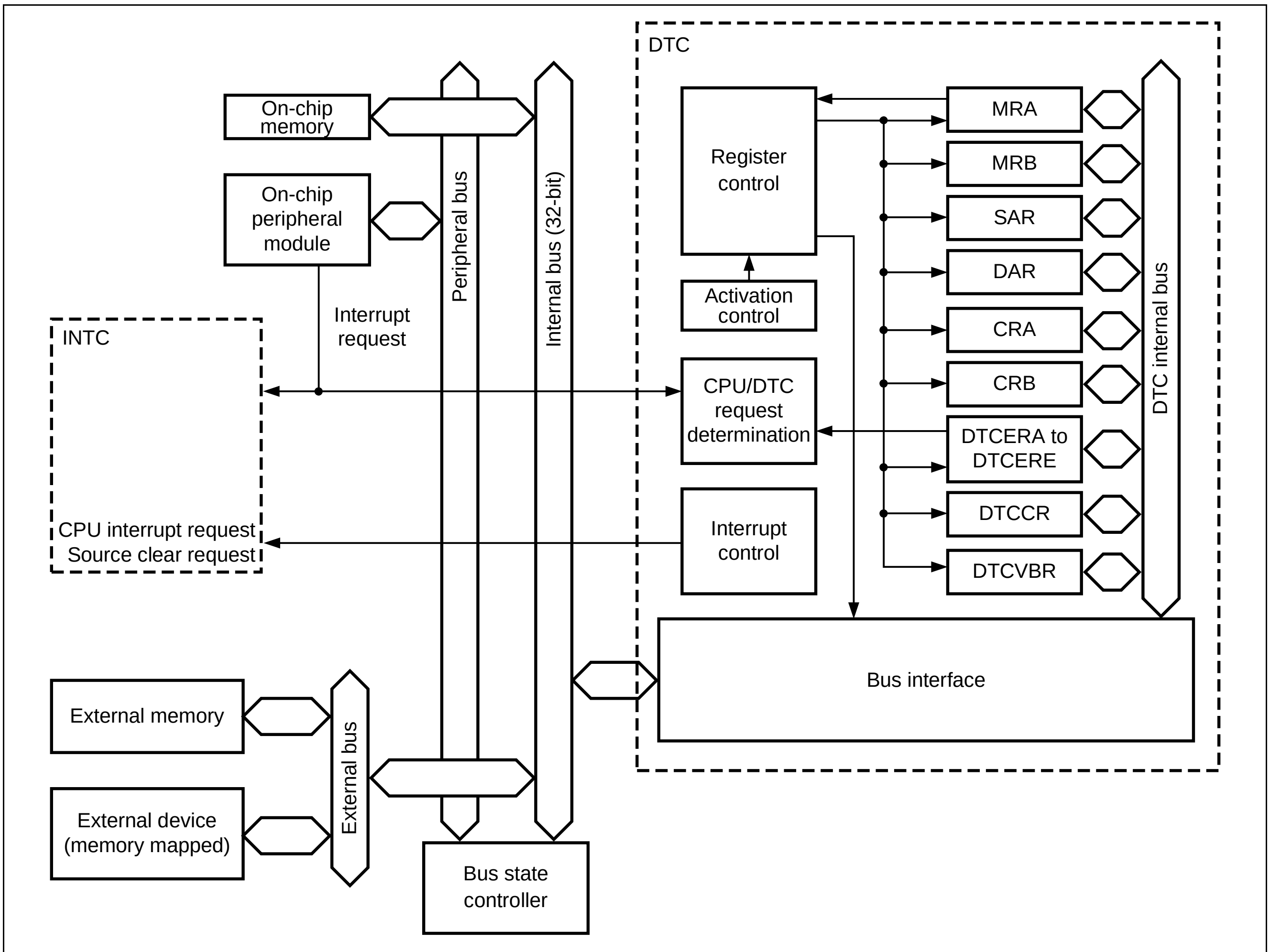
The transfer information is allocated in the data area.

For details of the DTC, see the Data Transfer Controller (DTC) section in the *SH7216 Group Hardware Manual* (rej09b0543).

Table 2 shows an overview of the DTC, and figure 2 is a block diagram of the DTC.

Table 2 DTC Overview

Item	Description
Transfer modes	Normal transfer mode, repeat transfer mode, block transfer mode
Transfer count	Normal transfer mode: 1 to 65,536 Repeat transfer mode: 1 to 256 Block transfer mode: 1 to 65,536
Data size	Selectable among byte, word, and longword
CPU interrupt requests	An interrupt request can be sent to the CPU after a single data transfer completes. An interrupt request can be sent to the CPU after the specified number of data transfers complete.
Activation sources	External pin, A/D, CMT, USB, MTU2, MTU2S, IIC3, SSU, SCI, SCIF
Other	Support for chain transfer (multiple data transfers triggered by a single activation source) Transfer information read skip mode setting Module stop mode setting Short address mode setting Selectable among three bus release timing settings Selectable among two DTC activation priority settings



Legend:
MRA, MRB: DTC mode registers A, B
SAR: DTC source address register
DAR: DTC destination address register
CRA, CRB: DTC transfer count registers A, B
DTCERA to DTCERE: DTC enable registers A to E
DTCCR: DTC control register
DTCVBR: DTC vector base register

Figure 2 DTC Block Diagram

(a) DTC Transfer Information Allocation

The transfer information is allocated within the data area. Use 4n as the transfer information start address. When an address other than 4n is specified, the bottom two bits are ignored when accessing the data area ([1:0] = B'00). Figure 3 illustrates the allocation of transfer information in the data area. Exclusively in cases when all transfer sources and transfer destinations for DTC transfers are located in the on-chip RAM and on-chip peripheral modules, the short address mode may be selected by setting to 1 the DTSA bit in the bus function extending register (BSCEHR).*[1]

Normally, reading the transfer information requires processing of 4 longwords, but this can be reduced to 3 longwords and the DTC activation time reduced by selecting short address mode.

Note: 1. See 9.4.8 Bus Function Extending Register (BSCEHR) in the Bus State Controller (BSC) section in the *SH7216 Group Hardware Manual* (rej09b0543).

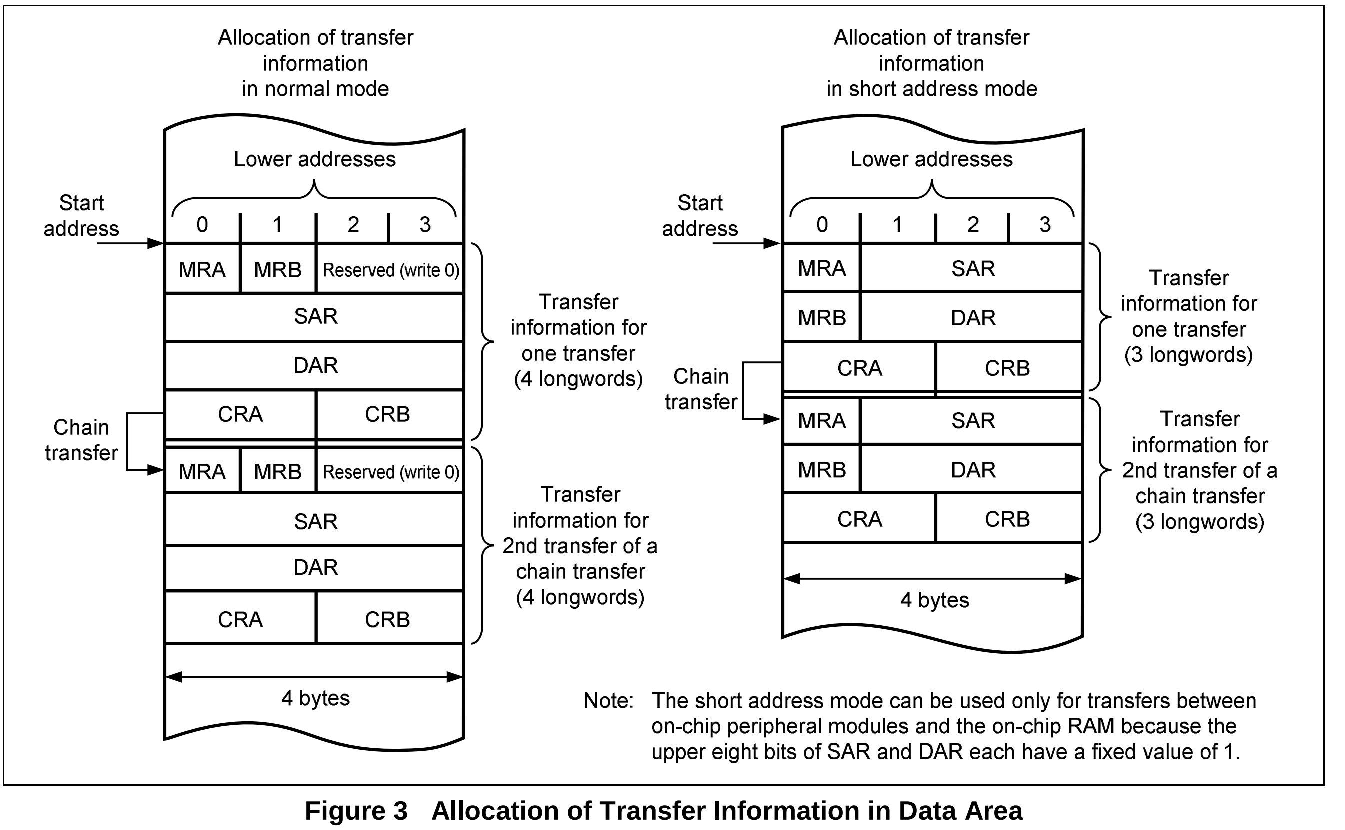


Figure 3 Allocation of Transfer Information in Data Area

(b) DTC Vector Table Allocation

- The DTC vector table is allocated in the RAM, so the address to be used as the vector base is set in the DTC vector base address register (DTCVBR).
- The start address of the transfer information is stored at the address pointed to by the DTC vector address offset.

For each activation source, the DTC reads the transfer information start address from the vector table and then reads the transfer information at that start address.

Figure 4 shows the correspondence between the DTC vector table and transfer information.

Table 3 lists the correspondences between the interrupt sources, DTC vector addresses, and DTCE Bits.

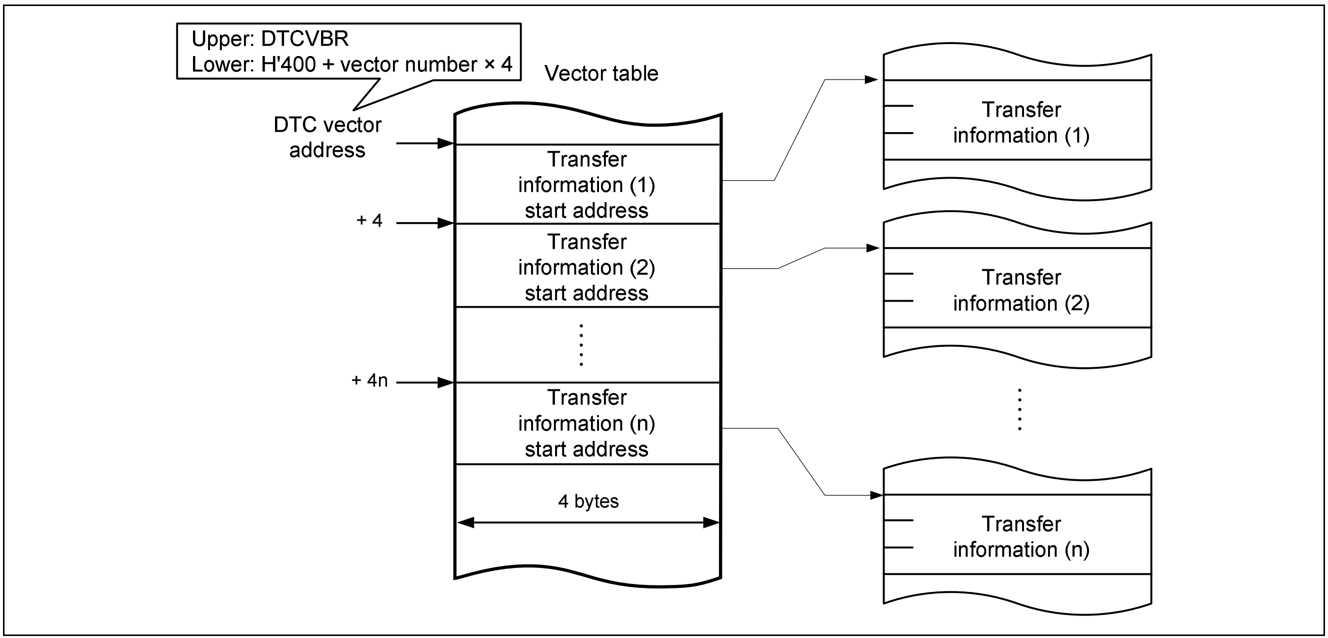


Figure 4 Correspondences between DTC Vector Table and Transfer Information

Table 3 Correspondences between Interrupt Sources, DTC Vector Addresses, and DTCE Bits

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*[1]
External pin	IRQ0	64	H'00000500	DTCERA15
	IRQ1	65	H'00000504	DTCERA14
	IRQ2	66	H'00000508	DTCERA13
	IRQ3	67	H'0000050C	DTCERA12
	IRQ4	68	H'00000510	DTCERA11
	IRQ5	69	H'00000514	DTCERA10
	IRQ6	70	H'00000518	DTCERA9
	IRQ7	71	H'0000051C	DTCERA8
A/D	ADI0	92	H'00000570	DTCERA7
	ADI1	96	H'00000580	DTCERA6
RCAN-ET	RM0_0	106	H'000005A8	DTCERA4
CMT	CMI0	140	H'00000630	DTCERA3
	CMI1	144	H'00000640	DTCERA2
USB	USBRXI1	150	H'00000658	DTCERE7
	USBTXI1	151	H'0000065C	DTCERE6
	USBRXI0	154	H'00000668	DTCERA1
	USBTXI0	155	H'0000066C	DTCERA0
MTU2_CH0	TGIA_0	156	H'00000670	DTCERB15
	TGIB_0	157	H'00000674	DTCERB14
	TGIC_0	158	H'00000678	DTCERB13
	TGID_0	159	H'0000067C	DTCERB12
MTU2_CH1	TGIA_1	164	H'00000690	DTCERB11
	TGIB_1	165	H'00000694	DTCERB10
MTU2_CH2	TGIA_2	172	H'000006B0	DTCERB9
	TGIB_2	173	H'000006B4	DTCERB8
MTU2_CH3	TGIA_3	180	H'000006D0	DTCERB7
	TGIB_3	181	H'000006D4	DTCERB6
	TGIC_3	182	H'000006D8	DTCERB5
	TGID_3	183	H'000006DC	DTCERB4
MTU2_CH4	TGIA_4	188	H'000006F0	DTCERB3
	TGIB_4	189	H'000006F4	DTCERB2
	TGIC_4	190	H'000006F8	DTCERB1
	TGID_4	191	H'000006FC	DTCERB0
	TCIV_4	192	H'00000700	DTCERC15
MTU2_CH5	TGIU_5	196	H'00000710	DTCERC14
	TGIV_5	197	H'00000714	DTCERC13
	TGIW_5	198	H'00000718	DTCERC12
MTU2S_CH3	TGIA_3S	204	H'00000730	DTCERC3
	TGIB_3S	205	H'00000734	DTCERC2
	TGIC_3S	206	H'00000738	DTCERC1
	TGID_3S	207	H'0000073C	DTCERC0
MTU2S_CH4	TGIA_4S	212	H'00000750	DTCERD15
	TGIB_4S	213	H'00000754	DTCERD14
	TGIC_4S	214	H'00000758	DTCERD13
	TGID_4S	215	H'0000075C	DTCERD12
	TCIV_4S	216	H'00000760	DTCERD11

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*[1]
MTU2S_CH5	TGIU_5S	220	H'00000770	DTCERD10
	TGIV_5S	221	H'00000774	DTCERD9
	TGIW_5S	222	H'00000778	DTCERD8
IIC3	RXI	230	H'00000798	DTCERD7
	TXI	231	H'0000079C	DTCERD6
RSPI	SPRI	234	H'000007A8	DTCERD5
	SPTI	235	H'000007Ac	DTCERD4
SCI4	RXI4	237	H'000007B4	DTCERD3
	TXI4	238	H'000007B8	DTCERD2
SCI0	RXI0	241	H'000007C4	DTCERE15
	TXI0	242	H'000007C8	DTCERE14
SCI1	RXI1	245	H'000007D4	DTCERE13
	TXI1	246	H'000007D8	DTCERE12
SCI2	RXI2	249	H'000007E4	DTCERE11
	TXI2	250	H'000007E8	DTCERE10
SCIF3	RXI3	254	H'000007F8	DTCERE9
	TXI3	255	H'000007FC	DTCERE8

Note: 1. DTCE bits with no corresponding interrupt are reserved. Always write 0 to these bits.

2.2 Sample Program Operation

Table 4 lists the settings for the sample program. Figure 5 illustrates the operation of the program.

Table 4 Sample Program Settings

Function	Item	Setting
DTC	Transfer mode	Normal mode
	Transfer count	64
	Transfer size	Longword
	DTC vector table	Allocated at H'FFF90000 (on-chip RAM)
	Transfer source area	On-chip flash memory
	Transfer destination area	On-chip RAM
	Transfer source addressing mode	SAR incremented after transfer
	Transfer destination addressing mode	DAR incremented after transfer
	Activation source	TGIA_0 of MTU2_CH0
	Interrupt handling	Interrupt to CPU after specified number of data transfers complete enabled
MTU2	Channel	CH0
	Function	Compare match output
	Timer count	Count at rising edge, clear at TGRA compare match, count on internal clock: Pϕ/64
	Operating mode	Normal operation (TGRA = H'0C35, output toggles every 4 ms) TIOC1A pin function: Initial output 0, output toggles at compare match
	Interrupt request	TGFA clear: Output compare flag A cleared

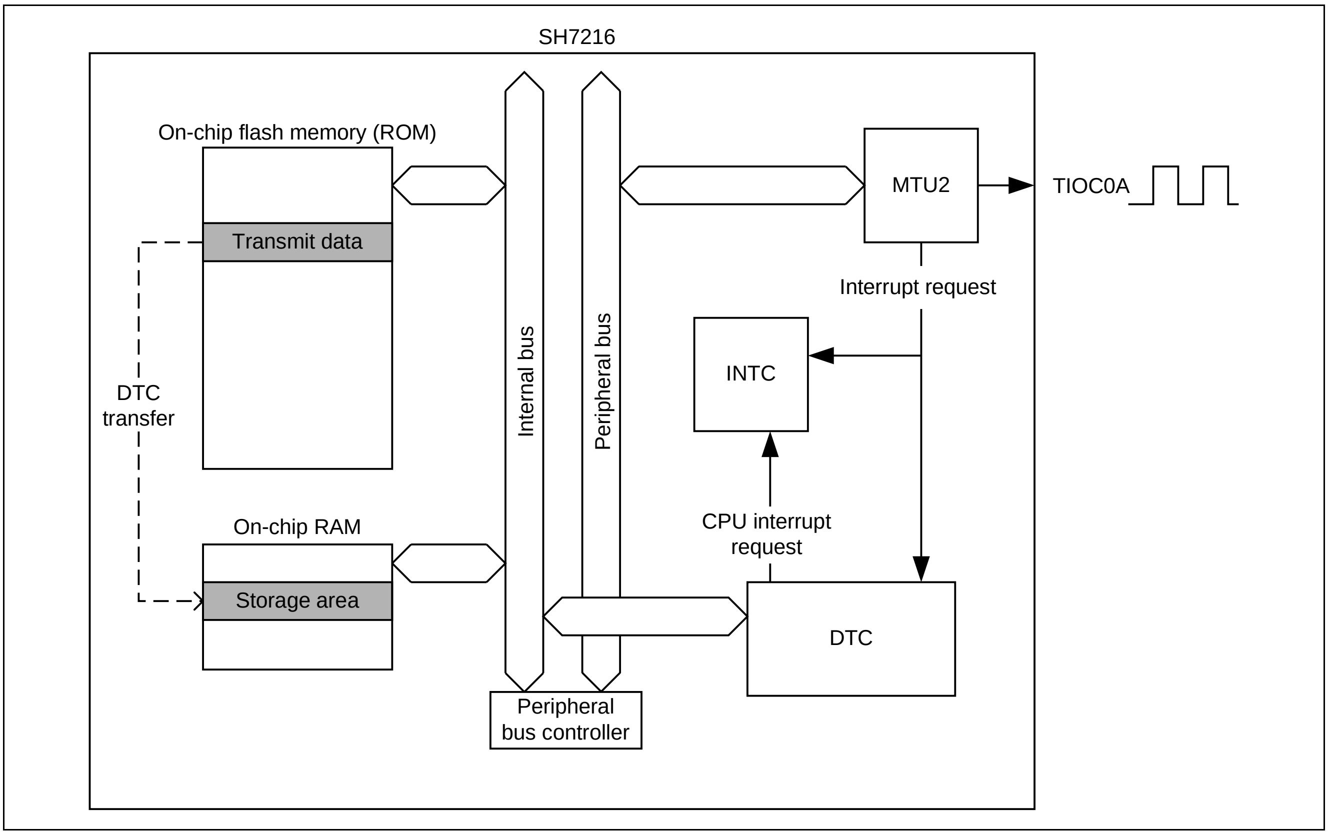


Figure 5 Illustration of Program Operation

2.3 Setting Procedure for Functions Used

The procedure for making initial settings for the functions used by the sample program is described below.

Figure 6 shows the initialization sequence for the DTC, and figure 7 shows the initialization sequence for MTU2.

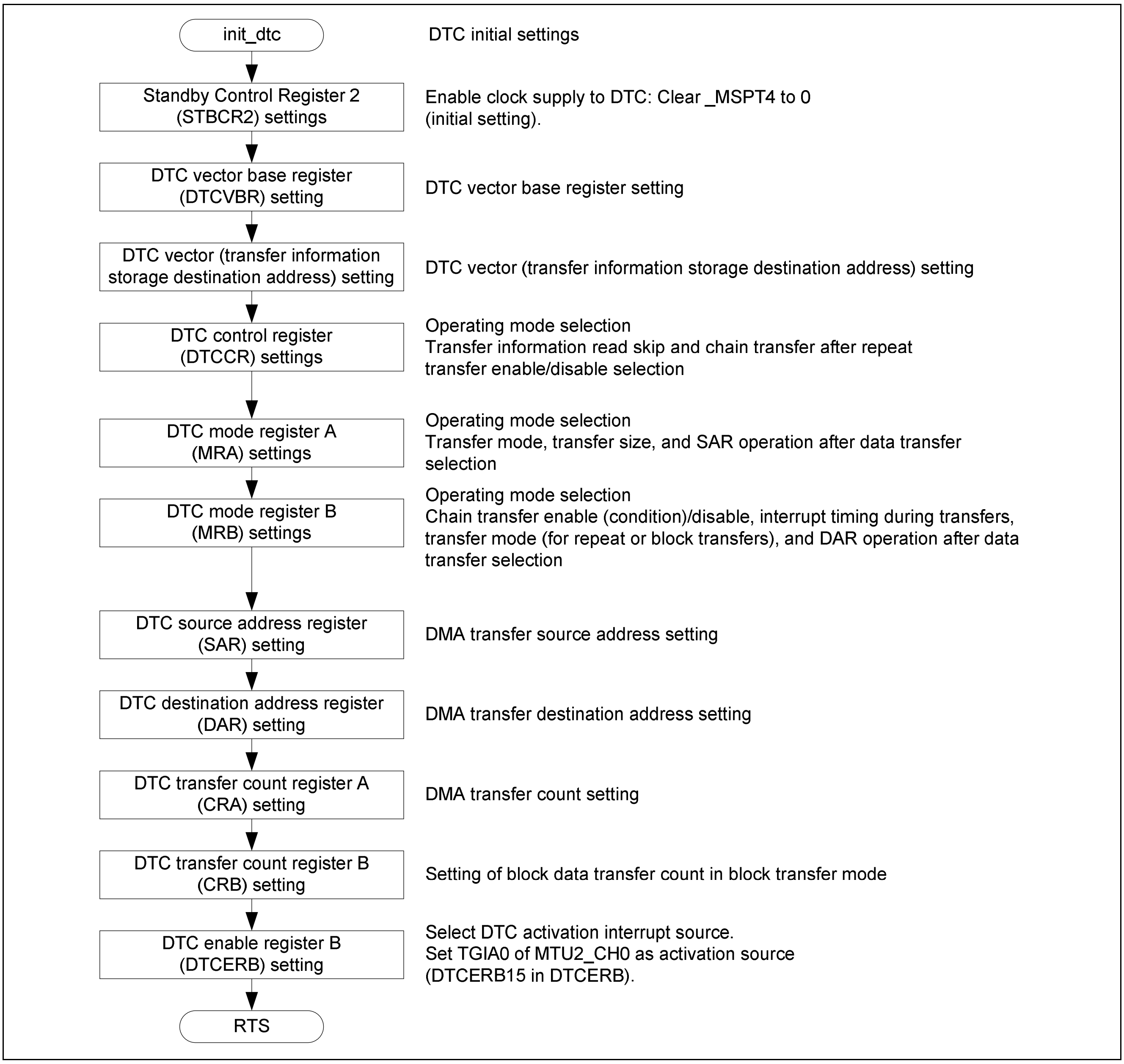


Figure 6 DTC Initialization Sequence

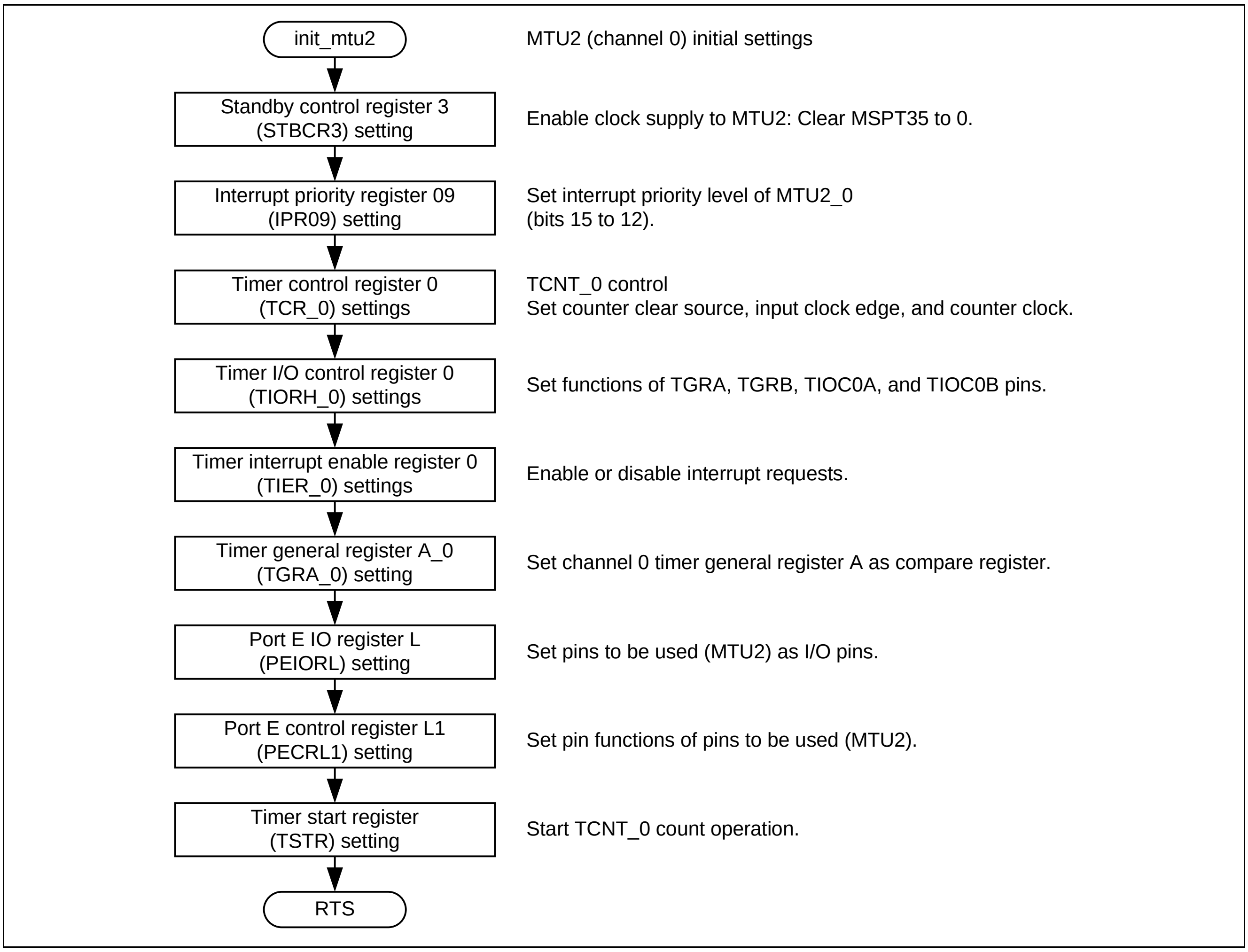


Figure 7 MTU2 Initialization Sequence

2.4 Register Settings for Sample Program

2.4.1 Clock Pulse Generator (CPG)

Table 5 lists the clock pulse generator settings.

Table 5 Clock Pulse Generator Settings

Register	Address	Setting value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC[2:0] = B'011: ×1/8 (Bϕ) IFC[2:0] = B'000: ×1/4 (Iϕ) PFC[2:0] = B'011: ×1/8 (Pϕ)

2.4.2 Power-Down Mode

Table 6 lists the standby control register (STBCR) settings.

Table 6 Standby Control Register Settings

Register	Address	Setting value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	Clear MSTP4 to 0: DMAC operates (initial value) Other bits: Initial values
Standby control register 3 (STBCR3)	H'FFFE0408	H'5E	Clear MSTP35 to 0: MTU2 operates Other bits: Initial values

2.4.3 Interrupt Controller (INTC)

Table 7 lists the interrupt priority register (IPR) settings.

Table 7 Interrupt Priority Register Settings

Register	Address	Setting value	Description
Interrupt priority register 09 (IPR09)	H'FFFE0C06	H'F000	Set MTU2_0 interrupt level to 15 (TGIA_0 to TGID_0).

2.4.4 Data Transfer Controller (DTC)

Table 8 lists the DTC register settings used in the sample program.

Table 8 DTC Register Settings

Register	Address	Setting value	Description
DTC control register (DTCCR)	H'FFFFCC90	H'00	RRS = 0: No transfer information read skip RCHNE = 0: Chain transfer after repeat transfer disabled ERR = 0: No interrupt request
DTC vector base register (DTCVBR)	H'FFFFCC94	H'FFF90000	DTC vector base address setting

DTC transfer information settings with TGIA0 as interrupt source

Register	Address	Setting value	Description
DTC mode register A (MRA)	H'FFF90800	H'28	MD[1:0] = B'00: Normal transfer mode Sz[1:0] = B'10: Longword transfer size SM[1:0] = B'10: SAR incremented after transfer
DTC mode register B (MRB)	H'FFF90801	H'08	CHNE = 0: Chain transfer disabled CHNS = 0: No effect because chain transfer disabled DISEL = 0: Interrupt request to CPU after specified number of transfers complete DTS = 0: No effect because normal transfer mode DM[1:0] = B'00: Fixed at DAR after transfer
DTC source address register (SAR)	H'FFF90804	—	Transfer source address setting Start address of data table (TR_DATA[]) allocated in on-chip flash memory
DTC destination address register (DAR)	H'FFF90808	H'FFF91000	Transfer destination address setting Start address of storage area (DTC_RX_ADD) in on-chip RAM
DTC transfer count register A (CRA)	H'FFF9080C	H'20	Transfer count setting 32
DTC transfer count register B (CRB)	H'FFF9080E	H'00	No effect because normal transfer mode
DTC enable register B (DTCERB)	H'FFFE6002	H'8000	Selection of interrupt source to activate DTC TGIA_0 of MTU2_CH0

2.4.5 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 9 lists the register settings for MTU2 (channel 0) used in the sample program.

Table 9 MTU2 (Channel 0) Register Settings

Register	Address	Setting value	Description
Timer control register 0 (TCR_0)	H'FFFE4300	H'23	CCLR[2:0] = B'001: Clear TCNT at TGRA compare match/input capture. CKEG[1:0] = B'00: Count at rising edge. TPSC[2:0] = B'011: Count on internal clock: Pϕ/64.
Timer I/O control register H_0 (TIORH_0)	H'FFFE4302	H'03	IOA[3:0] = B'0011 Set TGRA_0 as output compare register. Set TIOC0A pin to toggle output at compare match (initial output: 0).
Timer interrupt enable register 0 (TIER_0)	H'FFFE4304	H'01	TGIEA = 1: Interrupt requests (TGIA) triggered by TGFA bit enabled
Timer general register A_0 (TGRA_0)	H'FFFE4308	H'0C35	Toggle output every 4 ms (Pϕ: 50 MHz, TPSC: Pϕ/64).
Timer start register (TSTR)	H'FFFE4280	H'01	CST0 = 1: TCNT_0 performs count operation.

3. Reference Documents

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual
  SH7216 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.27.10	—	First edition issued
1.01	Jun.25.10	—	Modifications to source project due to change in FRQCR setting method

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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