SH7216 Group

Data Transfer Using MTU2 (Compare Match) as DMAC Activation Source

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Introduction

This application note presents an example of data transfer by the DMAC in which the MTU2 of the SH7216 is used as the activation source. The DMAC is activated with MTU2 compare match as the source and transfers data from the on-chip flash memory to the on-chip RAM.

Note that although the sample tasks and applications presented in this application note have been verified to work as intended, they should be checked in the actual operating environment before being put into actual use.

Target Device

SH7216

Contents

1. Introduction

1.1 Specifications

- Compare match on MTU2 channel 0 is used as the as the activation source for the DMAC.
- DMAC channel 0 is used to transfer data from the on-chip flash memory to the on-chip RAM.
- The cycle steal bus mode is used.

1.2 Functions Used

- Multi-function timer pulse unit 2 (MTU2), channel 0
- Direct memory access controller (DMAC), channel 0

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.06.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03.00, Release 00
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu –pic=1 –object="$(CONFIGDIR)¥$(FILELEAF).obj" -debug -gbr=auto –chgincpath –errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

2. Description of Sample Application

The sample application transfers data from the on-chip flash memory (ROM) to the on-chip RAM, using compare match on MTU2 (channel 0) as the source to activate the DMAC (channel 0).

2.1 Operation of Functions Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Multi-function timer pulse unit 2 (MTU2) is a multifunction timer unit that comprises six 16-bit timer channels. Each channel can be set to perform functions such as compare match and input capture. Channels 0 to 4 support waveform output using compare match, an input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clearing by compare match or input capture, simultaneous I/O to and from registers using synchronized counter operation, and up to 12-phase PWM output in combination with synchronous operation.

For details of the MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the *SH7216 Group Hardware Manual*.

Table 1 shows an outline of multi-function timer pulse unit 2 (MTU2). Figure 1 is a block diagram of MTU2.

Table 1 MTU2 Outline

Item	Description
Channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clocks	Selectable among eight counter input clocks for each channel (four counter input clocks for channel 5)
Operations of channels 0 to 5	• Waveform output using compare match, input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clearing by compare match or input capture • Simultaneous I/O to and from registers using synchronized counter operation, up to 12-phase PWM output in combination with synchronous operation.
A/D converter triggers	• Ability to generate A/D converter start triggers • Support for generation of interrupts at counter crest and trough as well as skipping of A/D converter start triggers in complementary PWM mode
Buffer operation	Support for register buffer settings for channels 0, 3, and 4
Operating modes	• PWM mode setting support for channels 0 to 4 • Independent phase counting mode setting support for channels 1 and 2 • Support for a total of six PWM waveform outputs consisting of three-phase positive and negative waveform outputs using complementary PWM mode or reset synchronous PWM mode and linked operation of channels 3 and 4
Interrupt requests	28 interrupt sources (compare match and input capture interrupts, etc.)
Other	• Operation with cascade connections • High-speed access via internal 16-bit bus • Automatic transfer of register data • Module standby mode • Dead time compensation counter function on channel 5

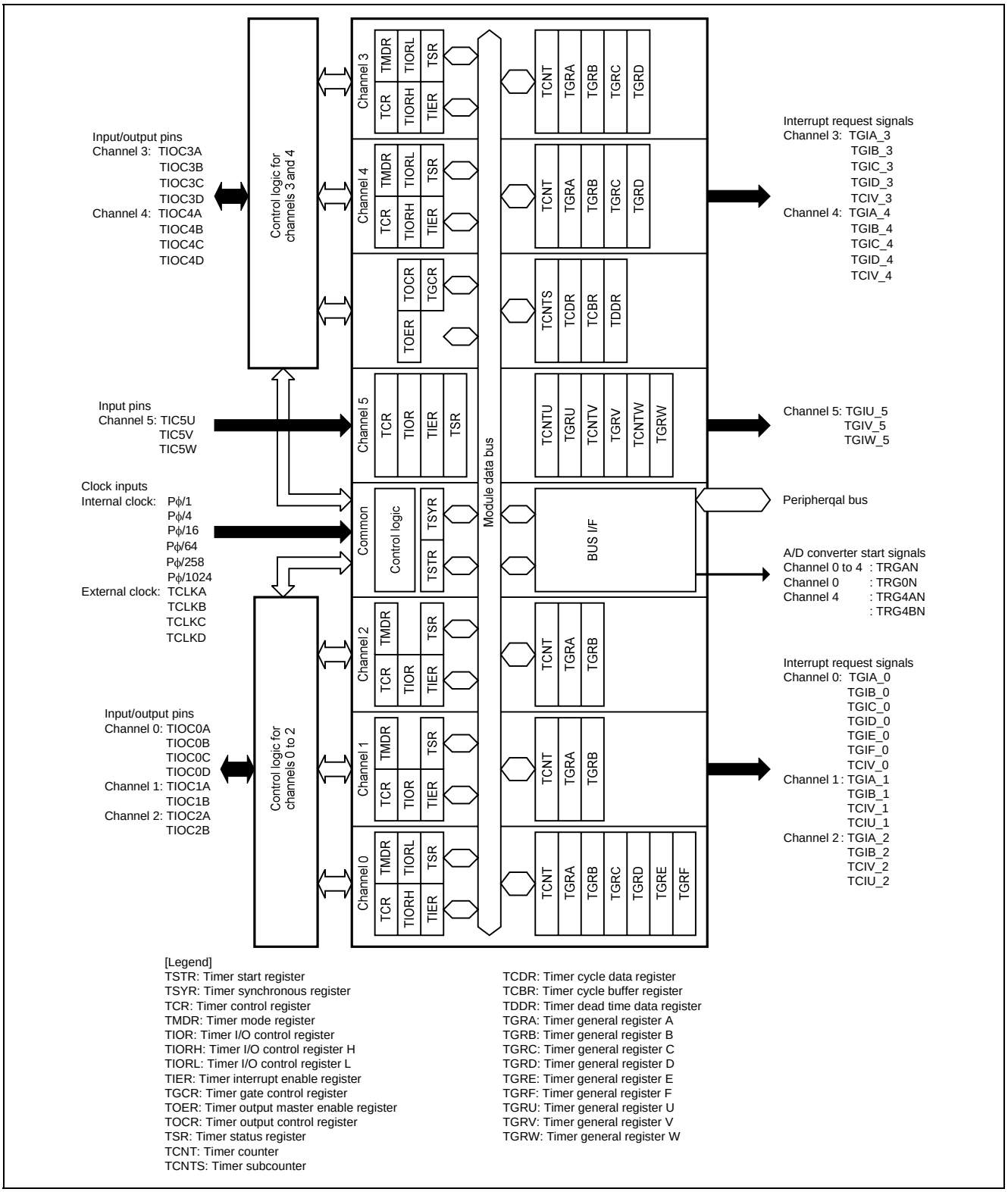


Figure 1 MTU2 Block Diagram

2.1.2 Direct Memory Access Controller (DMAC)

The DMAC of the SH7216 takes the place of the CPU to perform high-speed data transfers between external devices with DACK (transfer request acknowledge signal), external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral module.

The bus mode is selectable between cycle steal mode and burst mode.

For details of the DMAC, see the Direct Memory Access Controller (DMAC) section in the *SH7216 Group Hardware Manual*.

Table 2 shows an overview of the DMAC. Figure 2 shows an example of DMA transfer using cycle steal mode, and figure 3 shows an example of DMA transfer using burst mode. Figure 4 is a block diagram of the DMAC.

Table 2 DMAC Overview

Item	Description
Number of channels	8 channels: CH0 to CH7 External requests can be accepted on only four channels, CH0 to CH3.
Address space	4 GB
Transfer data length	Byte, word (2 bytes), longword (4 bytes), 16 bytes (longword × 4)
Max. transfer count	16,777,216 (24-bit) transfers
Addressing modes	Single address mode, dual address mode
Transfer requests	External request, on-chip peripheral module request, auto request (SCIF: 8 sources, I2C3: 2 sources, A/D converter: 1 source, MTU2: 5 sources, CMT: 2 sources)
Bus modes	Cycle steal mode (normal mode, intermittent mode), burst mode
Priority	Channel priority fixed mode, round-robin mode
Interrupt requests	Generation of interrupt request to CPU when data transfer half finished or at end of data transfer
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/ transfer end signal	Ability to set active level of DACK and TEND

In normal mode cycle steal operation, the DMAC releases bus mastership to another bus master each time transfer of a transfer unit (byte, word, longword, or 16-byte unit) completes. When the next transfer request occurs, the DMAC takes back bus mastership from another bus master, transfers another transfer unit, and again releases bus mastership to another master when the transfer completes. This process is repeated until the transfer end condition is satisfied. Normal mode cycle steal operation can be used for any transfer category, regardless of the transfer request source, transfer source, or transfer destination.

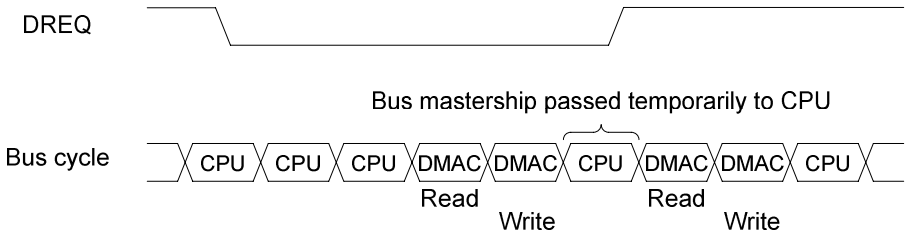


Figure 2 Example of DMA Transfer Using Cycle Steal Mode (Dual Address, DREQ Low Level Detection)

In burst mode, once the DMAC obtains bus mastership it performs data transfer continuously, not releasing bus mastership until the transfer end condition is satisfied. However, in external request mode when DREQ level detection is enabled and DREQ is not at the active level, the DMAC releases bus mastership to another bus master after all DMAC transfers for which requests have been received have completed, even if the transfer end condition has not been satisfied.

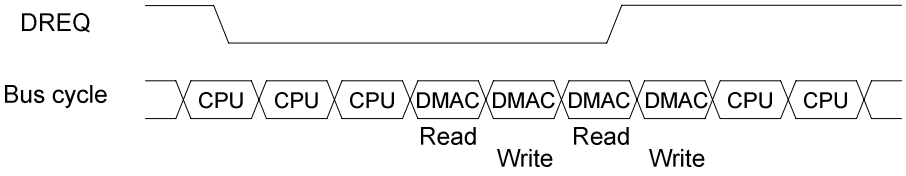
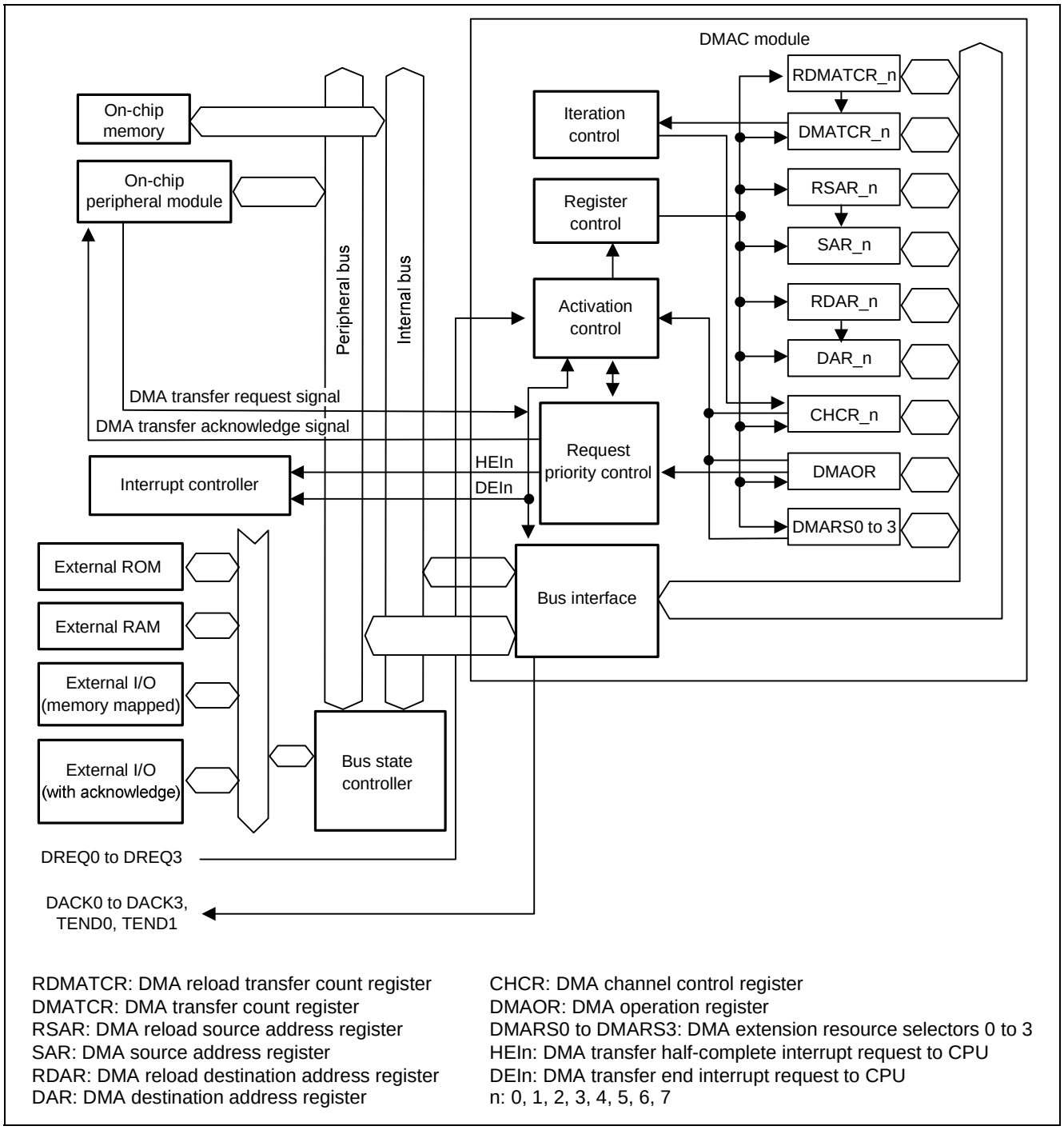


Figure 3 Example of DMA Transfer Using Burst Mode (Dual Address, DREQ Low Level Detection)



RDMATCR: DMA reload transfer count register
DMATCR: DMA transfer count register
RSAR: DMA reload source address register
SAR: DMA source address register
RDAR: DMA reload destination address register
DAR: DMA destination address register
CHCR: DMA channel control register
DMAOR: DMA operation register
DMARS0 to DMARS3: DMA extension resource selectors 0 to 3
HEIn: DMA transfer half-complete interrupt request to CPU
DEIn: DMA transfer end interrupt request to CPU
n: 0, 1, 2, 3, 4, 5, 6, 7

Figure 4 Block Diagram of DMAC

2.2 Sample Program Operation

Table 3 lists the settings for the sample program. Figure 5 illustrates the operation of the program.

Table 3 Sample Program Settings

Function	Item	Setting
MTU2	Channel	CH0
	Function	Compare match output
	Timer count	Count at rising edge, clear at TGRA compare match, count on internal clock: Pϕ/64
	Operating mode	Normal operation (TGRA = H'0C35, output toggles every 4 ms) TIOC1A pin function: Initial output 0, output toggles at compare match
	Interrupt request	TGFA clear: Output compare flag A cleared
DMAC	Channel	CH0
	Transfer data length	16 bytes
	Transfer count	4 transfers (4 × 16-byte data length = 64 bytes of data)
	Transfer source address	&(DMA_TR_DATA[0]) (on-chip flash memory)
	Transfer destination address	DMA_RX_ADD (on-chip RAM)
	Addressing mode	Dual address mode
	Bus mode	Cycle steal mode
	Priority	Fixed channel priority mode
	Interrupt request	DMAC stops when data transfer ends

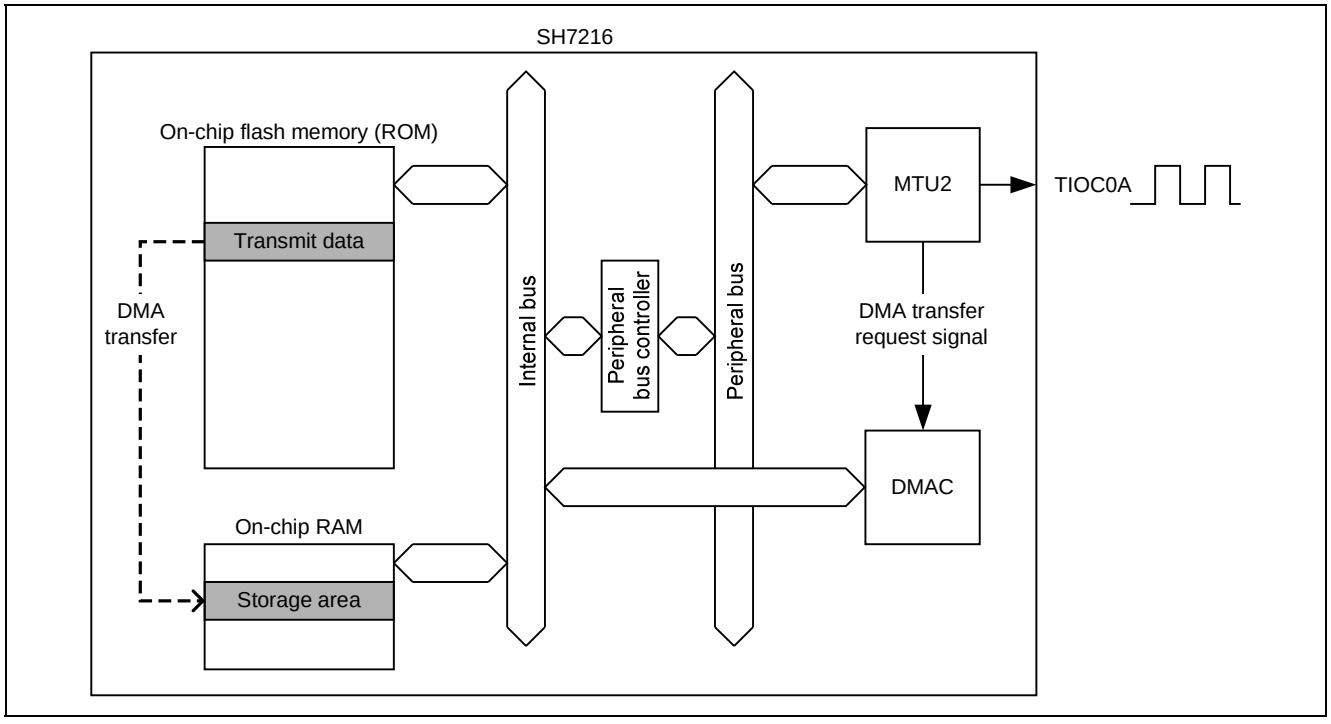


Figure 5 Illustration of Program Operation

2.3 Setting Procedure for Functions Used

The procedure for making initial settings for the functions used by the sample program is described below.

Figure 6 shows the initialization sequence for the DMAC (channel 0), and figure 7 shows the initialization sequence for MTU2 (channel 0).

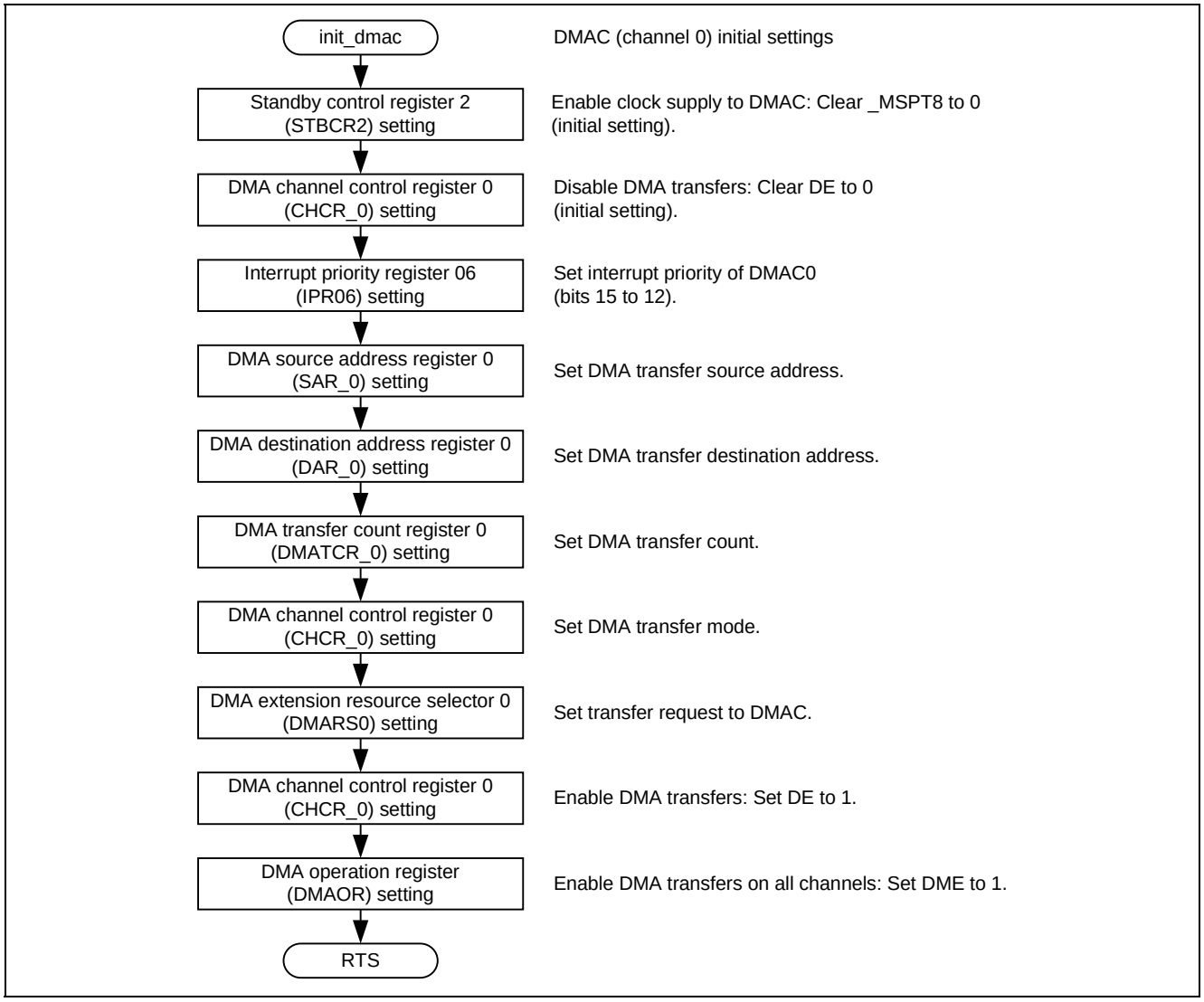


Figure 6 DMAC (Channel 0) Initialization Sequence

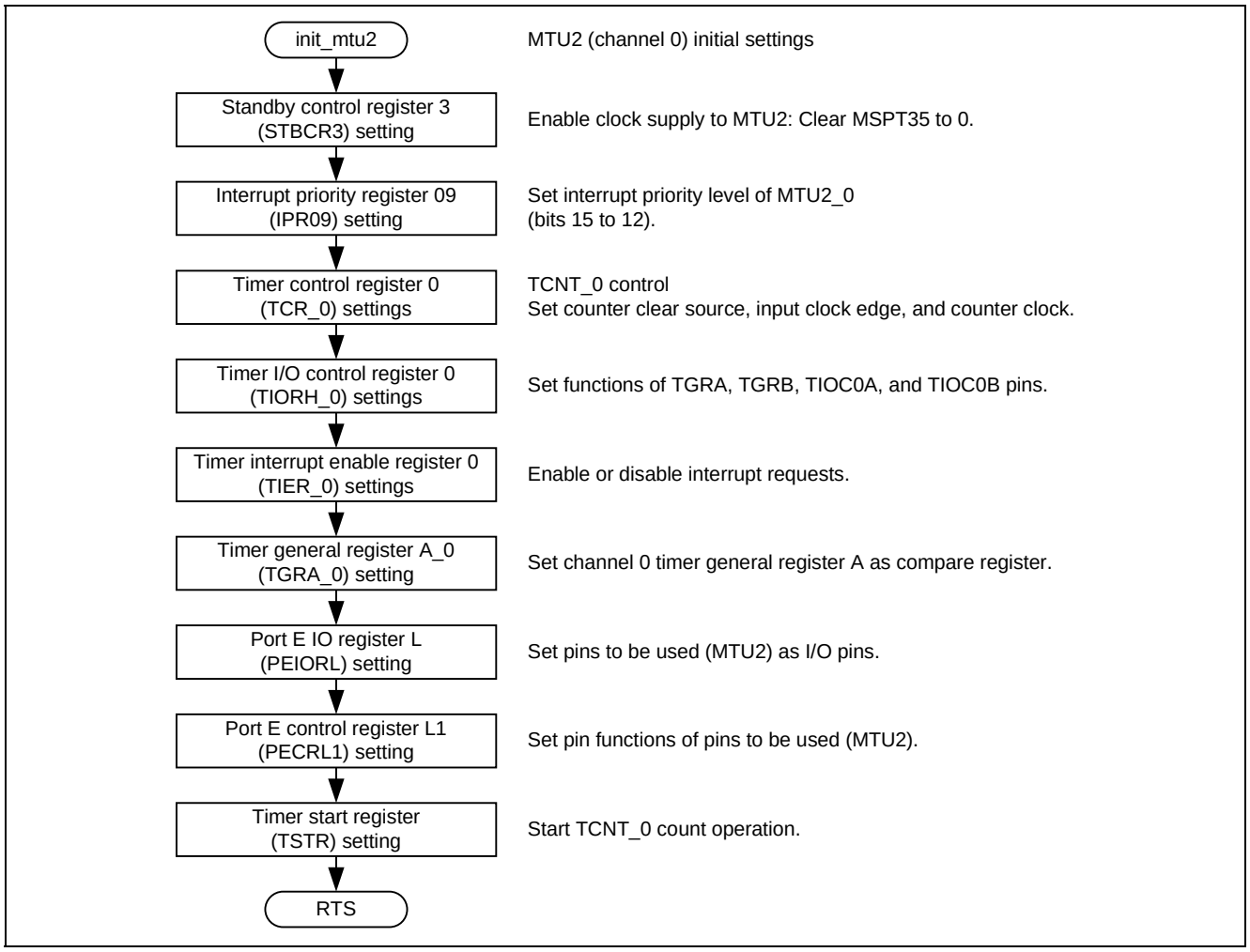


Figure 7 MTU2 Initialization Sequence

2.4 Register Settings for Sample Program

2.4.1 Clock Pulse Generator (CPG)

Table 4 lists the clock pulse generator settings.

Table 4 Clock Pulse Generator Settings

Register	Address	Setting value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC[2:0] = B'011: ×1/8 (Bϕ) IFC[2:0] = B'000: ×1/4 (Iϕ) PFC[2:0] = B'011: ×1/8 (Pϕ)

2.4.2 Power-Down Mode

Table 5 lists the standby control register (STBCR) settings.

Table 5 Standby Control Register Settings

Register	Address	Setting value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	Clear MSTP8 to 0: DMAC operates (initial value) Other bits: Initial values
Standby control register 3 (STBCR3)	H'FFFE0408	H'5E	Clear MSTP35 to 0: MTU2 operates Other bits: Initial values

2.4.3 Interrupt Controller (INTC)

Table 6 lists the interrupt priority register (IPR) settings.

Table 6 Interrupt Priority Register Settings

Register	Address	Setting value	Description
Interrupt priority register 06 (IPR06)	H'FFFE0C00	H'F000	Set DMAC0 interrupt level to 15.
Interrupt priority register 09 (IPR09)	H'FFFE0C06	H'F000	Set MTU2_0 interrupt level to 15 (TGIA_0 to TGID_0).

2.4.4 Direct Memory Access Controller (DMAC)

Table 7 lists the register settings for DMAC (channel 0).

Table 7 DMAC (Channel 0) Register Settings

Register	Address	Setting value	Description
DMA source address register 0 (SAR_0)	H'FFFE1000	—	Set the start address of the character string in on-chip flash memory as the DMA transfer source address (&(DMA_TR_DATA[0])).
DMA destination address register 0 (DAR_0)	H'FFFE1004	H'FFF88000	Set the on-chip RAM area as the DMA transfer destination address (DMA_RX_ADD).
DMA transfer count register 0 (DMATCR_0)	H'FFFE1008	H'00000004	Set the DMA transfer count to 4. (Set the single transfer size in CHCR_0.)
DMA channel control register 0 (CHCR_0)	H'FFFE100C	H'8000581C	TC = 1: Number of transfers per transfer request is count set in DMATCR. RLD = 0: Reload function disabled (initial value) DM[1:0] = B'01: Increment destination address (+16 when transferring 16-byte units) SM[1:0] = B'01: Increment source address (+16 when transferring 16-byte units) RS[3:0] = B'1000: DMA extension resource selector TB = 0: Cycle steal mode (initial value) TS[1:0] = B'11: Transfer unit set to 16 bytes (4 longwords) IE = 1: Interrupt requests enabled TE: Clear to 0 at DMA transfer end interrupt. DE: Before DMAC initial settings, clear to 0 to disable DMA transfers (initial value). After DMAC initial settings, set to 1 to enable DMA transfers. Clear to 0 to disable DMA transfers at DMA transfer end interrupt.
DMA operation register (DMAOR)	H'FFFE1200	—	DME: After DMAC initial settings, set to 1 to enable DMA transfers on all channels. Clear to 0 to disable DMA transfers on all channels at DMA transfer end interrupt.
DMA extension resource selector 0 (DMARS0)	H'FFFE1300	H'00E3	Set MTU2 (TGIA_0) as activation source for channel 0.

2.4.5 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 8 lists the register settings for MTU2 (channel 0) used in the sample program.

Table 8 MTU2 (Channel 0) Register Settings

Register	Address	Setting value	Description
Timer control register 0 (TCR_0)	H'FFFE4300	H'23	CCLR[2:0] = B'001: Clear TCNT at TGRA compare match/input capture. CKEG[1:0] = B'00: Count at rising edge. TPSC[2:0] = B'011: Count on internal clock: Pϕ/64.
Timer I/O control register H_0 (TIORH_0)	H'FFFE4302	H'03	IOA[3:0] = B'0011 Set TGRA_0 as output compare register. Set TIOC0A pin to toggle output at compare match (initial output: 0).
Timer interrupt enable register 0 (TIER_0)	H'FFFE4304	H'01	TGIEA = 1: Interrupt requests (TGIA) triggered by TGFA bit enabled
Timer general register A_0 (TGRA_0)	H'FFFE4308	H'0C35	Toggle output every 4 ms (Pϕ: 50 MHz, TPSC: Pϕ/64).
Timer start register (TSTR)	H'FFFE4280	H'01	CST0 = 1: TCNT_0 performs count operation.
Timer status register 0 (TSR_0)	H'FFFE4305	—	TGFA: Set to 0 in MTU2 (channel 0) compare match interrupt handler.

3. Reference Documents

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual
  SH7216 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.27.10	—	First edition issued
1.01	Jun.25.10	—	Modifications to source project due to change in FRQCR setting method

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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