

## SH7216 Group

R01AN0293EJ0210

Rev.2.10

## Using RSPI to Reprogram Flash Memory in User Program Mode

Feb 28, 2011

### Introduction

In the sample application, the user program mode of the SH7216 is used to reprogram the on-chip flash memory. The data used to program the on-chip flash is stored in an external device connected to the SH7216, and the Renesas serial peripheral interface (RSPI) is used for data transfer.

The program used to reprogram the on-chip flash in the sample application is located in the user MAT of the SH7216. The simple flash API (standard API) for the SH-2 and SH-2A, supplied by Renesas Electronics, is used to reprogram the on-chip flash.

### Target Device

SH7216

### Contents

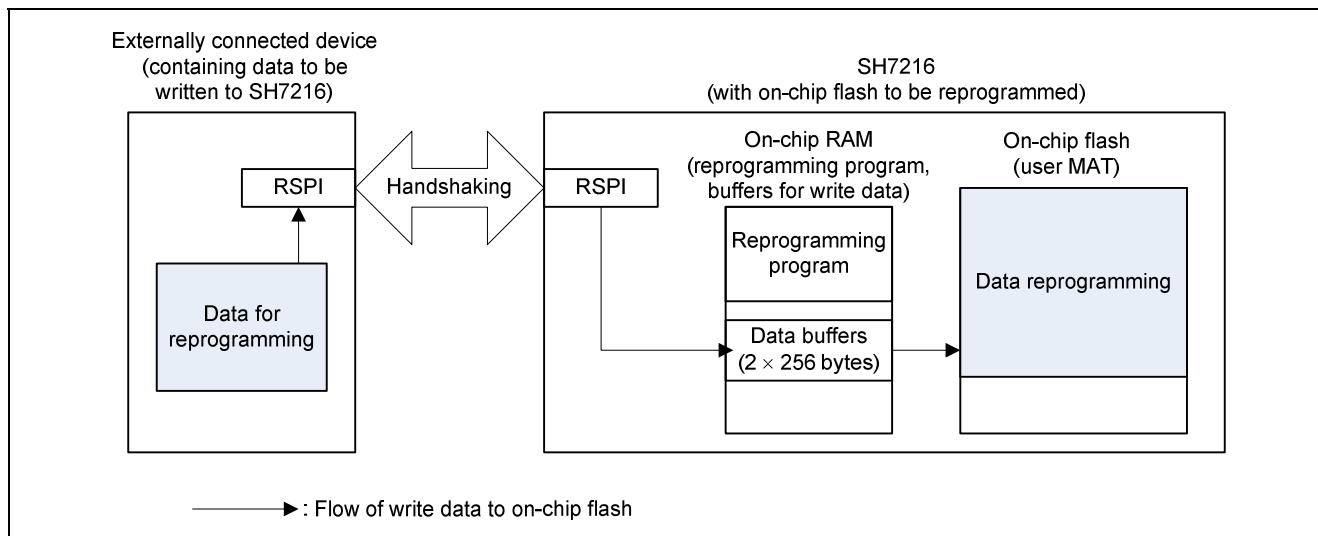
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## 1. Introduction

In the sample application, the SH7216 receives data from a connected external device and reprograms the on-chip flash in user program mode.

### 1.1 Specifications

Figure 1 shows a system overview of the sample application.



**Figure 1 System Configuration**

- The SH7216 operating mode is user program mode.
- The data to be written to the SH7216 is stored in the external device.
- The SH7216 and external device are connected by the RSPI, via which handshaking and transfer of write data take place.
- The SH7216 executes a program in on-chip RAM during reprogramming of the on-chip flash.
- The SH7216 has two data buffer areas (256 bytes each), which are used in parallel for writing to the on-chip flash and for downloading data.
- A user-specified erasure area is erased according to instructions from the external device.
- Data is written to a user-specified address according to instructions from the external device.
- A standard API supplied by Renesas Electronics is used to program and erase the on-chip flash.

**Table 1 SH7216 Mode Pin Settings**

| Mode              | Pin Settings |     |     |
|-------------------|--------------|-----|-----|
|                   | FWE          | MD1 | MD0 |
| User program mode | 1            | 1   | 0   |

### 1.2 Functions Used

- Renesas serial peripheral interface (RSPI)
- Dedicated sequencer for on-chip flash (FCU)

### 1.3 Applicable Conditions

|                                    |  |
|------------------------------------|--|
| MCU                                | SH7216   |
| Operating frequency                | Internal clock: 200 MHz  |
|                                    | Bus clock: 50 MHz  |
|                                    | Peripheral clock: 50 MHz   |
|                                    | MTU2S clock: 100 MHz   |
|                                    | AD clock: 50 MHz   |
| Integrated development environment | Renesas Electronics High-performance Embedded Workshop,<br>Ver. 4.07.00  |
| C compiler                         | Renesas Electronics SuperH RISC engine Family<br>C/C++ Compiler Package, Ver. 9.03.00, Release 02  |
| Compile options                    | High-performance Embedded Workshop default settings<br>(-cpu=sh2afpu -pic=1 -object="\$(CONFIGDIR)\\$(FILELEAF).obj"<br>-debug -gbr=auto -chgincpath -errorpath -global_volatile=0<br>-opt_range=all -infinite_loop=0 -del_vacant_loop=0<br>-struct_alloc=1 -nologo) |

### 1.4 Related Application Notes

The following application note is related to this application note. Refer to it as necessary in conjunction with this application note.

SH Family: Simple Flash API for SH-2 and SH-2A

## 2. Overview and Functions

In the sample application, the SH7216 and external device are connected by the RSPI. In addition, a dedicated sequencer (FCU) is used on the SH7216 to program and erase the on-chip flash.

### 2.1 Description of Functions Used

#### 2.1.1 Renesas Serial Peripheral Interface (RSPI) Functions

The RSPI is a module that supports full-duplex synchronous serial communication. It enables high-speed serial communication with multiple processors and peripheral devices. In the sample application, the RSPI is used for handshake communication and transfer of data for reprogramming the on-chip flash between the SH7216 and the external device.

Figure 2 is a block diagram of the RSPI.

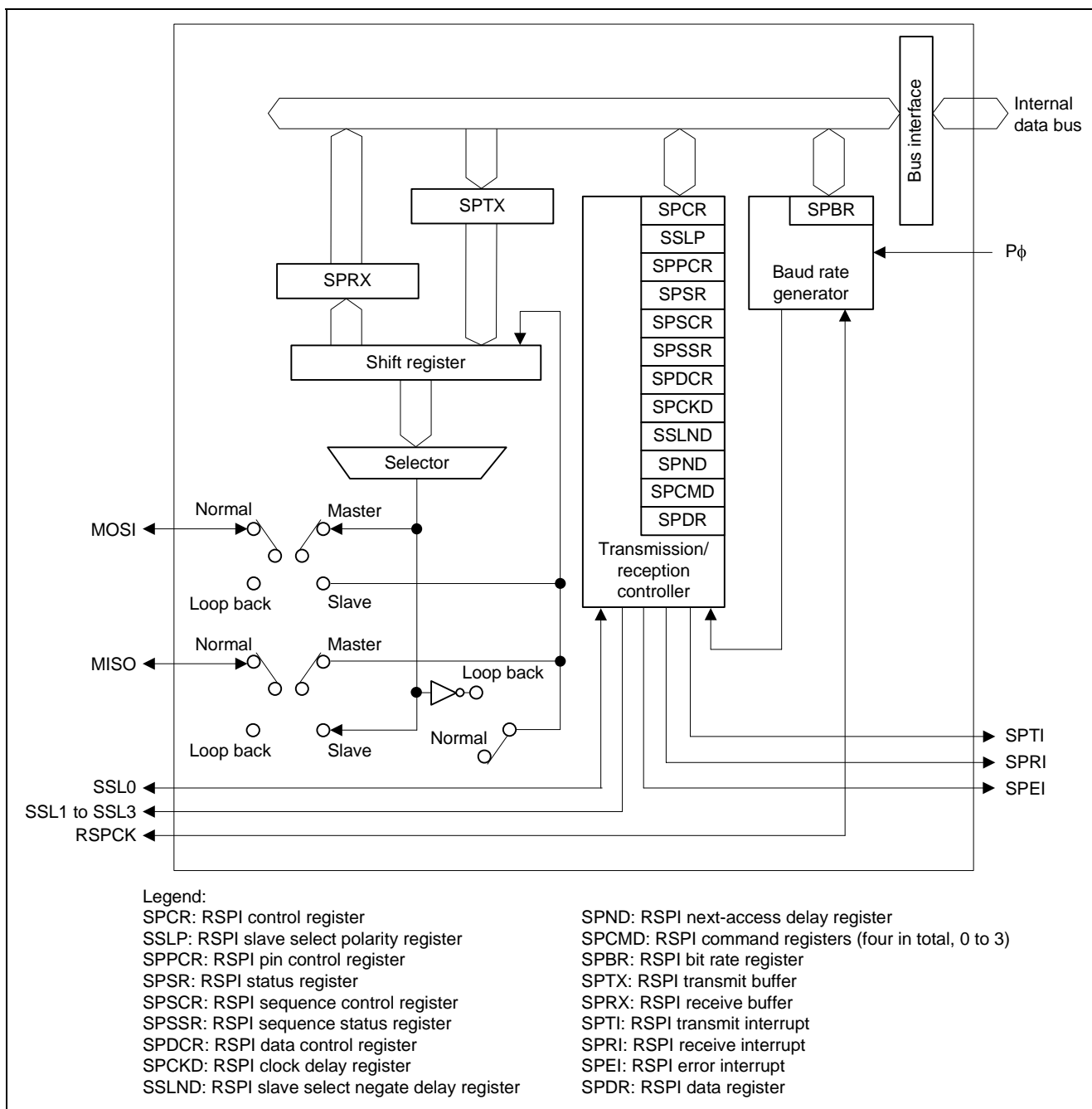


Figure 2 Block Diagram of RSPI

### 2.1.2 On-Chip Flash Dedicated Sequencer (FCU) Functions

The SH7216 uses the FCU to reprogram the on-chip flash.

Figure 3 is a block diagram of the on-chip flash.

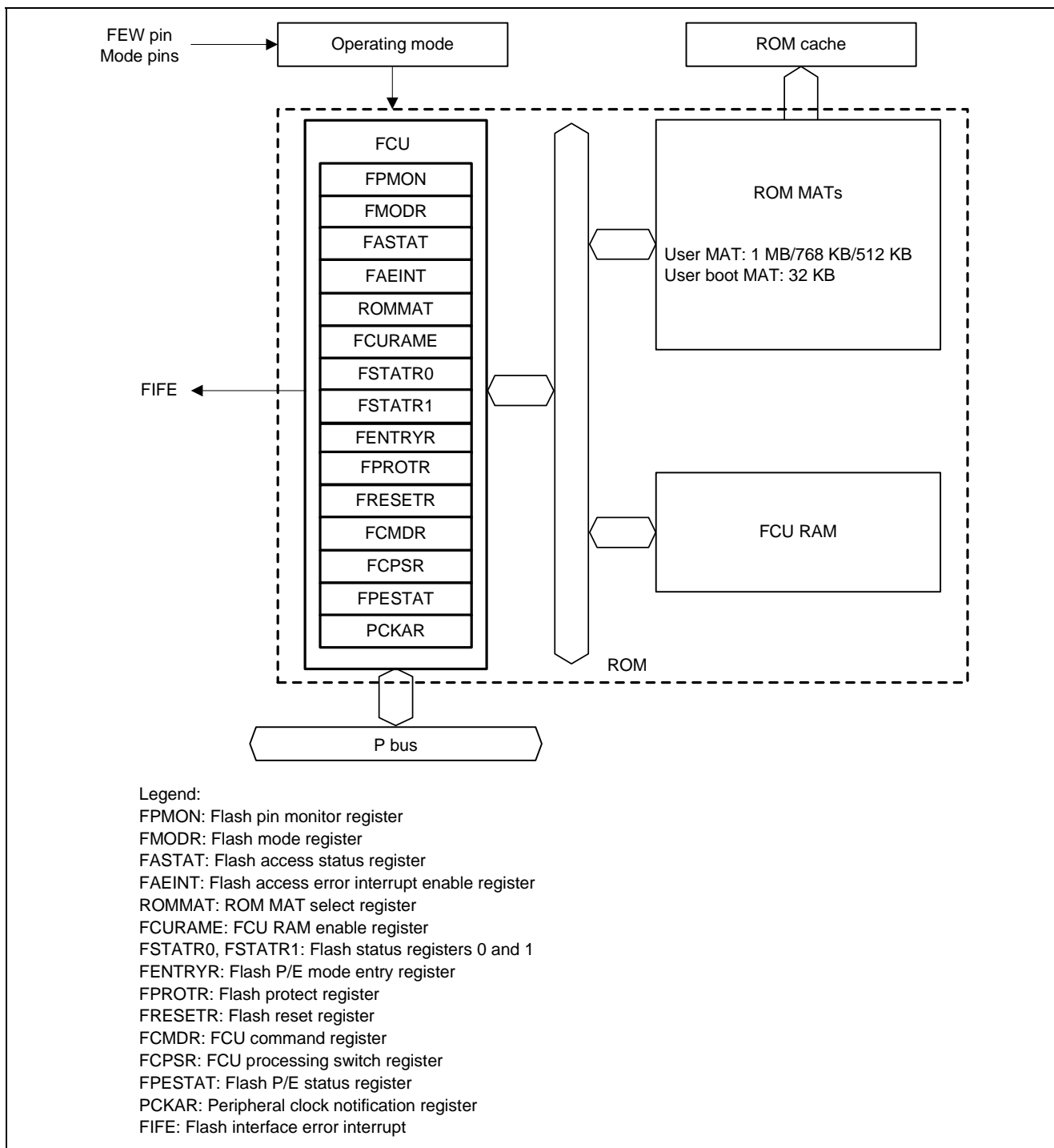


Figure 3 Block Diagram of On-Chip Flash

## 2.2 On-Chip Flash Programming/Erasing Operation

The SH7216 uses the FCU to program and erase the on-chip flash. The procedure for reprogramming the on-chip flash is described below. For a more detailed explanation, see *SH7216 Hardware Manual*. Note that the sample application uses the standard API to program and erase the on-chip flash. For details of the standard API, see the related application note.

### 2.2.1 Preparation for On-Chip Flash Programming/Erasing

In order to use the FCU, the FCU firmware must be stored in the FCU RAM. After the FCU firmware has been transferred, the FCU can be used to program or erase the on-chip flash by issuing FCU commands to it.

The FCU firmware is stored in the FCU firmware area of the device, and it must be transferred to the FCU RAM at startup. In addition, FCU RAM access is disabled at device startup, so access must be enabled by making the appropriate register setting.

### 2.2.2 On-Chip Flash Erasing

On the SH7216, the on-chip flash is divided into multiple blocks, and erasing is performed in block units. After the FCU firmware has been transferred, the FCU performs a block erase when an erase command\*<sup>1</sup> and an execute command are written to the address of the erasure target block.

Figure 4 shows the division of the SH7216 erasure blocks, and table 2 lists the addresses of the individual blocks.

Note: 1. The erase command may be written to any valid program/erase address in the on-chip flash.

| Program/erase address | On-chip flash<br>(user MAT) | Erasure block |
|-----------------------|-----------------------------|---------------|
| H'8080_0000           | 8 KB × 8                    | EB00          |
| ⋮                     |                             | ⋮             |
| H'8080_FFFF           | 64 KB × 9                   | EB07          |
| H'8081_0000           |                             | EB08          |
| ⋮                     |                             | ⋮             |
| H'8089_FFFF           | 128 KB × 3                  | EB16          |
| H'808A_0000           |                             | EB17          |
| ⋮                     | ⋮                           | ⋮             |
| H'808F_FFFF           |                             | EB19          |

Figure 4 Division of On-Chip Flash Erasure Blocks

**Table 2 Erasure Blocks and Addresses**

| Erasure block | Actual address             | Program/erase address      | Unit capacity |
|---------------|----------------------------|----------------------------|---------------|
| EB00          | H'0000_0000 to H'0000_1FFF | H'8080_0000 to H'8080_1FFF | 8 KB          |
| EB01          | H'0000_2000 to H'0000_3FFF | H'8080_2000 to H'8080_3FFF |               |
| EB02          | H'0000_4000 to H'0000_5FFF | H'8080_4000 to H'8080_5FFF |               |
| EB03          | H'0000_6000 to H'0000_7FFF | H'8080_6000 to H'8080_7FFF |               |
| EB04          | H'0000_8000 to H'0000_9FFF | H'8080_8000 to H'8080_9FFF |               |
| EB05          | H'0000_A000 to H'0000_BFFF | H'8080_A000 to H'8080_BFFF |               |
| EB06          | H'0000_C000 to H'0000_DFFF | H'8080_C000 to H'8080_DFFF |               |
| EB07          | H'0000_E000 to H'0000_FFFF | H'8080_E000 to H'8080_FFFF |               |
| EB08          | H'0001_0000 to H'0001_FFFF | H'8081_0000 to H'8081_FFFF | 64 KB         |
| EB09          | H'0002_0000 to H'0002_FFFF | H'8082_0000 to H'8082_FFFF |               |
| EB10          | H'0003_0000 to H'0003_FFFF | H'8083_0000 to H'8083_FFFF |               |
| EB11          | H'0004_0000 to H'0004_FFFF | H'8084_0000 to H'8084_FFFF |               |
| EB12          | H'0005_0000 to H'0005_FFFF | H'8085_0000 to H'8085_FFFF |               |
| EB13          | H'0006_0000 to H'0006_FFFF | H'8086_0000 to H'8086_FFFF |               |
| EB14          | H'0007_0000 to H'0007_FFFF | H'8087_0000 to H'8087_FFFF |               |
| EB15          | H'0008_0000 to H'0008_FFFF | H'8088_0000 to H'8088_FFFF |               |
| EB16          | H'0009_0000 to H'0009_FFFF | H'8089_0000 to H'8089_FFFF | 128 KB        |
| EB17          | H'000A_0000 to H'000B_FFFF | H'808A_0000 to H'808B_FFFF |               |
| EB18          | H'000C_0000 to H'000D_FFFF | H'808C_0000 to H'808D_FFFF |               |
| EB19          | H'000E_0000 to H'000F_FFFF | H'808E_0000 to H'808F_FFFF |               |

### 2.2.3 On-Chip Flash Programming

Programming of the on-chip flash can only take place when the target area is in the erased state. A single write to the user MAT comprises a 256-byte unit of data. As with erasing, the programming procedure consists of issuing a command to the FCU, after which the FCU performs the operation. A write command and the write size\*<sup>1</sup> are issued to the program/erase address, followed by writing\*<sup>2</sup> the write data (256 bytes) to the write destination address.\*<sup>3</sup>

- Notes:
1. The write size is fixed at 256 bytes when writing to the user MAT and user boot MAT (issue H'80 as the size).
  2. The write data is written to the program/erase address in word size.
  3. This address (the program/erase address) is the write address plus H'8080\_0000.

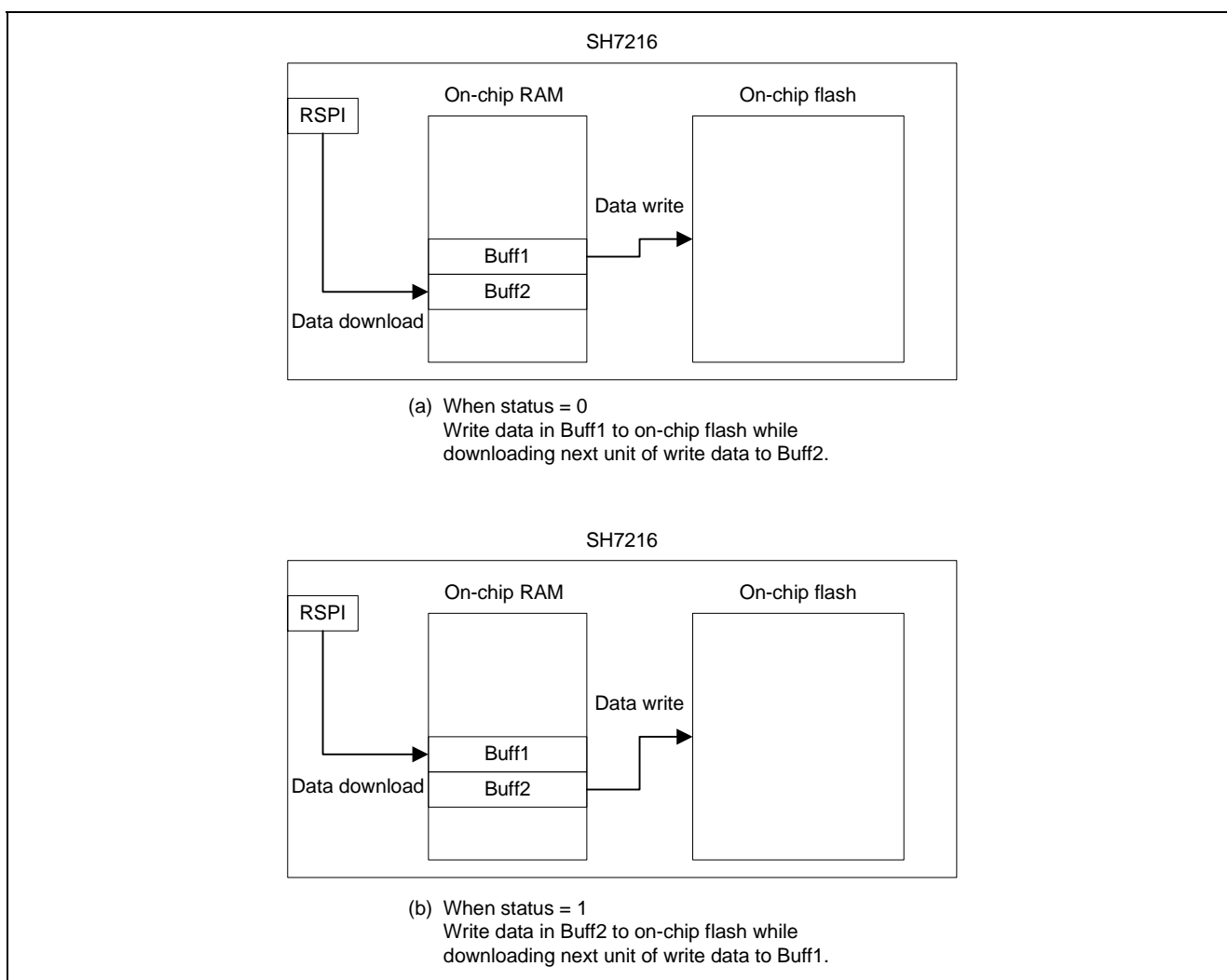
## 2.3 Data Buffer for Reprogramming On-Chip Flash

In the sample application, a buffer area in the SH7216 is used to save the write data to be programmed to the on-chip RAM. The capacity of the buffer area is 256 bytes, which corresponds to the size of one on-chip flash write operation. A double-buffer configuration is used to enable data transfers from the external device and writing to the on-chip flash to take place in parallel.

The operation of the buffers is determined by using status flags.\*<sup>1</sup> When status = 0, the data in buffer 1 (Buff1) is written to the on-chip flash while simultaneously the next unit of write data is downloaded to buffer 2 (Buff2). When status = 1, the operations are reversed.

Figure 5 shows an outline of buffer operation, and table 3 lists the addresses in the data buffer area.\*<sup>2</sup>

- Note:
1. In the sample application these flags are set to user-defined values. For details, see table 3.2, Variables Used by Sample Program.
  2. The data buffer area is managed by dividing it into sections. The addresses assigned to the sections can be changed, allowing user-specified addresses to be set for the buffer area.



**Figure 5 Outline of Buffer Operation**

**Table 3 Data Buffer Area**

| Buffer | Address                    | Size      | Operation Condition                     |
|--------|----------------------------|-----------|---|
| Buff1  | H'FFF8_1000 to H'FFF8_10FF | 256 Bytes | Write to on-chip flash when status = 1. |
| Buff2  | H'FFF8_1100 to H'FFF8_11FF | 256 Bytes | Write to on-chip flash when status = 0. |



3. Operation of Sample Program

Figure 6 shows the overall operation sequence of the SH7216 and the external device.

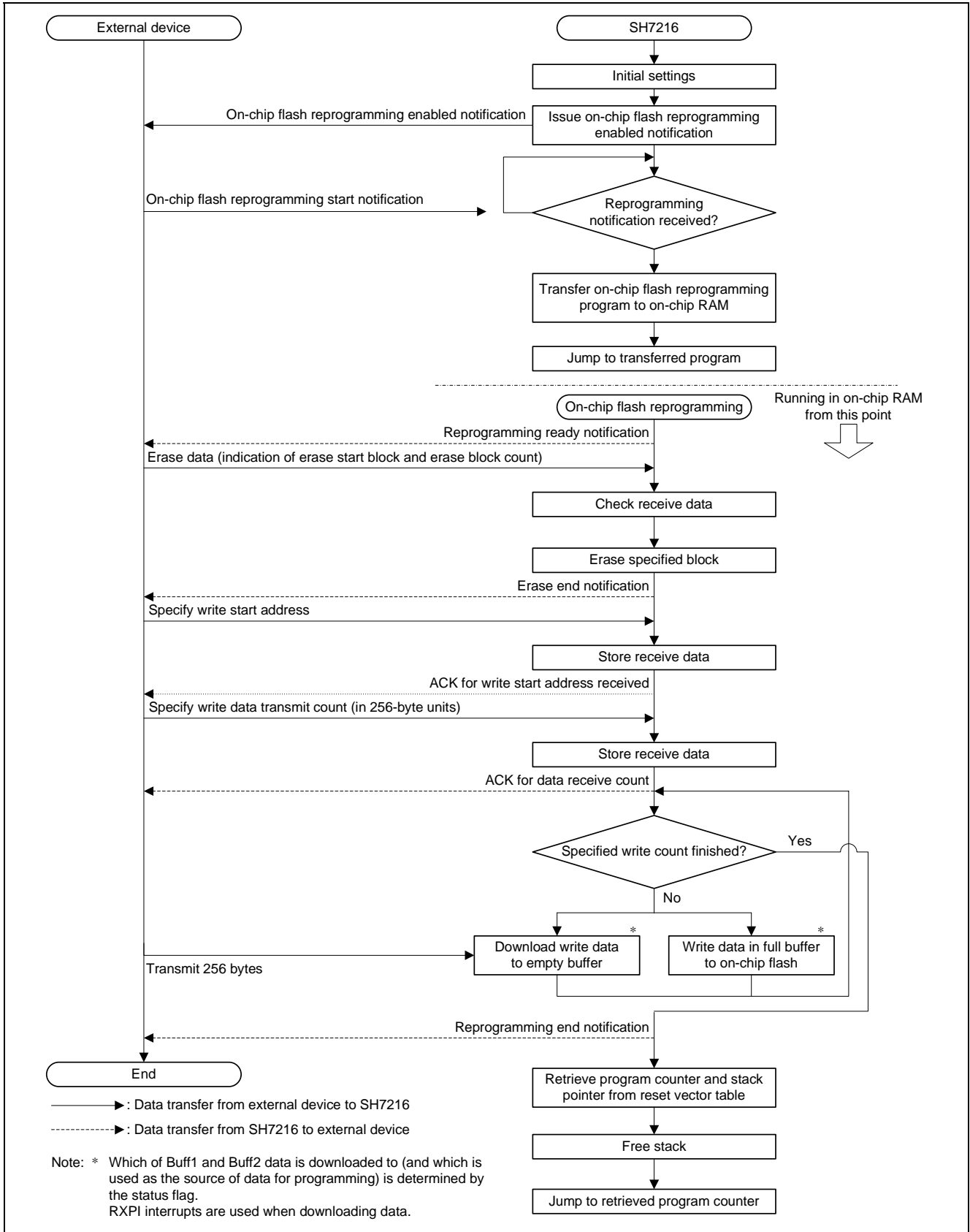


Figure 6 Overall Operation Sequence

## SH7216 Group Using RSPI to Reprogram Flash Memory in User Program Mode

After initial settings complete, the SH7216 issues an on-chip flash reprogramming enabled notification to the external device. After that, it receives a reprogramming start notification from the external device and reprogramming of the on-chip flash starts.

The on-chip flash reprogramming program is executed from the on-chip RAM of the SH7216. Erasing and programming take place according to instructions from the external device. The external device can specify any erasure area and write destination address.

After reprogramming of the on-chip flash finishes, the SH7216 reads the reset vector and frees the stack, after which program execution returns to the on-chip flash.

### 3.1 Basic Specifications of Sample Program

#### 3.1.1 Settings of Sample Program

Table 4 lists the setting used in the sample application.

**Table 4 SH7216 Settings**

| Function | Item                           | Description  |
|----------|--------------------------------|--|
| General  | Frequency<br>(Input: 12.5 MHz) | I $\phi$ = 200 MHz, B $\phi$ = P $\phi$ = 50 MHz,<br>M $\phi$ = 100 MHz, A $\phi$ = 50 MHz     |
|          | Register bank usage            | Enabled for all interrupt levels   |
|          | Interrupt mask level           | 0  |
| RSPI     | Communication mode             | SPI operation (4-line)   |
|          | Pins used                      | PA6 → RSPCK<br>PA7 → MOSI<br>PA8 → MISO<br>PA9 → SSL0  |
|          | Data format                    | MSB first  |
|          | Bit rate                       | 1 Mbps   |
|          | Bit length                     | 32 bits  |
|          | Number of frames               | When transferring write data: 4 frames<br>Communication at other times (command, ACK): 1 frame |
|          | SSL signal polarity            | 1 (H) active   |
|          | Master/slave                   | Master   |
|          | Signal delay setting           | 1 RSPCK  |
|          | Interrupt                      | Receive interrupt (level: H'A)   |

### 3.1.2 Variables Used by Sample Program

Table 5 lists the variables used in the sample application.

**Table 5 Variables Used by Sample Program**

| Variable      | Function   | Type Declaration | Remarks                      |
|---------------|--|------------------|------------------------------|
| Buff1_full    | Shows the state of buffer 1.<br>0: Download in progress or empty<br>1: Download finished                   | unsigned char    |                              |
| Buff2_full    | Shows the state of buffer 2.<br>0: Download in progress or empty<br>1: Download finished                   | unsigned char    |                              |
| Buff_num      | Shows the data position within the buffer (array).   | unsigned char    |                              |
| Status        | Shows the overall state.<br>0: Data in Buff2 is written to flash.<br>1: Data in Buff1 is written to flash. | unsigned char    |                              |
| passfail      | Stores return value from standard API.   | unsigned char    |                              |
| rcv_data      | Stores receive data from RSPI.   | unsigned long    |                              |
| erase_top     | Stores start block of erasure target block.  | unsigned char    | Specified by external device |
| erase_num     | Stores number of blocks to be erased.  | unsigned char    |                              |
| wr_start_addr | Stores write start address.  | unsigned long    |                              |
| wr_num        | Stores write count (256 bytes/write).  | unsigned long    |                              |

### 3.1.3 Details of Handshake Communication

Table 6 lists details of what is communicated between the SH7216 and the external device in the sample program.

**Table 6 List of Communication Details**

| Item                                   | Data        | Function   | Transfer Direction       |
|--|-------------|--|--------------------------|
| Reprogramming enabled notification     | H'8888_8888 |  | SH7216 → External device |
| Reprogramming start notification       | H'0000_1234 |  | External device → SH7216 |
| Reprogramming ready notification       | H'0000_5678 | Sends notification that program execution has transitioned to RAM on the SH7216.           | SH7216 → External device |
| Erase data                             | H'xxxx_yyzz | yy: Erase start block (1 byte)<br>zz: Erase block count (1 byte)                           | External device → SH7216 |
| Erase data received ACK                | H'xxxx_yyzz | Returns the above data.  | SH7216 → External device |
| Erase end notification                 | H'0000_9999 | Sends notification that erasure of the specified area in the SH7216 has finished.          | SH7216 → External device |
| Write start address                    | H'xxxx_xxxx | Specifies the write start address. The data is stored in [wr_start_addr].                  | External device → SH7216 |
| Write start address received ACK       | H'xxxx_xxxx | Returns the above receive data unmodified.   | SH7216 → External device |
| Write data transmit count              | H'xxxx_xxxx | Specifies the write count (256 bytes per write operation). The data is stored in [wr_num]. | External device → SH7216 |
| Write data transmit count received ACK | H'xxxx_xxxx | Returns the above data.  | SH7216 → External device |
| Write data transmit request            | H'1111_1111 |  | SH7216 → External device |
| Write end notification                 | H'A5A5_5A5A |  | SH7216 → External device |

## 3.2 Operation Procedures of Sample Program

This section describes the SH7216 operation procedures. Operate the external device in to match the procedures described below.

### 3.2.1 Procedure [1] Initial Settings

After initial settings of the frequency, RSPI, etc., the SH7216 transmits a [reprogramming enabled notification] to the external device.

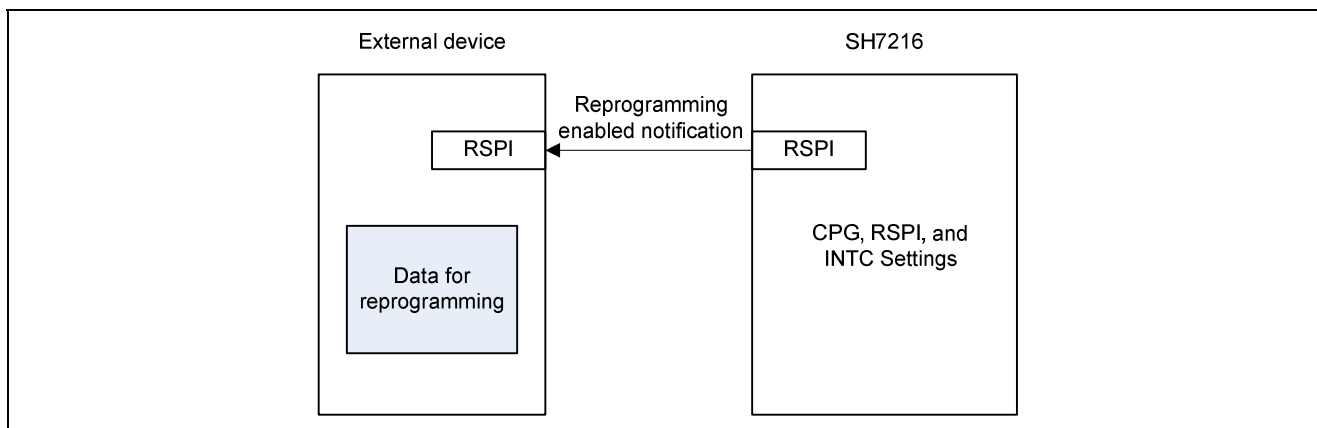


Figure 7 Initial Settings

### 3.2.2 Procedure [2] Preparation for On-Chip Flash Reprogramming

When the SH7216 receives a [reprogramming start notification] from the external device, it prepares to reprogram the on-chip flash.

Preparation for reprogramming consists of transferring the on-chip flash reprogramming program to the on-chip RAM and transitioning the program's execution area from the on-chip flash to the on-chip RAM. In addition, the vector base register (VBR) value is changed because the sample program uses the RSPI data receive interrupt when receiving reprogramming data from the external device.

After preparation for reprogramming is completed, a [reprogramming ready notification] is transmitted to the external device.

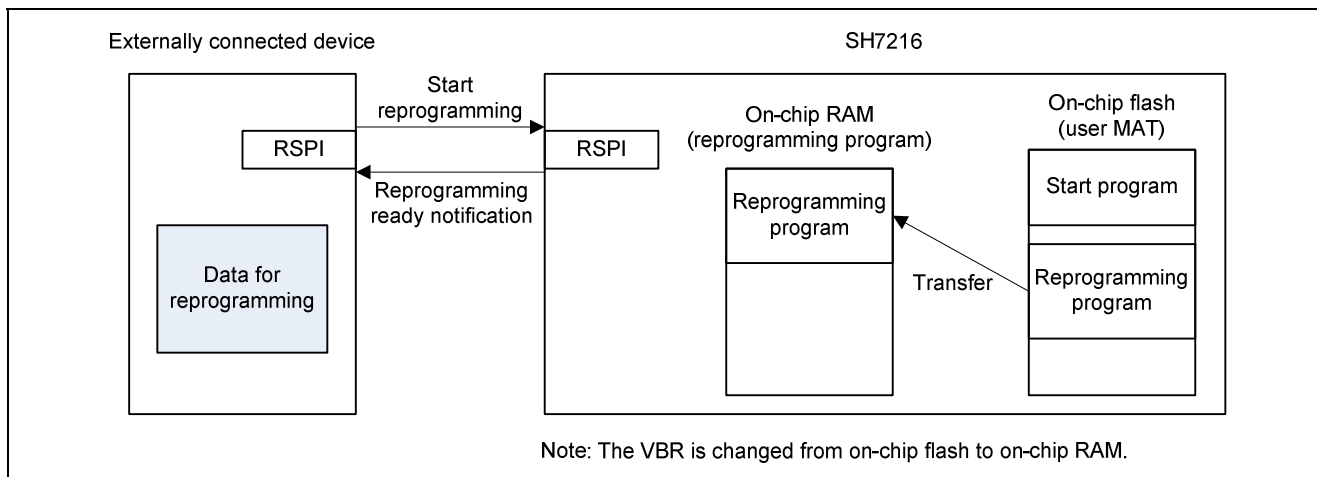
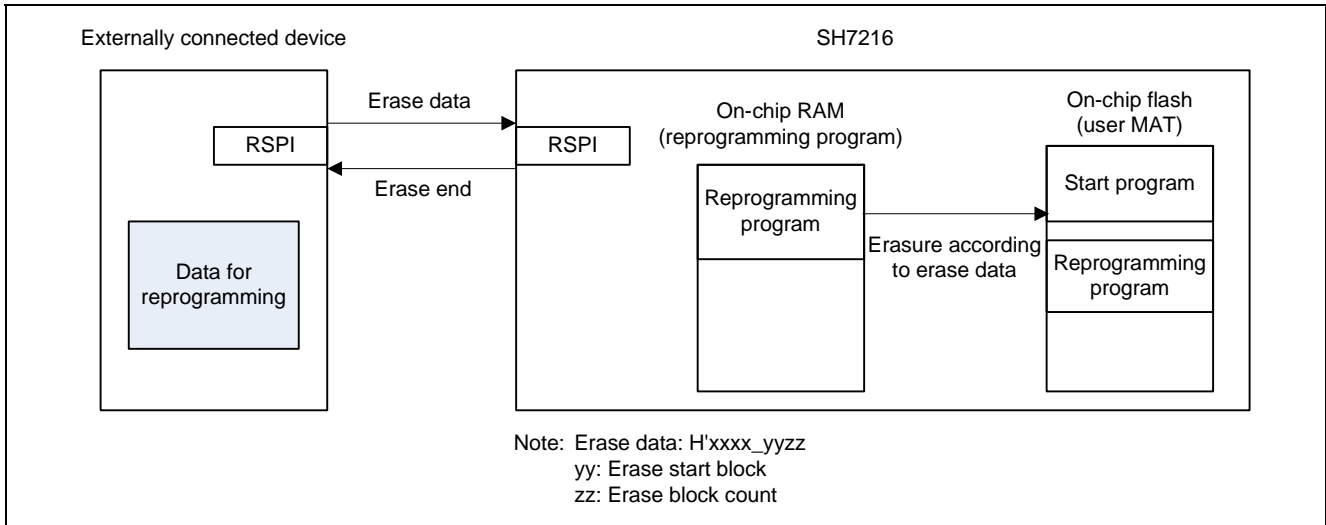


Figure 8 Preparation for Reprogramming

### 3.2.3 Procedure [3] Erasing On-Chip Flash

The SH7216 erases an area in the on-chip flash according to the [erase data] transmitted to it by the external device. After erasure of the specified area is completed, an [erase end notification] is transmitted to the external device.



**Figure 9 Erase Operation**

3.2.4 Procedure [4] Programming On-Chip Flash

The SH7216 programs the on-chip flash according to the [write start address] and [write data transmit count (256 bytes/write)].

The reprogramming data sent from the external device is stored in data buffers in the on-chip RAM. There are two data buffers, and writing of data to the on-chip flash proceeds according to the state of the data downloads from the external device.

After programming of the on-chip flash is completed, a [write end notification] is transmitted to the external device.

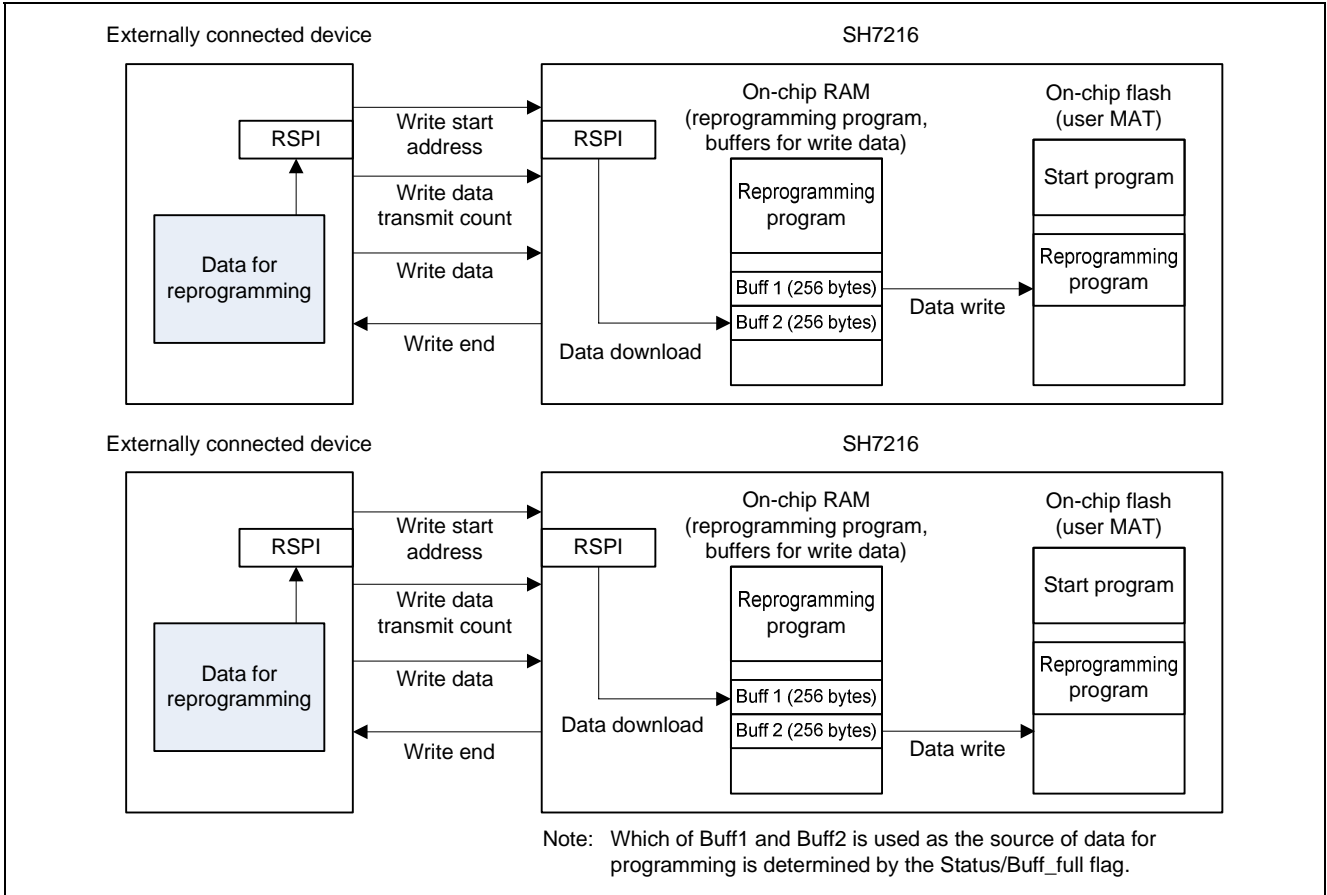


Figure 10 Programming Operation

3.2.5 Procedure [5] Program Reset

After reprogramming of the on-chip flash completes, the SH7216 reads the reset vector in the on-chip flash and returns program operation to the on-chip flash.

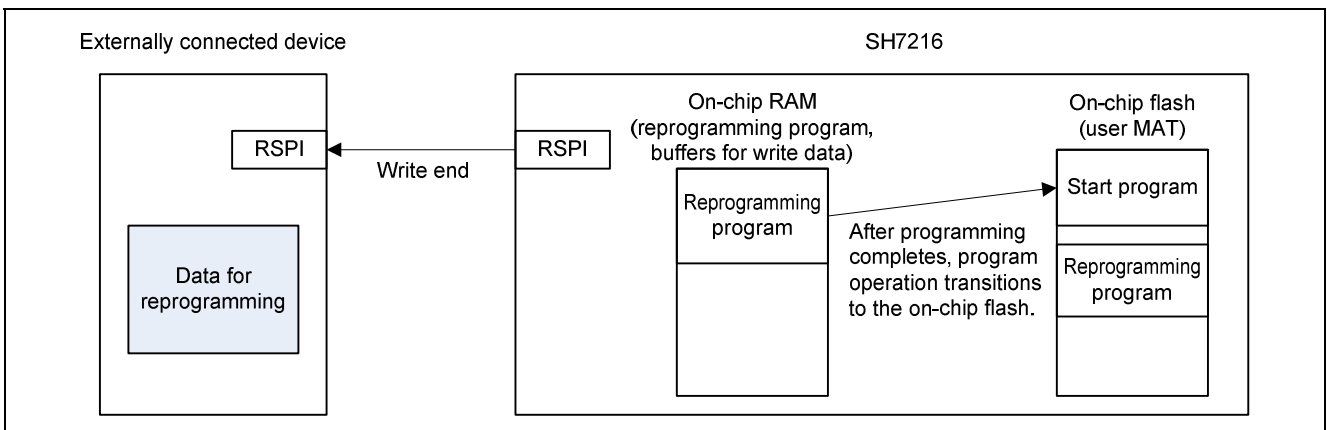


Figure 11 Programming Operation

### 3.3 Register Settings of Sample Program

Table 7 lists the register settings used in the sample application.

**Table 7 Register Settings**

| Module                                     | Register Name                                   | Address    | Setting Value | Description   |
|--|---|------------|---------------|---|
| Clock pulse generator (CPG)                | Frequency control register (FRQCR)              | H'FFFE0010 | H'0303        | STC[2:0] = B'011: ×1/8<br>IFC[2:0] = B'000: ×1/4<br>PFC[2:0] = B'011: ×1/8  |
|  | MTU2S clock frequency control register (MCLKCR) | H'FFFE0410 | H'41          | MSDIVS[1:0] = B'01: ×1/2  |
|  | AD clock frequency control register (ACLKCR)    | H'FFFE0414 | H'43          | ASDIVS[1:0] = B'11: ×1/4  |
| Interrupt controller (INTC)                | Interrupt priority register 17 (IPR17)          | H'FFFE0C12 | H'F000        | The interrupt priority level is set to 15.  |
|  | Bank number register (IBNR)                     | H'FFFE080E | H'C000        | BE[1:0] = B'11: Usage of register banks is according to setting of IBCR.  |
|  | Bank control register (IBCR)                    | H'FFFE080C | H'FFFE        | Enable register bank usage for all interrupt levels.  |
| Standby control                            | Standby control register 5 (STBCR5)             | H'FFFE0418 | H'FE          | MSTP50 = 0: RSPI operates   |
| Pin function controller (PFC)              | Port A control register L3 (PACRL3)             | H'FFFE3812 | H'0055        | PA9MD[2:0] = B'101: SSL0 I/O<br>PA8MD[2:0] = B'101: MISO I/O  |
|  | Port A control register L2 (PACRL2)             | H'FFFE3814 | H'5500        | PA7MD[2:0] = B'101: MOSI I/O<br>PA6MD[2:0] = B'101: RSPCK I/O   |
| Renesas serial peripheral interface (RSPI) | RSPI control register (SPCR)                    | H'FFFFB000 | H'C8          | SPRIE = B'1: Generation of RSPI receive interrupt requests enabled<br>SPE = B'1: RSPI function enabled<br>MSTR = B'1: Master mode<br>SPMS = B'0: SPI operation (4-wire) |
|  | RSPI slave select polarity register (SSLP)      | H'FFFFB001 | H'00          | SSL[3:0]P = B'0000: SSL0 signal set to active-0   |
|  | RSPI pin control register (SPPCR)               | H'FFFFB002 | H'30          | MOIFE = B'1: MOSI output value equals value set in MOIFV bit.<br>MOIFV = B'1: MOSI idle fixed value equals 1.<br>SPOM = B'0: RSPI output pin is CMOS output.            |
|  | RSPI status register (SPSR)                     | H'FFFFB003 | H'22          | When making settings:<br>Clear SPRF.<br>Set SPTEF.<br>Clear OVRF.   |
|  | RSPI data register (SPDR)                       | H'FFFFB004 |               | Transmit and receive data controlled by RSPI commands are written to and read from this register.   |
|  | RSPI sequence control register (SPSCR)          | H'FFFFB008 | H'00          | SPLN[2:0] = B'000: Sequence length of 1   |
|  | RSPI bit rate register (SPBR)                   | H'FFFFB00A | H'24          | RSPI 4-wire master mode bit rate: 1 Mbps  |



| Module                                     | Register Name                      | Address    | Setting Value          | Description   |
|--|------------------------------------|------------|------------------------|---|
| Renesas serial peripheral interface (RSPI) | RSPI data control register (SPDCR) | H'FFFFB00B | H'20                   | SPLW = B'1: Longword access to SPDR register  |
|  |                                    |            | H'23                   | SPFC[1:0] = B'00: 1 frame can be stored in SPDR register.<br>SPFC[1:0] = B'11: 4 frame can be stored in SPDR register.  |
|  | RSPI command register 0 (SPCMD0)   | H'FFFFB010 | H'0703<br>or<br>H'0203 | SCKDEN = B'0: RSPCK delay of 1 RSPCK<br>SLNDEN = B'0: SSL negation delay of 1 RSPCK<br>SPNDEN = B'0: Next-access delay of 1 RSPCK<br>LSBF = B'0: MSB first<br>SPB[3:0]: Transfer data length setting<br>SSLKP = B'0: All SSL signals negated upon completion of transfer<br>SSLA[2:0] = B'000: Asserted at SSL0<br>BRDV[1:0] = B'00: Base bit rate selected<br>CPOL = B'1: RSPCK = 1 when idle<br>CPHA = B'1: Data change at odd edge, data sampling at even edge |

3.4 Flowchart of Sample Program

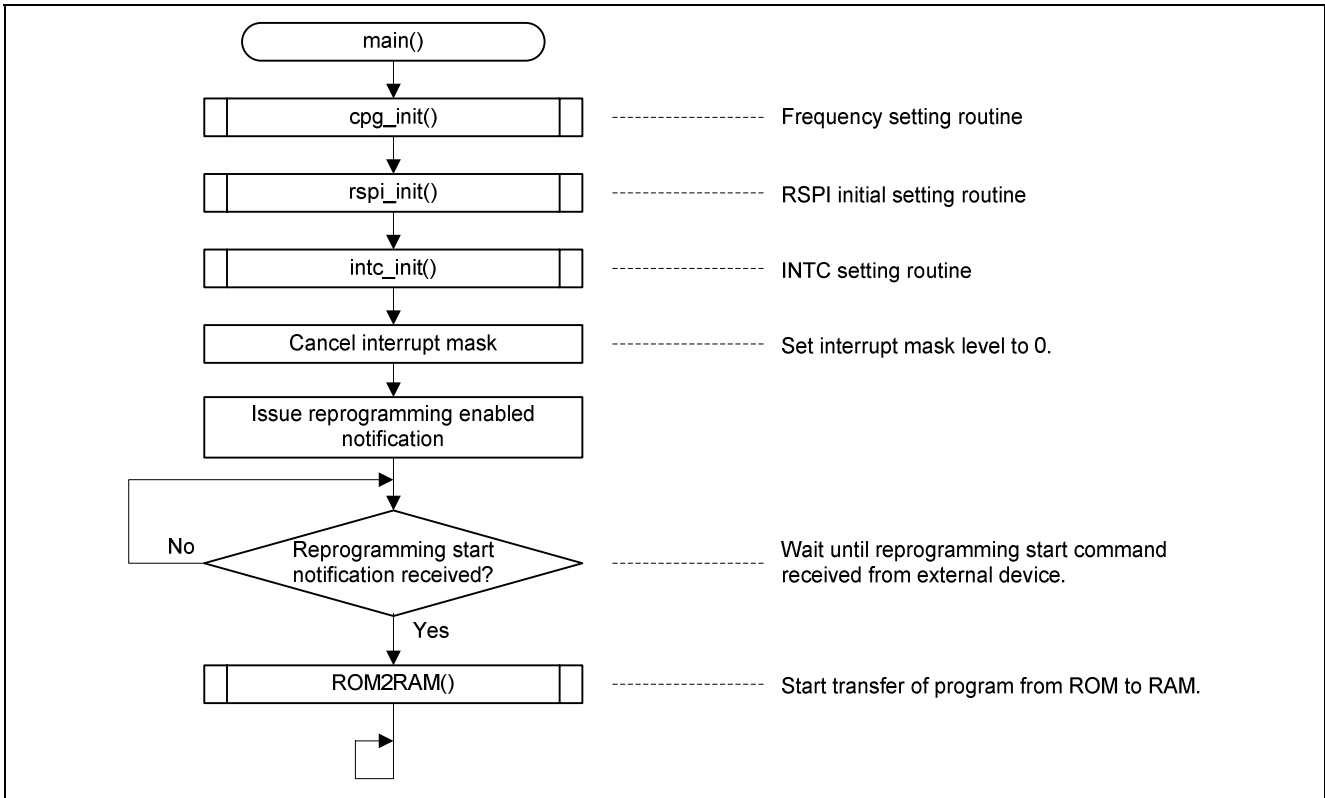


Figure 12 Main Routine

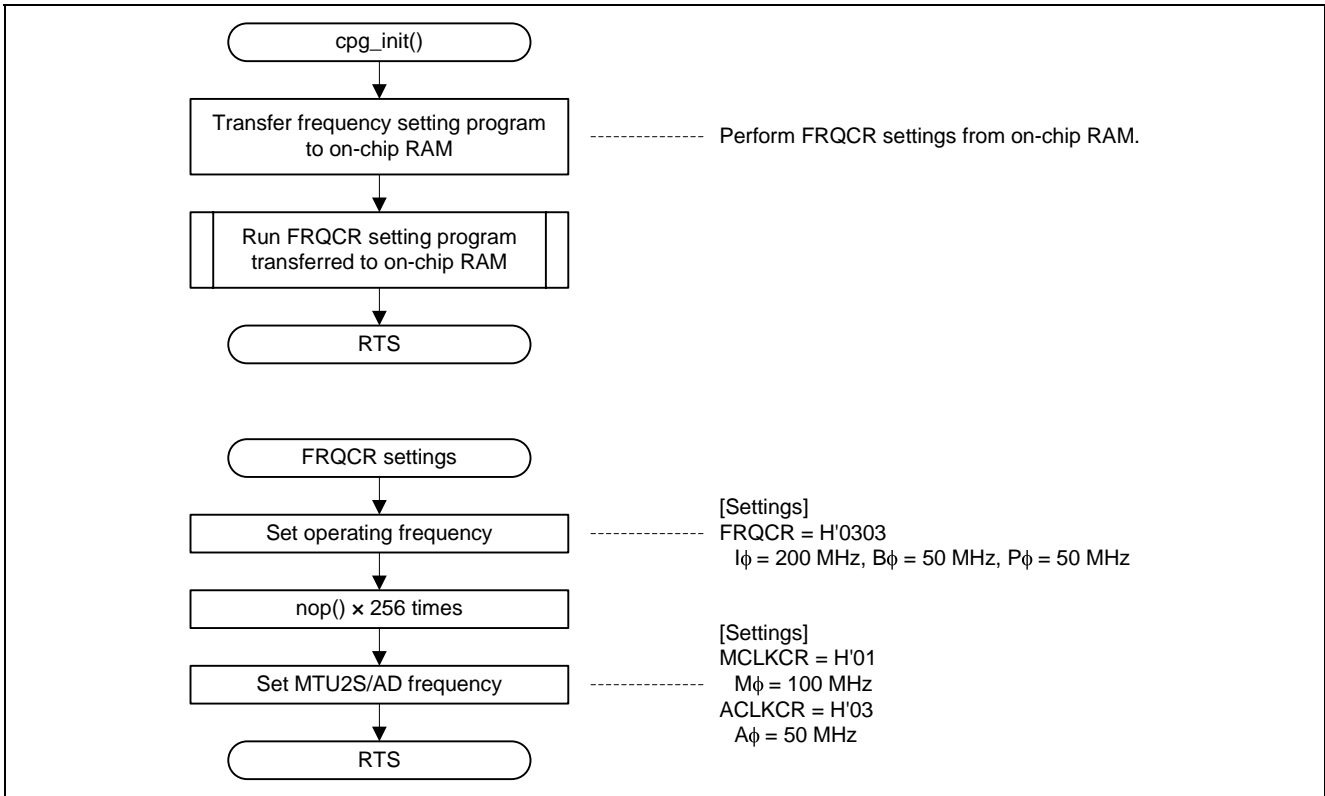


Figure 13 Frequency Setting Routine

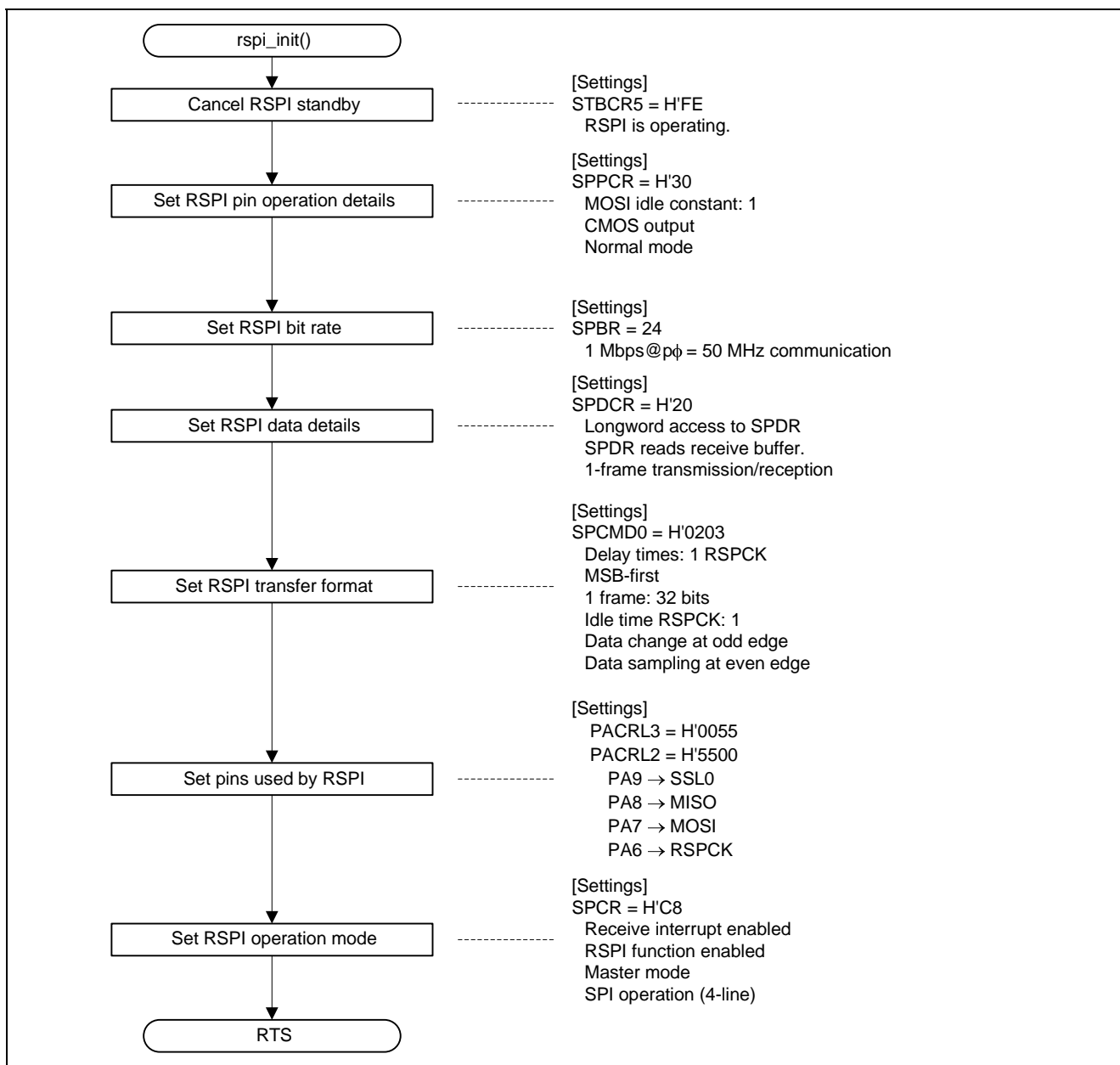


Figure 14 RSPI Initial Setting Routine

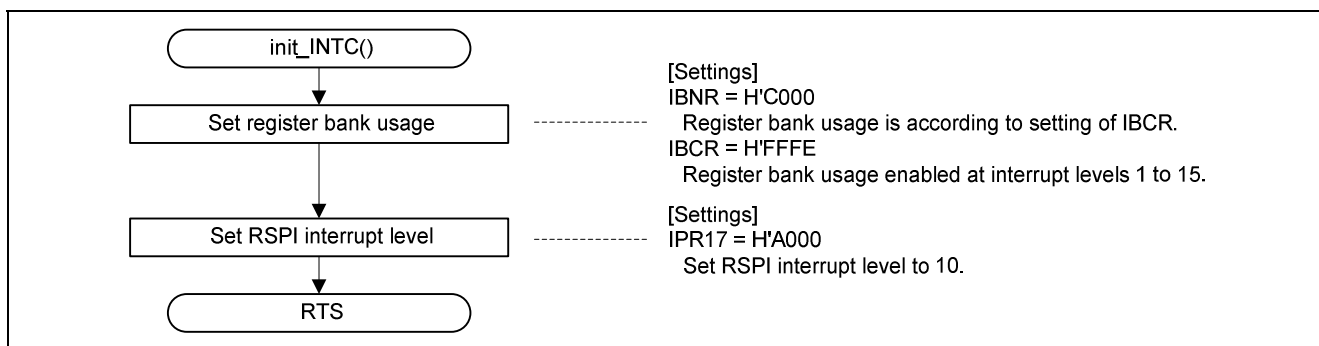
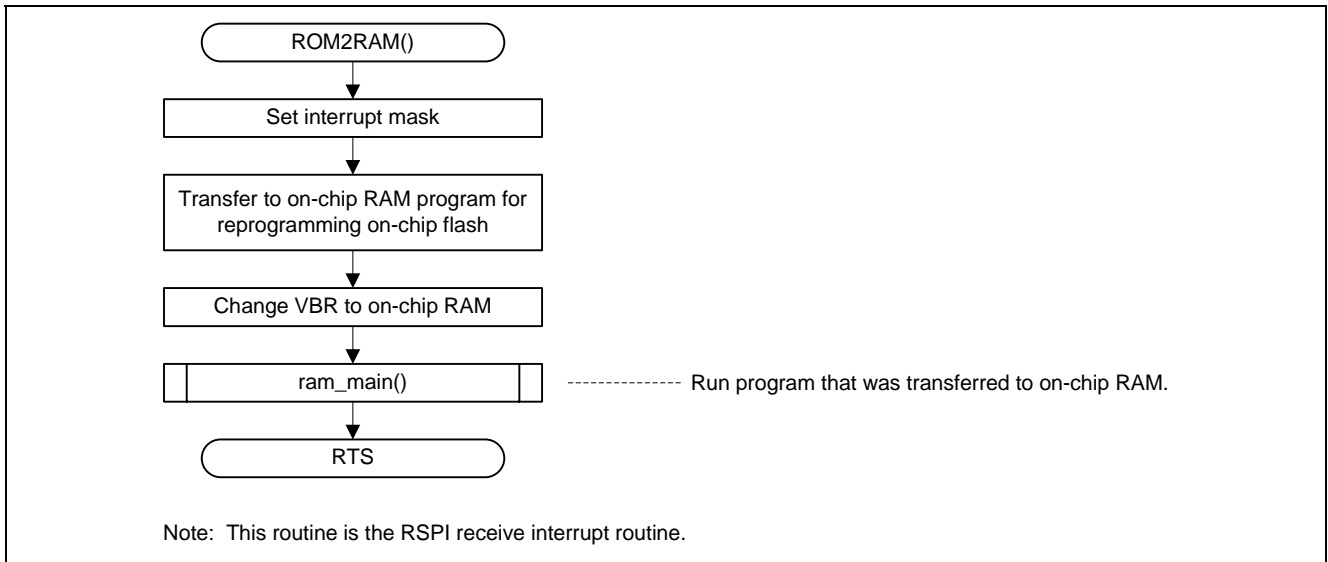


Figure 15 INTC Initial Setting Routine

**Figure 16 Reprogramming Preparation (Program Transfer) Routine**

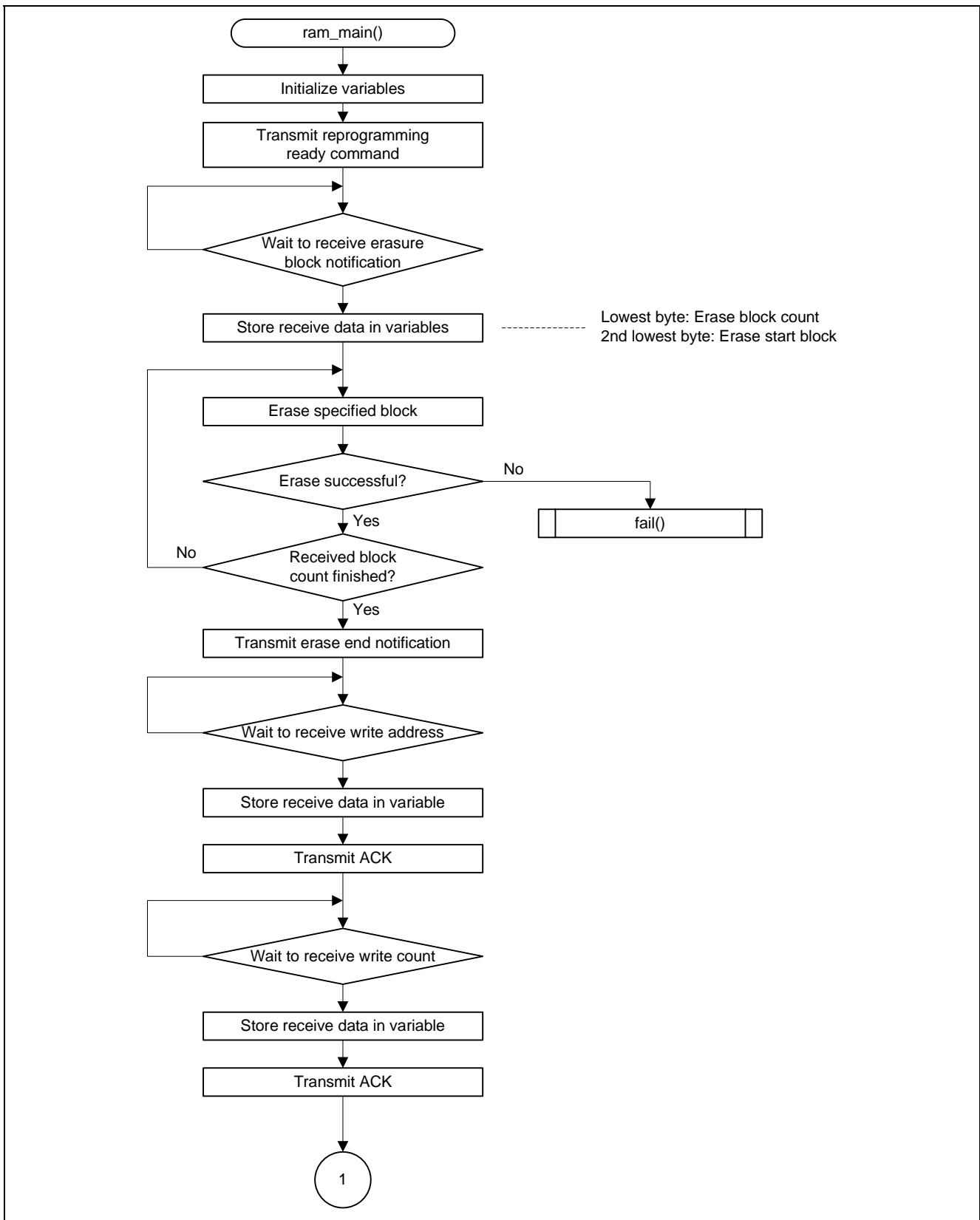


Figure 17 Reprogramming Control Routine (1)

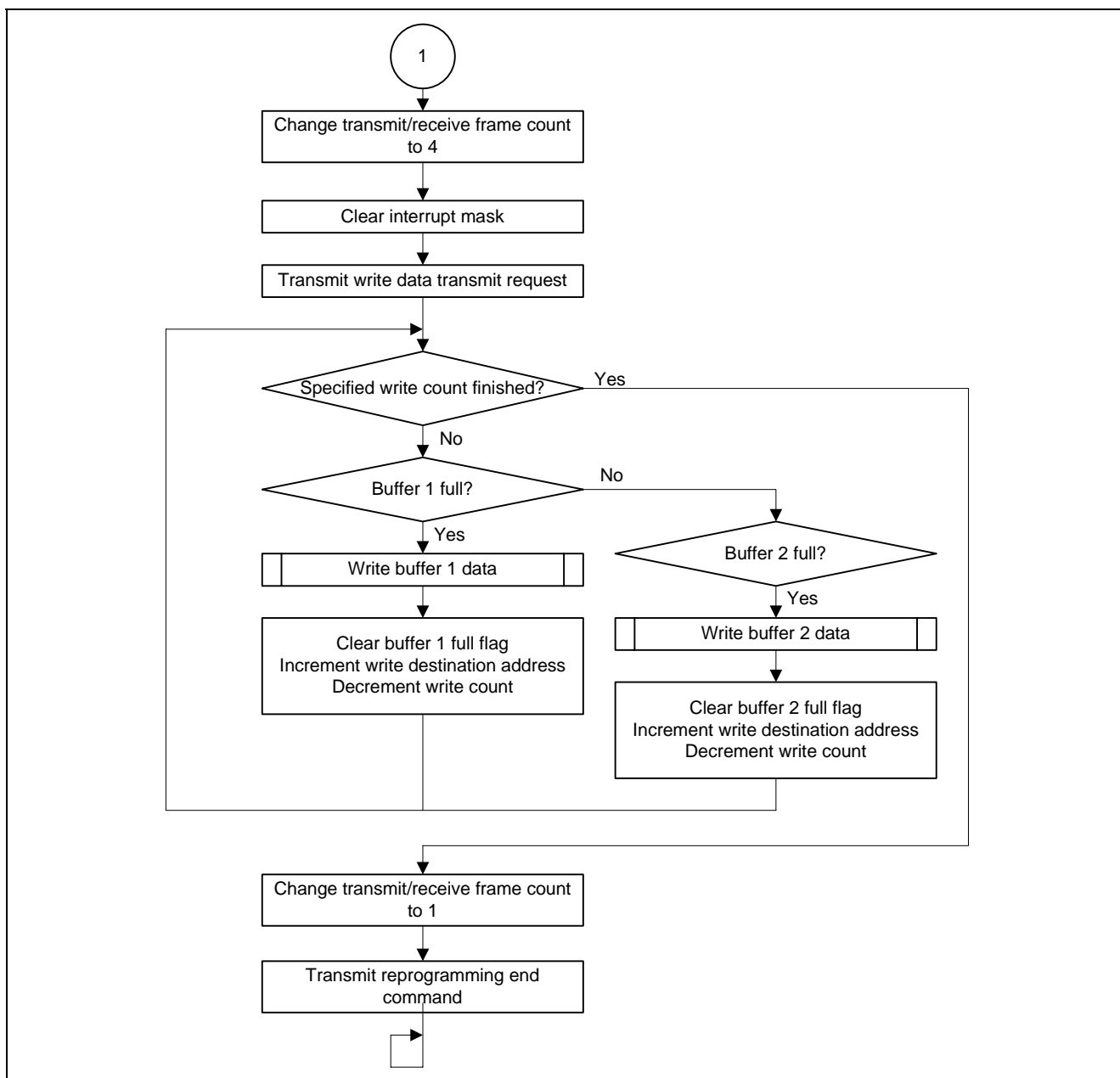


Figure 18 Reprogramming Control Routine (2)

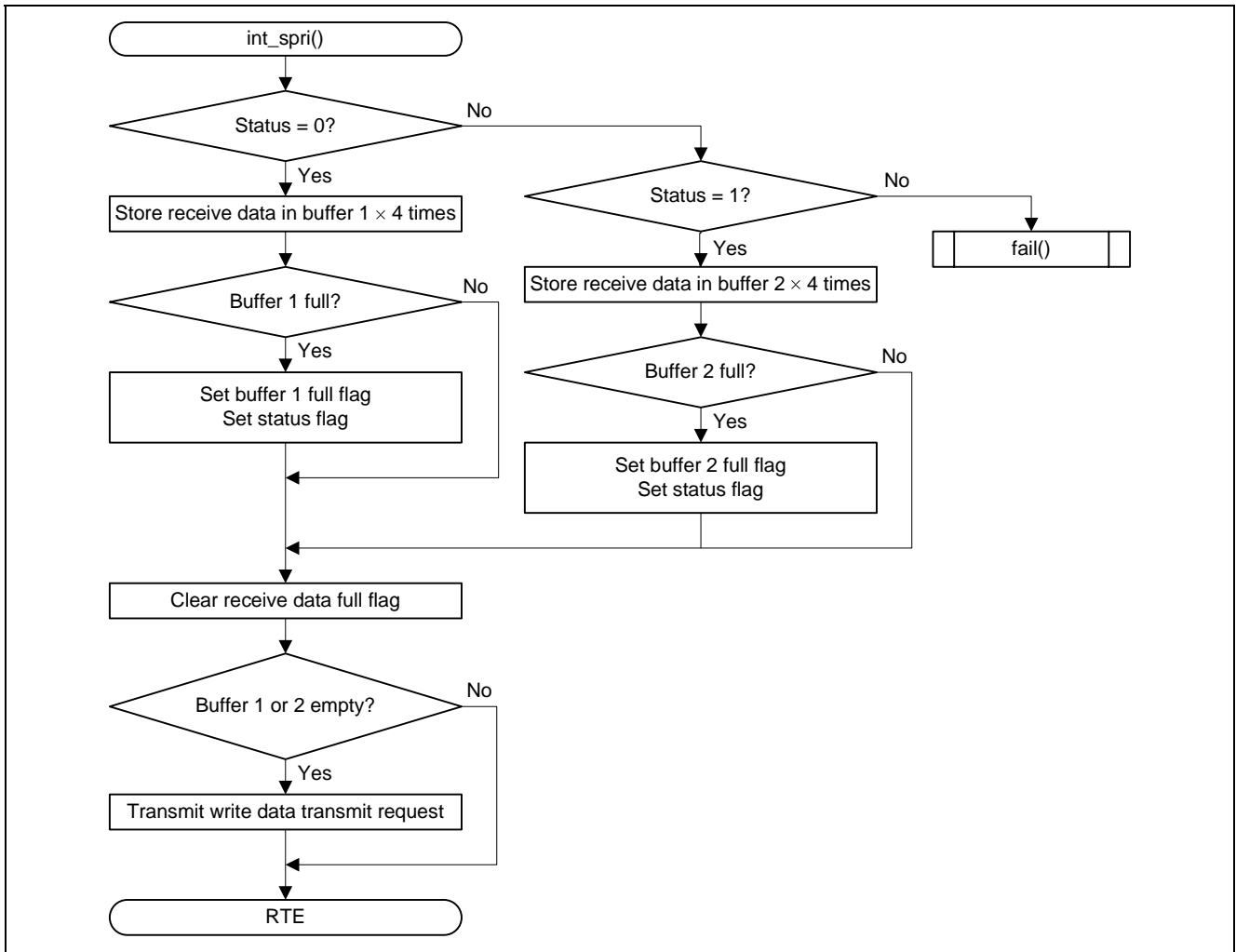


Figure 19 Write Data Download Routine (Receive Interrupt)

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## Revision Record

| Rev. | Date      | Description |   |
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|      |           | Page        | Summary   |
| 1.00 | Jun.20.10 | —           | First edition issued  |
| 2.00 | Dec.14.10 | —           | Amended to use simple flash API for SH-2 and SH-2A<br>Revised overall |
| 2.10 | Feb.28.11 | —           | Added read after FRQCR settings                                       |
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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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**Renesas Electronics America Inc.**  
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**  
7F, No. 363 Fu Shing North Road Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: +65-6213-0200, Fax: +65-6278-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141