
SH7216 Group

Using RCAN-ET to Reprogram Flash Memory in User Program Mode

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Introduction

In the sample application, the user program mode of the SH7216 is used to reprogram the on-chip flash memory. The data used to program the on-chip flash is stored in an external device connected to the SH7216, and the Renesas controller area network (RCAN-ET) is used for data transfer.

The program used to reprogram the on-chip flash in the sample application is located in the user MAT of the SH7216. The simple flash API (standard API) for the SH-2 and SH-2A, supplied by Renesas Electronics, is used to reprogram the on-chip flash.

Target Device

SH7216

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1. Introduction

In the sample application, the SH7216 receives data from a connected external device and reprograms the on-chip flash in user program mode.

1.1 Specifications

Figure 1 shows a system overview of the sample application.

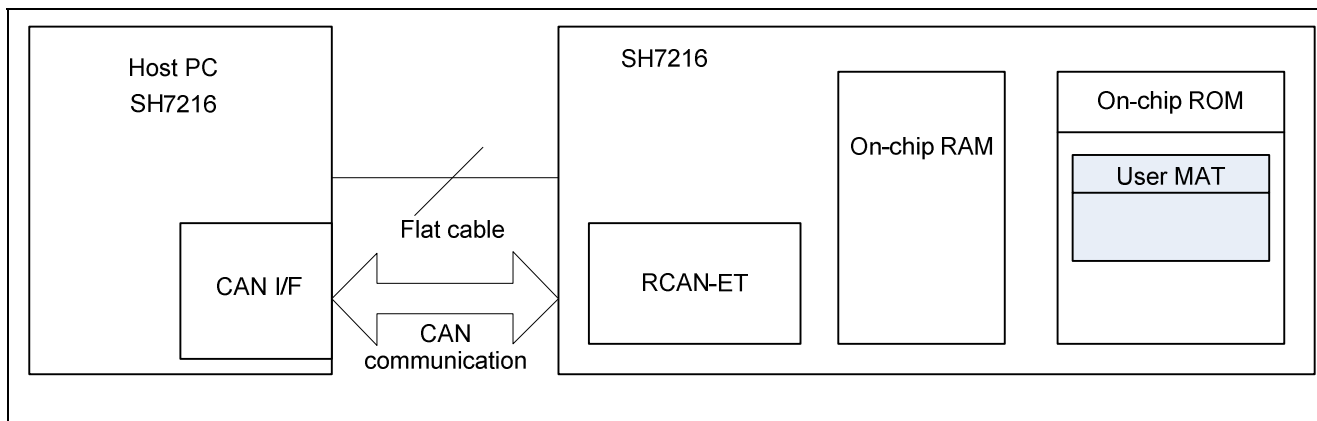


Figure 1 System Configuration

- The SH7216 operating mode is user program mode.
- The data to be written to the SH7216 is stored in the external device.
- The SH7216 and external device are connected by the RCAN-ET, via which the write data is transferred.
- The SH7216 executes a program in on-chip RAM during reprogramming of the on-chip flash.
- The SH7216 has two data buffer areas (256 bytes each), which are used in parallel for writing to the on-chip flash and for downloading data.
- The standard API is used to program and erase the on-chip flash.

Table 1 SH7216 Mode Pin Settings

Mode	Pin Settings		
	FWE	MD1	MD0
User program mode	1	1	0

1.2 Functions Used

- Renesas controller area network (RCAN-ET)
- Dedicated sequencer for on-chip flash (FCU)

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz
	Bus clock: 50 MHz
	Peripheral clock: 50 MHz
	MTU2S clock: 100 MHz
	AD clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package, Ver. 9.03.00, Release 02
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu -pic=1 -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Notes

The following application note is related to this application note. Refer to it as necessary in conjunction with this application note.

SH Family: Simple Flash API for SH-2 and SH-2A

2. Overview and Functions

In the sample application, the SH7216 and external device are connected by the RCAN-ET. In addition, a dedicated sequencer (FCU) is used on the SH7216 to program and erase the on-chip flash.

2.1 Description of Functions Used

2.1.1 Controller Area Network (RCAN-ET) Functions

The RCAN-ET is a module for controlling a controller area network (CAN) designed to provide real-time communication for applications such as automotive or industrial machinery systems. In the sample application, the RCAN-ET is used to transfer between the SH7216 and an external device data for reprogramming the on-chip flash memory.

Figure 2 is a block diagram of the RCAN-ET.

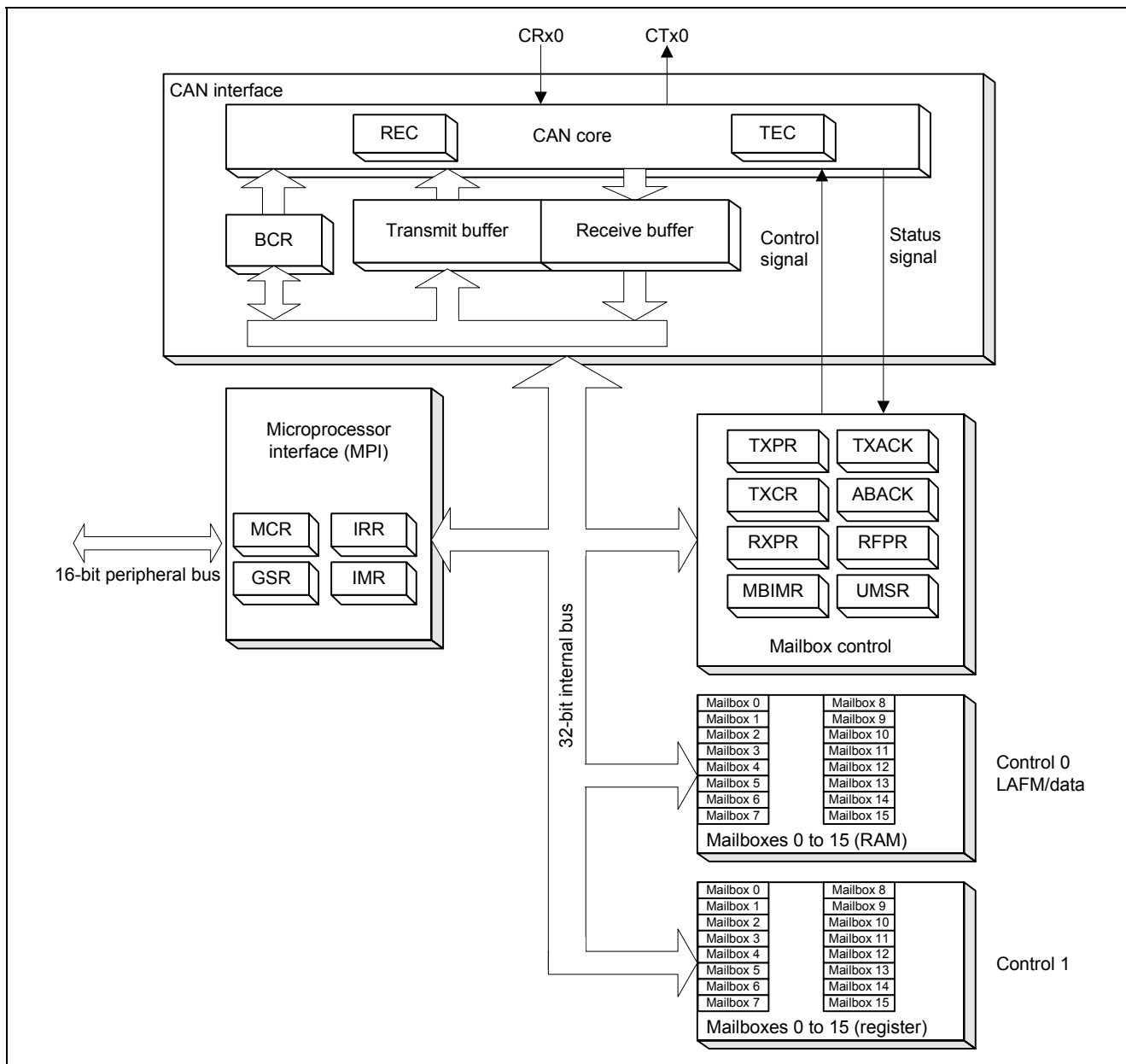


Figure 2 Block Diagram of RCAN-ET

2.1.2 On-Chip Flash Dedicated Sequencer (FCU) Functions

The SH7216 uses the FCU to reprogram the on-chip flash.

Figure 3 is a block diagram of the on-chip flash.

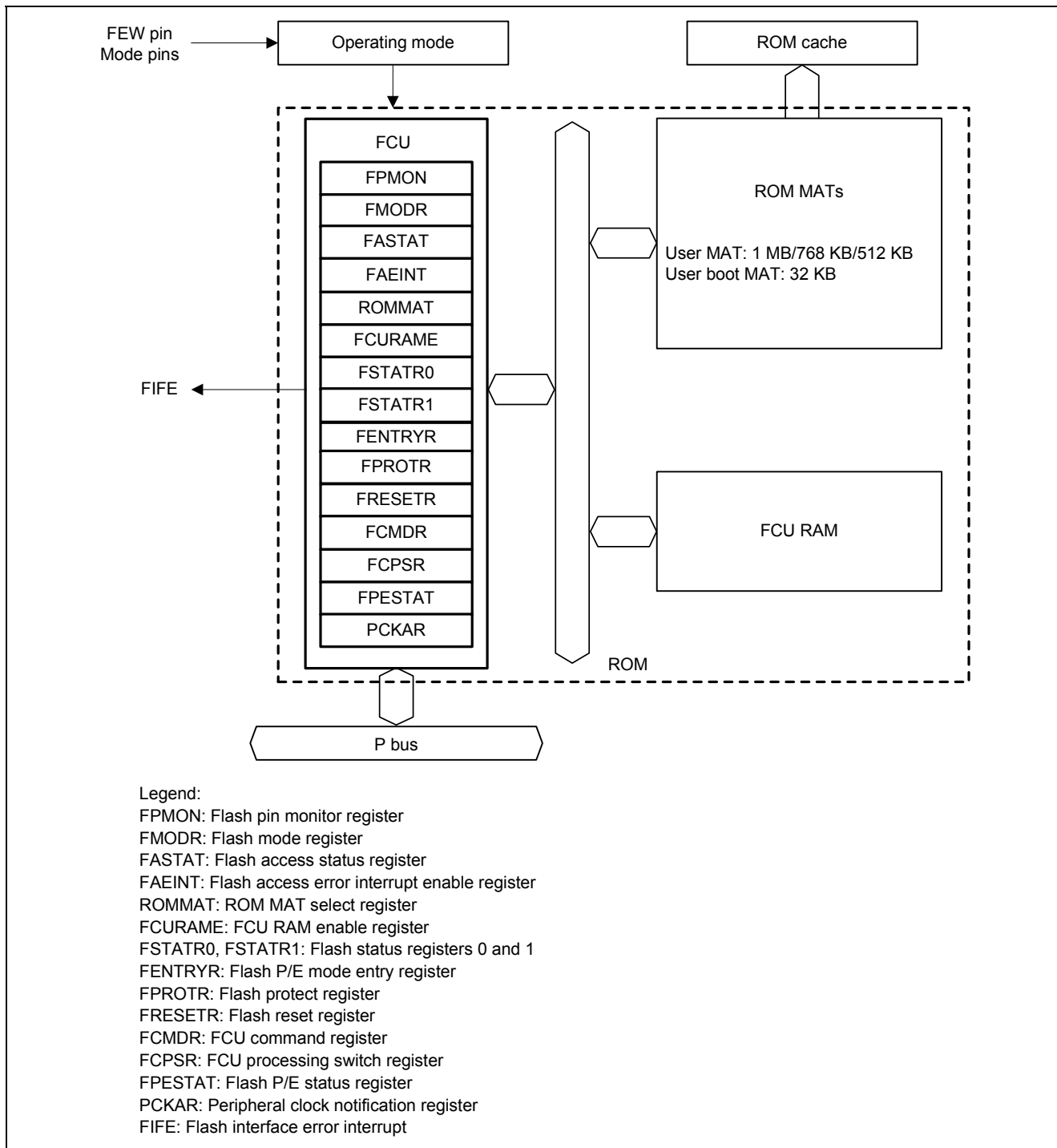


Figure 3 Block Diagram of On-Chip Flash

2.2 On-Chip Flash Programming/Erasing Operation

The SH7216 uses the FCU to program and erase the on-chip flash. In the sample application, a standard API is used to program and erase the on-chip flash. The operations described below are carried out within the standard API. For details of the standard API, see the related application note.

2.2.1 Preparation for On-Chip Flash Programming/Erasing

In order to use the FCU, the FCU firmware must be stored in the FCU RAM. After the FCU firmware has been transferred, the FCU can be used to program or erase the on-chip flash by issuing FCU commands to it.

The FCU firmware is stored in the FCU firmware area of the device, and it must be transferred to the FCU RAM at startup. In addition, FCU RAM access is disabled at device startup, so access must be enabled by making the appropriate register setting.

2.2.2 On-Chip Flash Erasing

On the SH7216, the on-chip flash is divided into multiple blocks, and erasing is performed in block units. After the FCU firmware has been transferred, the FCU performs a block erase when an erase command*¹ and an execute command are written to the address of the erasure target block.

Figure 4 shows the division of the SH7216 erasure blocks, and table 2 lists the addresses of the individual blocks.

Note: 1. The erase command may be written to any valid program/erase address in the on-chip flash.

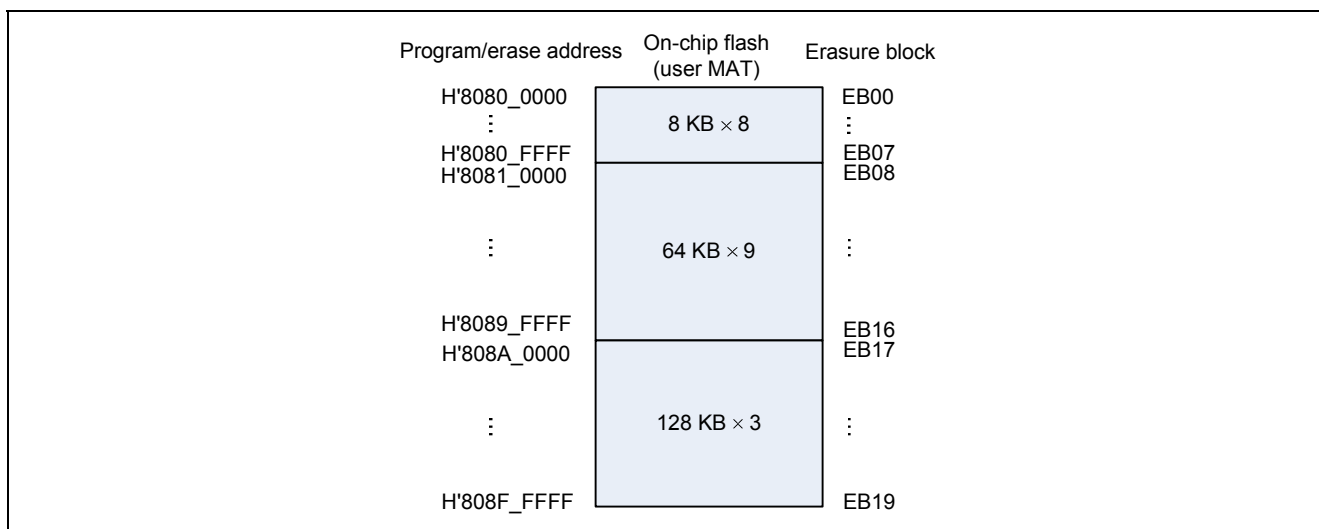


Figure 4 Division of On-Chip Flash Erasure Blocks

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Table 2 Erasure Blocks and Addresses

Erasure Block	Actual Address	Program/Erase Address	Unit Capacity
EB00	H'0000_0000 to H'0000_1FFF	H'8080_0000 to H'8080_1FFF	8 KB
EB01	H'0000_2000 to H'0000_3FFF	H'8080_2000 to H'8080_3FFF	
EB02	H'0000_4000 to H'0000_5FFF	H'8080_4000 to H'8080_5FFF	
EB03	H'0000_6000 to H'0000_7FFF	H'8080_6000 to H'8080_7FFF	
EB04	H'0000_8000 to H'0000_9FFF	H'8080_8000 to H'8080_9FFF	
EB05	H'0000_A000 to H'0000_BFFF	H'8080_A000 to H'8080_BFFF	
EB06	H'0000_C000 to H'0000_DFFF	H'8080_C000 to H'8080_DFFF	
EB07	H'0000_E000 to H'0000_FFFF	H'8080_E000 to H'8080_FFFF	
EB08	H'0001_0000 to H'0001_FFFF	H'8081_0000 to H'8081_FFFF	64 KB
EB09	H'0002_0000 to H'0002_FFFF	H'8082_0000 to H'8082_FFFF	
EB10	H'0003_0000 to H'0003_FFFF	H'8083_0000 to H'8083_FFFF	
EB11	H'0004_0000 to H'0004_FFFF	H'8084_0000 to H'8084_FFFF	
EB12	H'0005_0000 to H'0005_FFFF	H'8085_0000 to H'8085_FFFF	
EB13	H'0006_0000 to H'0006_FFFF	H'8086_0000 to H'8086_FFFF	
EB14	H'0007_0000 to H'0007_FFFF	H'8087_0000 to H'8087_FFFF	
EB15	H'0008_0000 to H'0008_FFFF	H'8088_0000 to H'8088_FFFF	
EB16	H'0009_0000 to H'0009_FFFF	H'8089_0000 to H'8089_FFFF	
EB17	H'000A_0000 to H'000B_FFFF	H'808A_0000 to H'808B_FFFF	128 KB
EB18	H'000C_0000 to H'000D_FFFF	H'808C_0000 to H'808D_FFFF	
EB19	H'000E_0000 to H'000F_FFFF	H'808E_0000 to H'808F_FFFF	

2.2.3 On-Chip Flash Programming

Programming of the on-chip flash can only take place when the target area is in the erased state. A single write to the user MAT comprises a 256-byte unit of data. As with erasing, the programming procedure consists of issuing a command to the FCU, after which the FCU performs the operation. A write command and the write size*¹ are issued to the program/erase address, followed by writing*² the write data (256 bytes) to the write destination address.*³

- Notes:
1. The write size is fixed at 256 bytes when writing to the user MAT and user boot MAT (issue H'80 as the size).
 2. The write data is written to the program/erase address in word size.
 3. This address (the program/erase address) is the write address plus H'8080_0000.

2.3 Data Buffer for Reprogramming On-Chip Flash

In the sample application, a buffer area in the SH7216 is used to save the write data to be programmed to the on-chip RAM. The capacity of the buffer area is 256 bytes, which corresponds to the size of one on-chip flash write operation. A double-buffer configuration is used to enable data transfers from the external device and writing to the on-chip flash to take place in parallel.

The operation of the buffers is determined by using the buff0_full and buff1_full flags. When the value of buff0_full is BUF_ON, the data in buffer 0 (Buff0) is written to the on-chip flash while simultaneously the next unit of write data is downloaded to buffer 1 (Buff1). When the value of buff1_full is BUF_ON, the operations are reversed.

Figure 5 shows an outline of buffer operation.

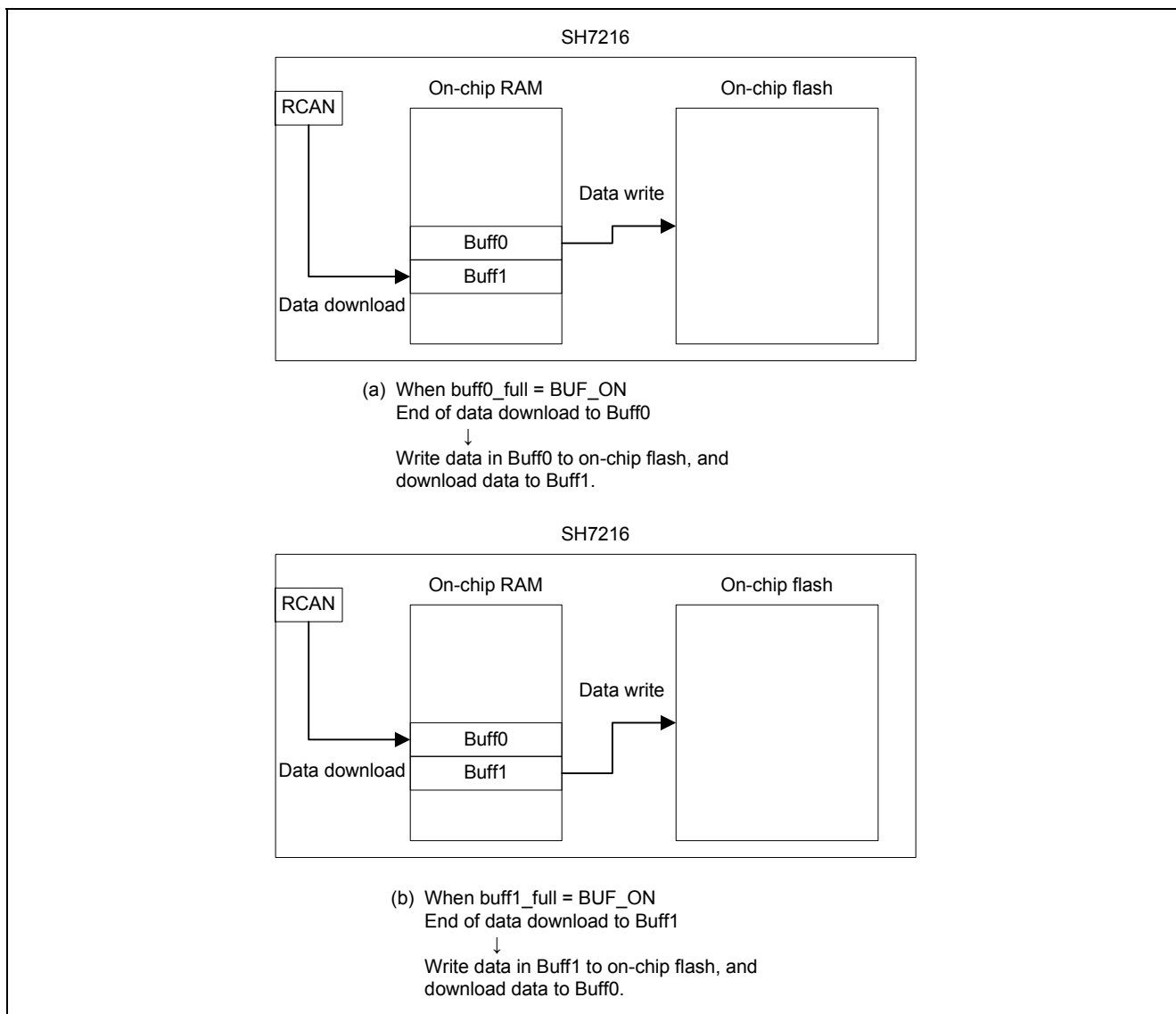


Figure 5 Outline of Buffer Operation

3. Operation of Sample Program

3.1 Outline of Operation Overall

The sample application erases and programs the user MAT area except for block EB00 (EB01 to EB19).

Figure 6 shows the overall operation sequence.

The above-mentioned area in the on-chip flash programming target device (SH7216) is erased, and, after RCAN initialization, the SH7216 waits to receive a start command. After a start command is received from the external device, the SH7216 continues to receive data from the external device until a write end command is received.

After all the data has been written, the SH7216 ends processing.

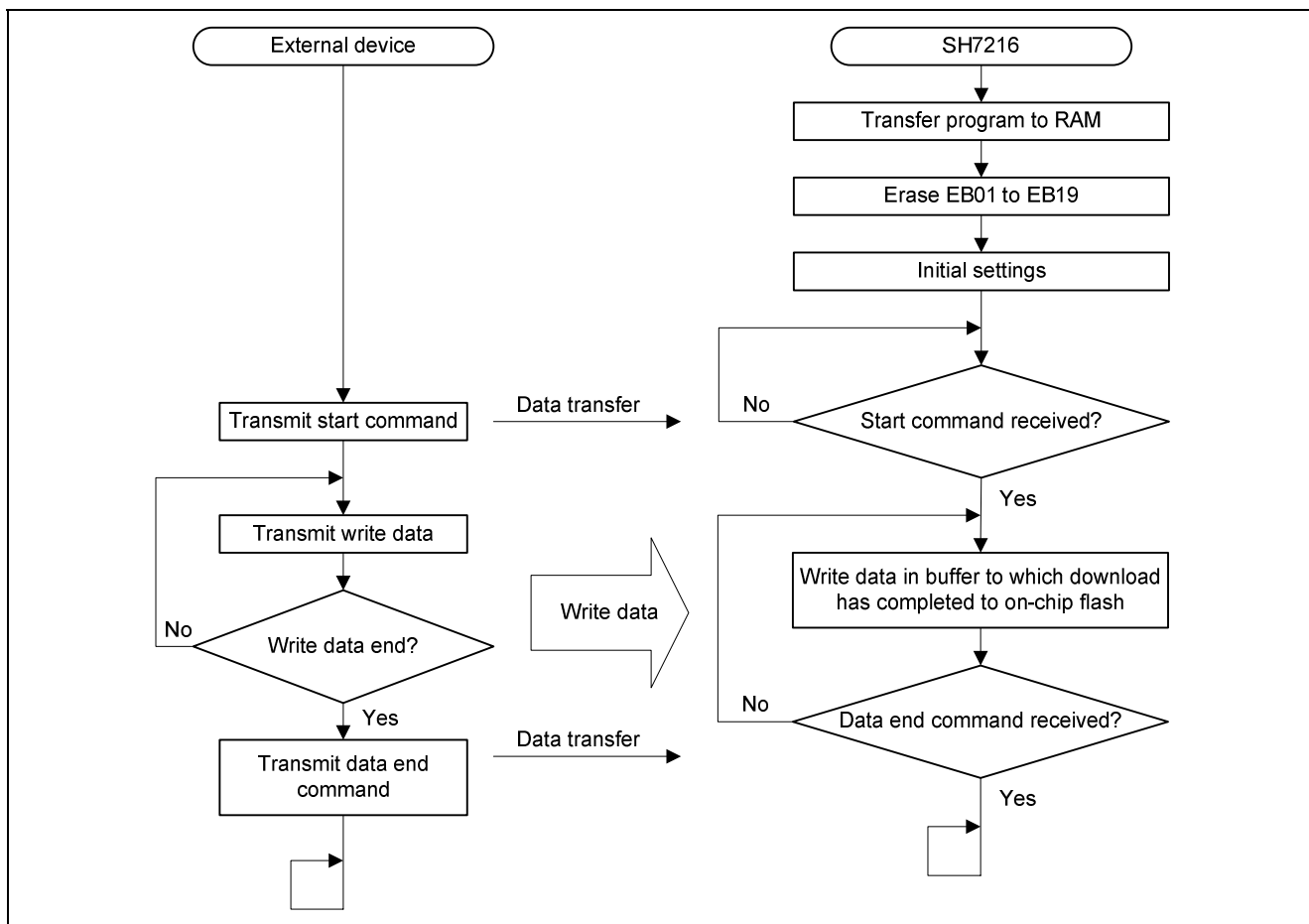


Figure 6 Overall Operation Sequence

3.2 Basic Specifications of Sample Program

3.2.1 Functions Used by Sample Program

Table 3 lists the control flags used in the sample application.

Table 3 Control Flags

Variable	Function	Type Declaration
buff_no	Indicates buffer number (0/1) used for download.	
write_area	Write start address in on-chip flash	
on_write0	Indicates the on-chip flash write state of buffer 0. 0 (BUFF_OFF): No data write in progress 1 (BUFF_ON): Data write in progress	
on_write1	Indicates the on-chip flash write state of buffer 1. 0 (BUFF_OFF): No data write in progress 1 (BUFF_ON): Data write in progress	
buff0_full	Indicates the download state of buffer 0. 0 (BUFF_OFF): Buffer empty 1 (BUFF_ON): Buffer data full	
buff1_full	Indicates the download state of buffer 1. 0 (BUFF_OFF): Buffer empty 1 (BUFF_ON): Buffer data full	
dl_number	Data download count	

3.2.2 Control Functions of Sample Program

Table 4 lists the functions used in the sample application.

Table 4 List of Functions Used

Function Name	Function	Remarks
main	Erases on-chip flash and makes initial settings.	Figure 10
ROM_WE_MAIN	Processes writing to on-chip flash (writing of buffer data using control flags).	Figure 11
INTR_RCANET	RCAN receive interrupt (data reception from external device)	Figure 15
can_init	Initializes RCAN.	Figure 12
R_FlashErase	Erases specified block.	Standard API
R_FlashWrite	Writes data to specified address.	

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3.2.3 Section Settings of Sample Program

Table 5 lists the section settings used in the sample application.

Table 5 Sample Program Section Settings

Section Name	Address	Description	Remarks
DVECTTBL	H'0000_0000	Vector table	On-chip flash
DINTTBL			
PResetPRG		Reset handler	
PIntPRG		Exception handler	
P	H'0000_1000	Program area	
PFRAM		Standard API	
C\$BSEC		Constant area	
C\$DSEC			
D		Initialization data area	
RDVECTTBL	H'FFF8_0000	Vector table (allocated in RAM)	On-chip RAM
RDINTTBL			
RResetPRG		Reset handler (allocated in RAM)	
RIntPRG		Exception handler (allocated in RAM)	
RP	H'FFF8_1000	Program area (allocated in RAM)	
RPFAM		Standard API (allocated in RAM)	
RC\$BSEC		Constant area (allocated in RAM)	
RC\$DSEC			
B	H'FFF8_4000	Uninitialized data area	
R		Initialization data area (allocated in RAM)	
S	H'FFF9_FC00	Stack area	

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3.2.4 Register Settings of Sample Program

Table 6 lists the register settings used in the sample application.

Table 6 Register Settings

Register Name	Address	Setting Value	Description
Interrupt priority register 18 (IPR18)	H'FFFE0018	0x0F00	Set interrupt priority level to 15.
Port A control register (PACRL1)	H'FFFE3816	0x0055	Set PJ0 and PJ1 to CTx_A and CRx_A.
Port A I/O register L (PAIORL)	H'FFFE3816	0x0002	
Standby control register (STBCR6)	H'FFFE041C	H'CF	MSTP64 = 0: Controller area network operates.
Master control register (MCR)	H'FFFFD000	H'0001	MCR0 = 1: Reset mode transition request
		H'8001	MCR15 = 1: Different orders for RCAN-ET and HCAN2
		H'8000	MCR0 = 0: Reset mode canceled
Interrupt mask register (IMR)	H'FFFFD00A	H'FFFD	Controller area network data frame received interrupt enabled
Mailbox interrupt mask register 0 (MBIMR0)	H'FFFFD052	H'FFEA	Controller area network interrupts enabled (MB0, MB2, MB4)
Bit configuration register 1 (BCR1)	H'FFFFD004	H'F700	TSEG1[3:0] = B'1111 PRSEG;PHSEG1 = 16Tq TSEG2[2:0] = B'1111: PSEG2 = 8Tq SJW = 0: SJW = 1Tq BSP = 0: Bit sampling at one point
Bit configuration register 0 (BCR0)	H'FFFFD006	H'0001	BRP[7:0] = 3: 1Tq = 2xPφ
Mailbox 0 message control field (MB[0]CONTROL1H)	H'FFFFD110	H'0200	MBC[2:0] = B'010 data frame and remote frame reception enabled
Mailbox 1 message control field (MB[1]CONTROL1H)	H'FFFFD130	H'0001	MBC[2:0] = B'000 data frame and remote frame transmission enabled
Mailbox 2 message control field (MB[2]CONTROL1H)	H'FFFFD150	H'0200	MBC[2:0] = B'010 data frame and remote frame reception enabled
Mailbox 4 message control field (MB[4]CONTROL1H)	H'FFFFD190	H'0200	MBC[2:0] = B'010 data frame and remote frame reception enabled
Mailbox 0 local acceptance filter mask (MB[0]LAFMH)	H'FFFFD104	H'00000000	Clear: No mask setting

3.3 Flowcharts

Figures 7 to 12 show the operation sequences of the functions used in the sample application.

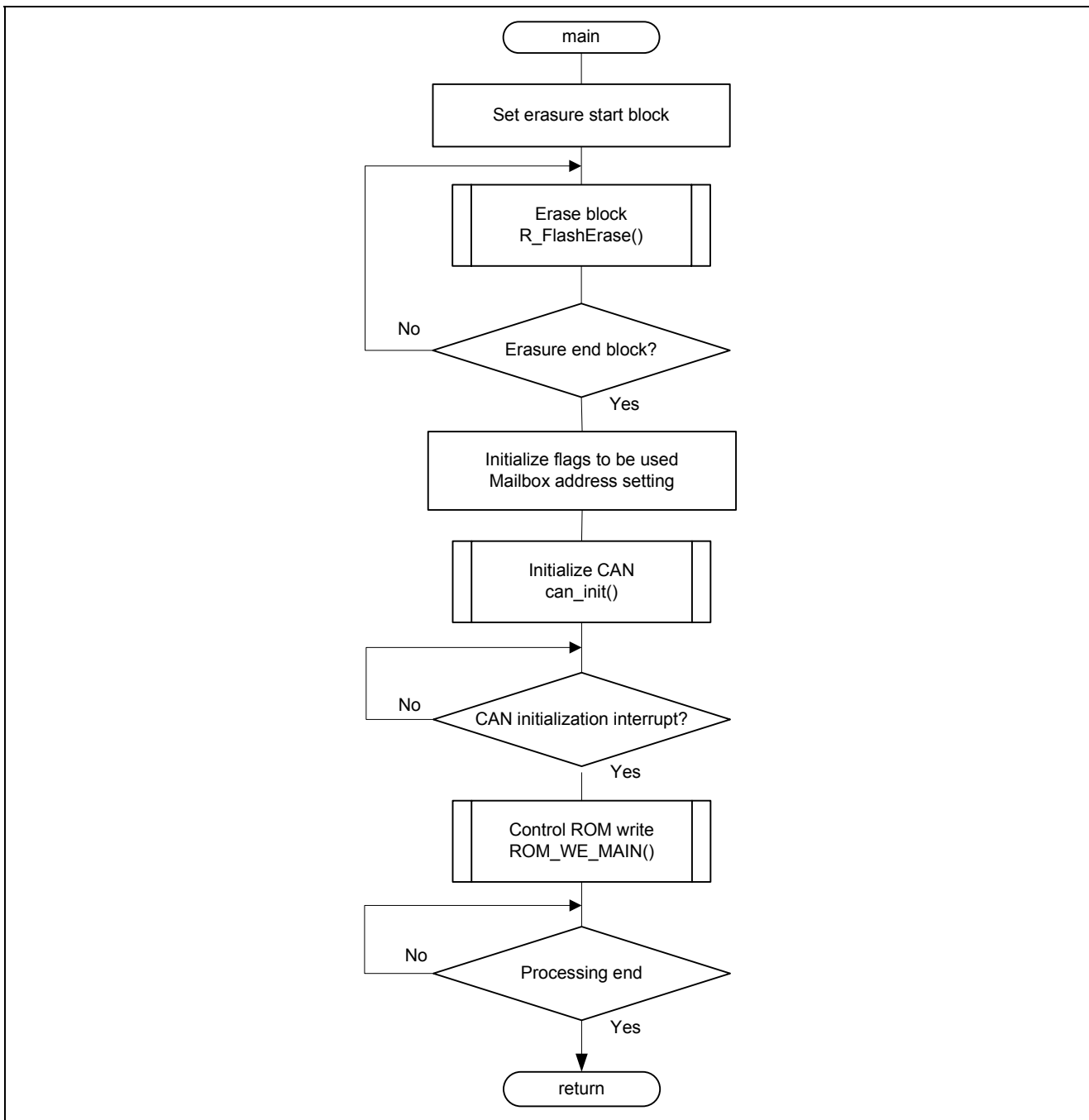


Figure 7 Main Process Sequence

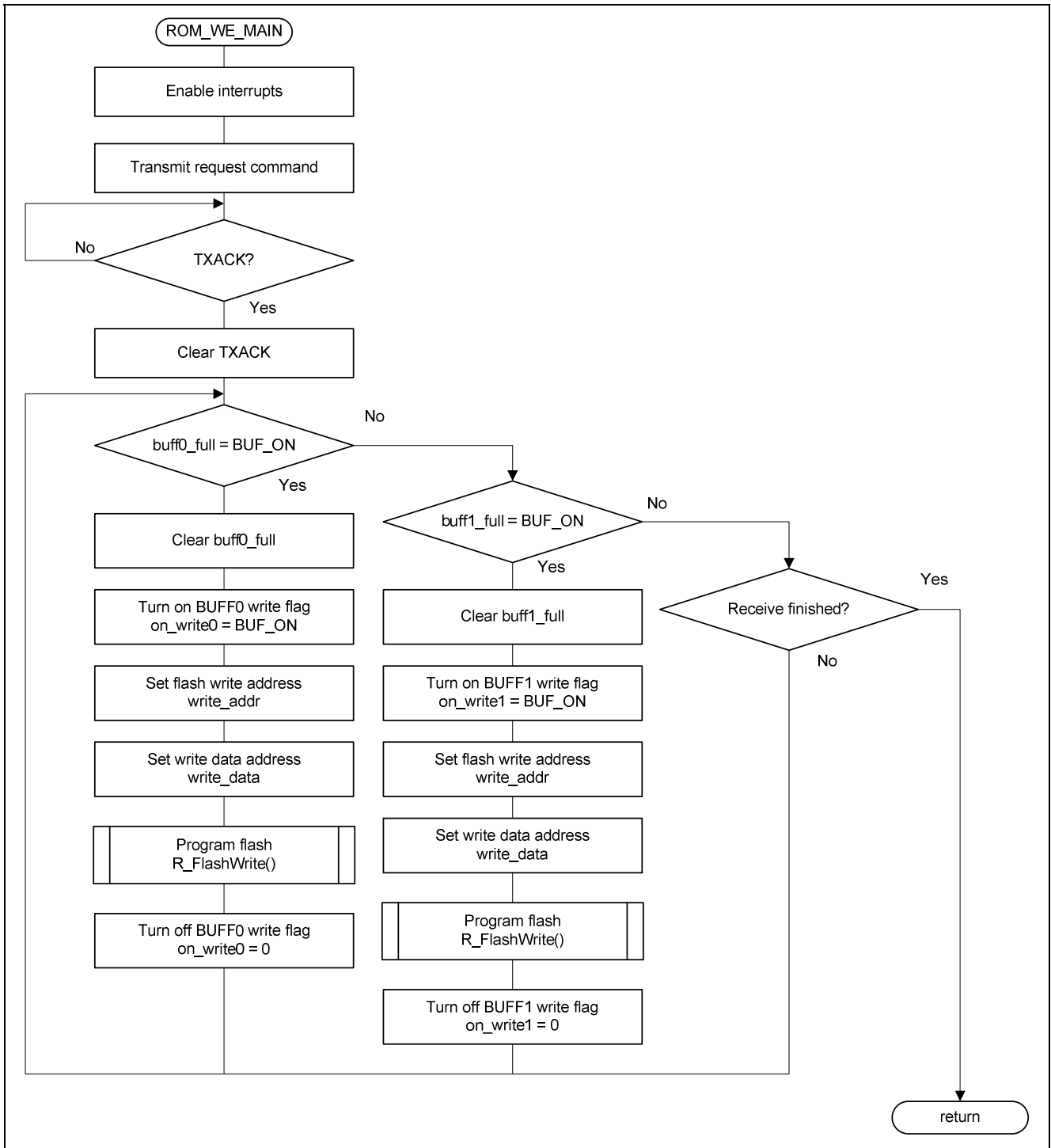


Figure 8 On-Chip Flash Programming Sequence

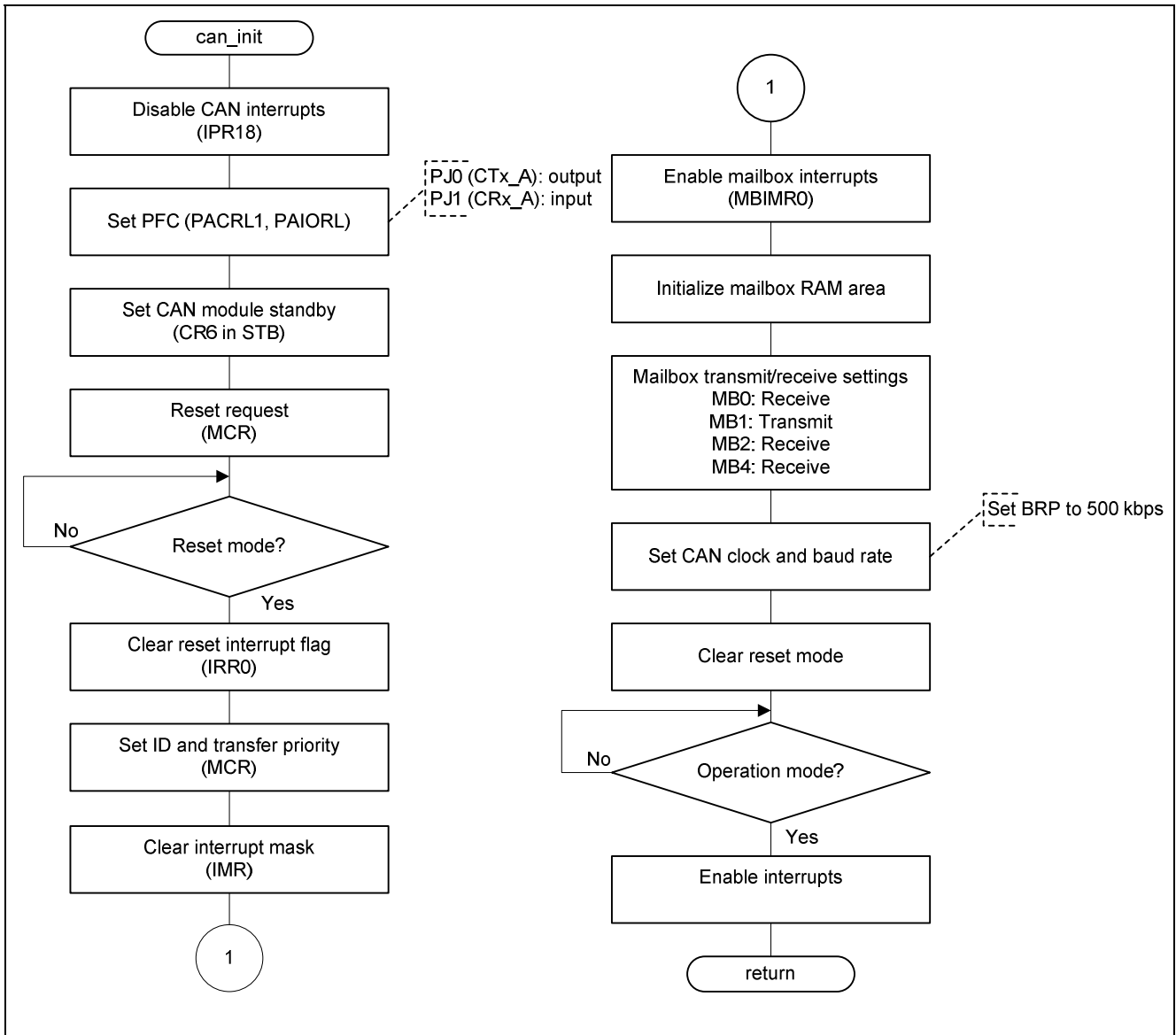


Figure 9 RCAN Initialization Sequence

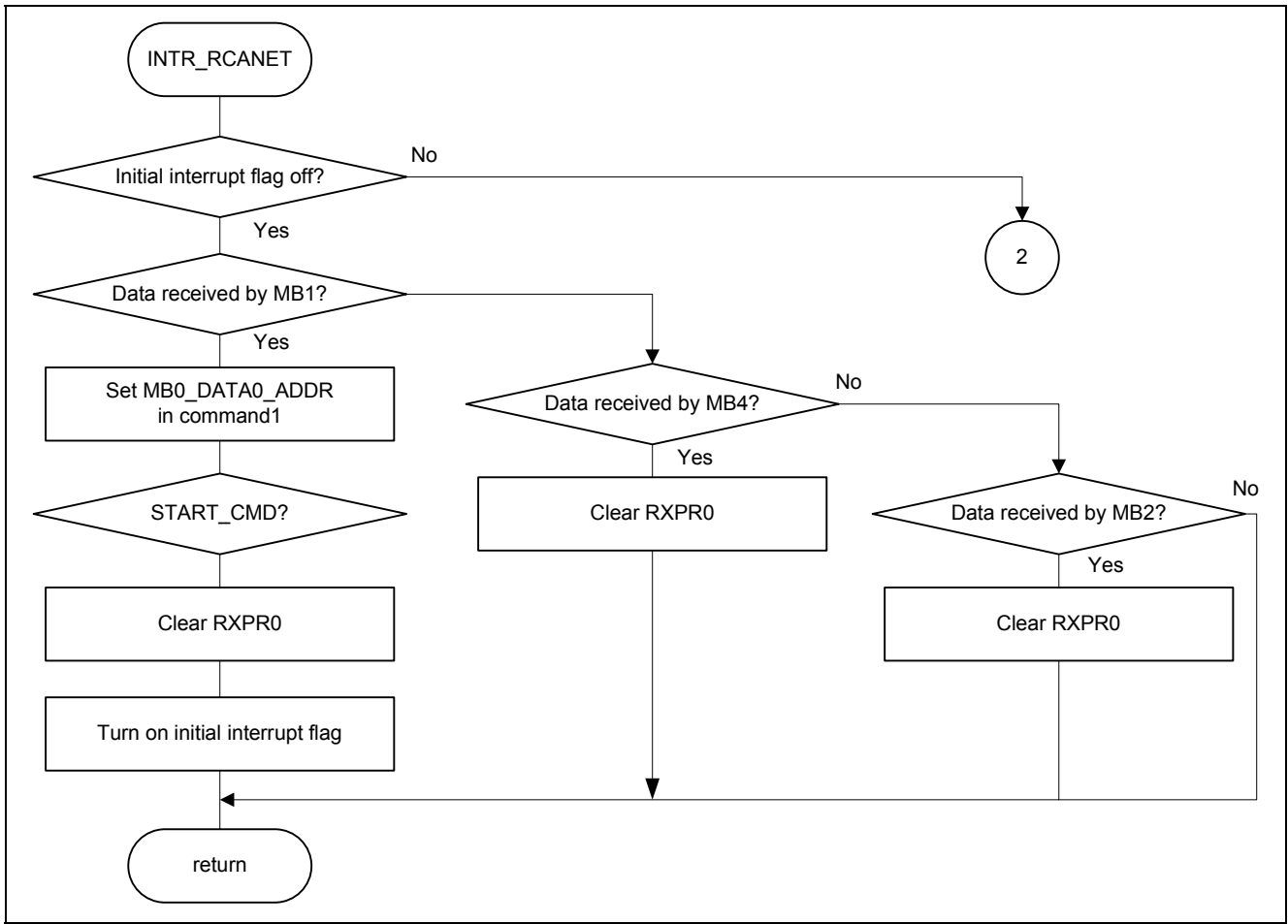


Figure 10 Receive Interrupt Sequence (1)

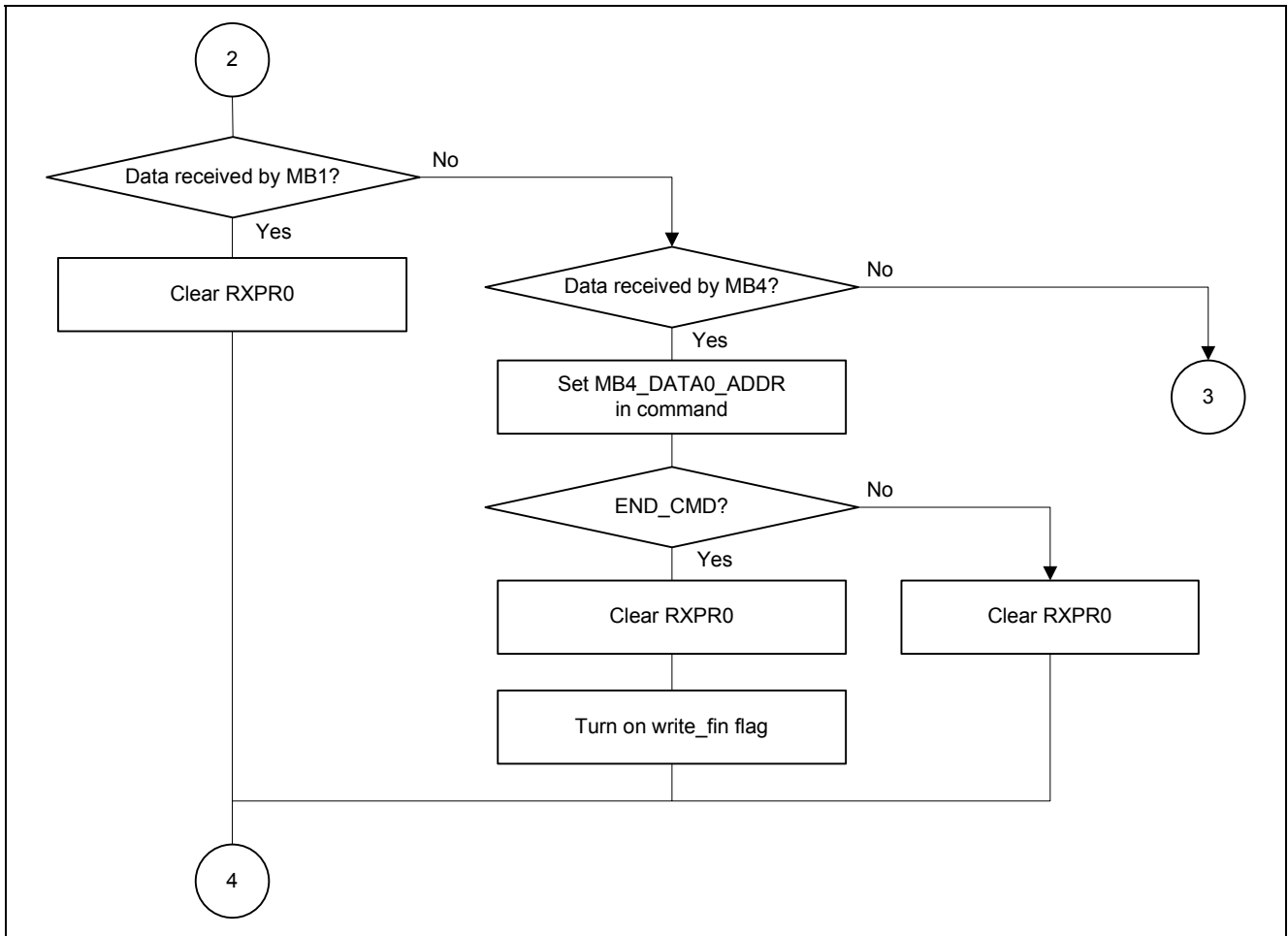


Figure 11 Receive Interrupt Sequence (2)

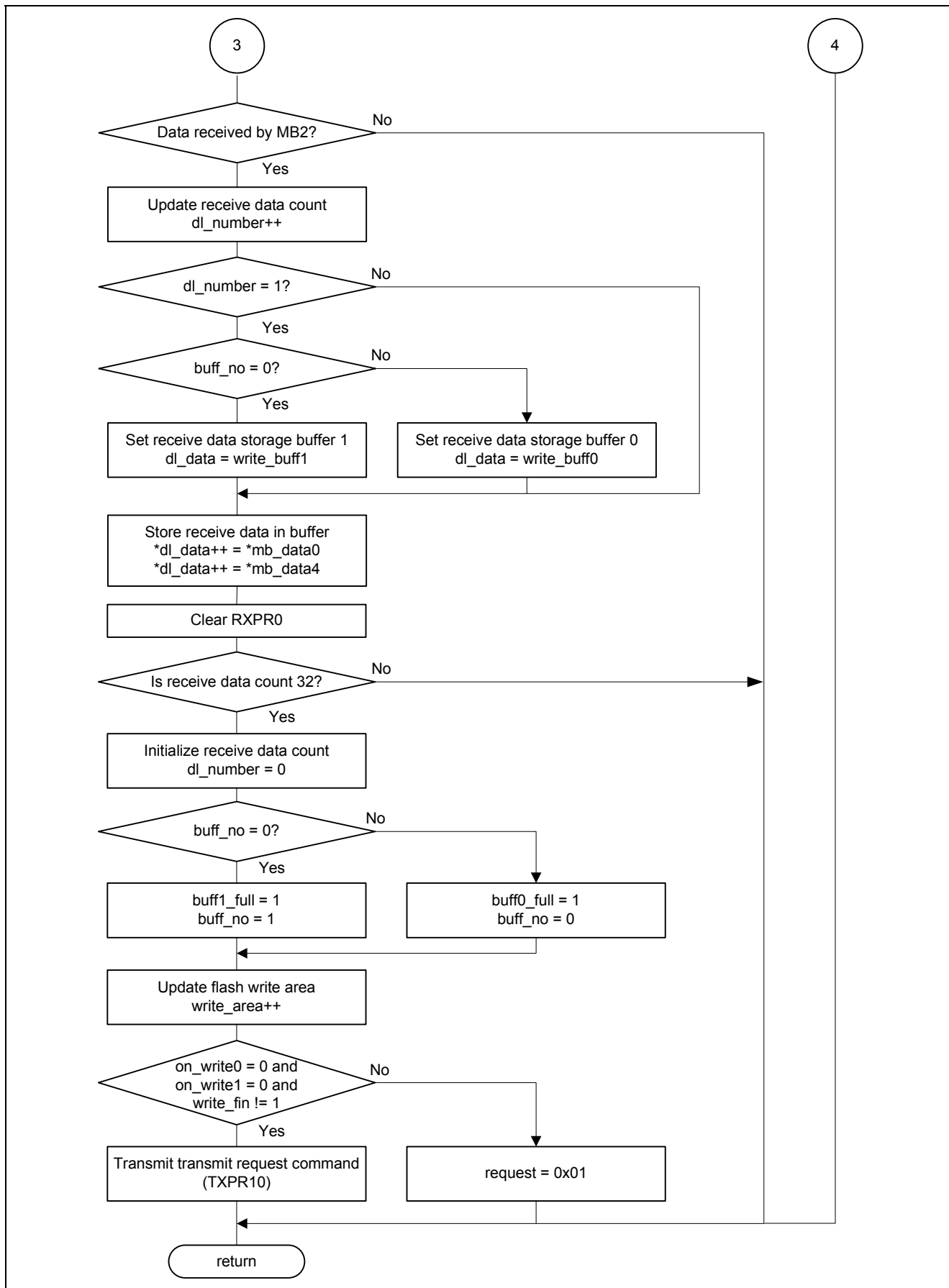


Figure 12 Receive Interrupt Sequence (3)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jun.20.10	—	First edition issued
2.00	Dec.14.10	—	Amended to use simple flash API for SH-2 and SH-2A Revised overall
2.10	Feb.28.11	—	Added read after FRQCR settings

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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