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# SH7216 Group

R01AN0528EJ0110

Rev.1.10

## Delayed Activation of A/D Converter by MTU2

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Feb 28, 2011

### Introduction

This application note describes the settings for delayed activation of the A/D converter during complementary pulse width modulation (PWM) waveform three-phase output using multi-function timer pulse unit 2 (MTU2) of the SH7216. This function can be used to perform A/D conversion at a timing specified by the user.

### Target Device

SH7216

### Contents

1. Preface .....	2
2. Overview .....	4
3. Documents for Reference .....	18

## 1. Preface

### 1.1 Specifications

The sample program activates the A/D converter at a user-defined timing during complementary PWM waveform three-phase output from channels 3 and 4 (ch3 and ch4) of MTU2. The basic specifications of this sample task are listed below.

- MTU2 ch3 and ch4 output a three-phase complementary PWM waveform with dead time, and output on TIOC3A toggles in synchronization with the cycle.
- When TCNT\_4 counts up, the A/D converter is activated at a compare-match between TCNT\_4 and TADCORA\_4.
- The A/D conversion start timing is updated when a ch3 compare-match interrupt occurs.
- The A/D converter operates in single mode.
- The A/D conversion result is stored in the on-chip RAM when the A/D conversion end interrupt occurs.

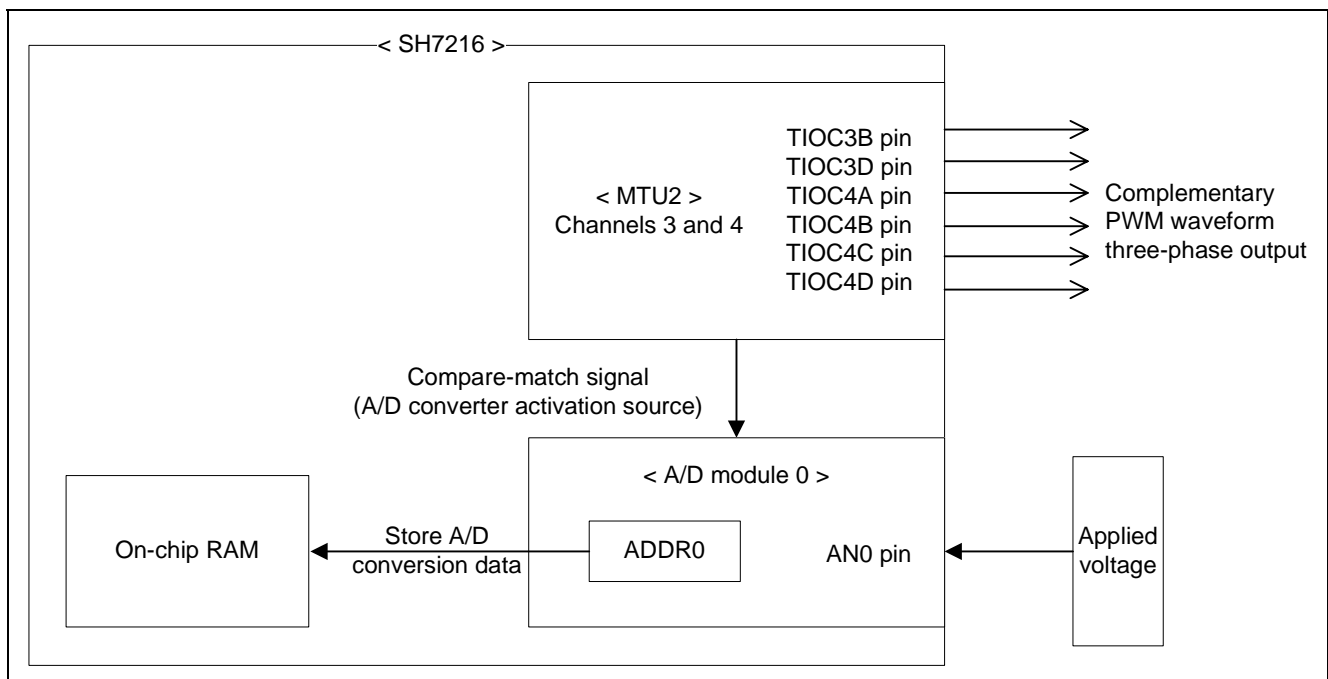


Figure 1 Block Diagram of A/D Conversion Using MTU2

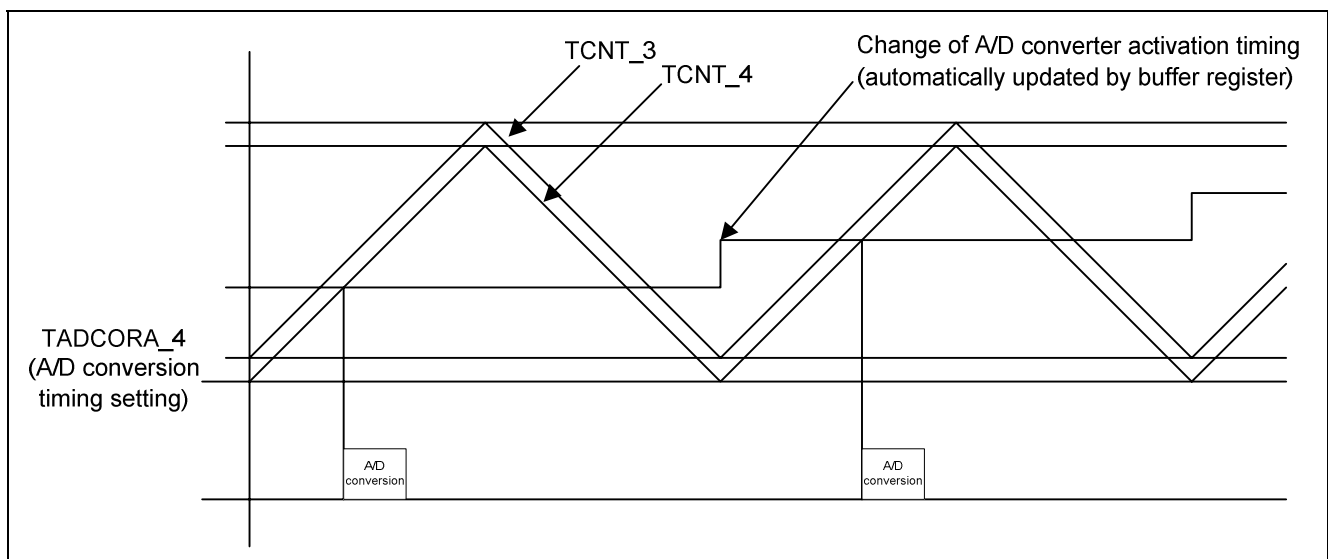


Figure 2 Activation of A/D Converter

## 1.2 Functions

- A/D converter (ADC)
- Multi-function timer pulse unit 2 (MTU2)
- Clock pulse generator (CPG)
- Pin function controller (PFC)
- Interrupt controller (INTC)

## 1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz MTU2S clock: 100 MHz AD clock: 50 MHz
Integrated development environment	Renesas Electronics High-Performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver.9.03.00 Release02
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu -pic=1 -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chginpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

## 1.4 Related Application Notes

Application notes related to this application note are listed below. Refer to them in conjunction with this application note.

- SH7216 Group Application Note: A/D Converter Activation at MTU2 Channel 0 Compare-Match
- SH7216 Group Application Note: A/D Converter Activation Skipping Using MTU2

## 2. Overview

The sample program uses the A/D conversion start request delay function of multi-function timer pulse unit 2 (MTU2) to activate the A/D converter (ADC).

### 2.1 Operation of Functions

#### 2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 3 is a block diagram of MTU2, and figure 4 is a block diagram of MTU2 (ch3 and ch4) as used by the A/D conversion start request delay function.

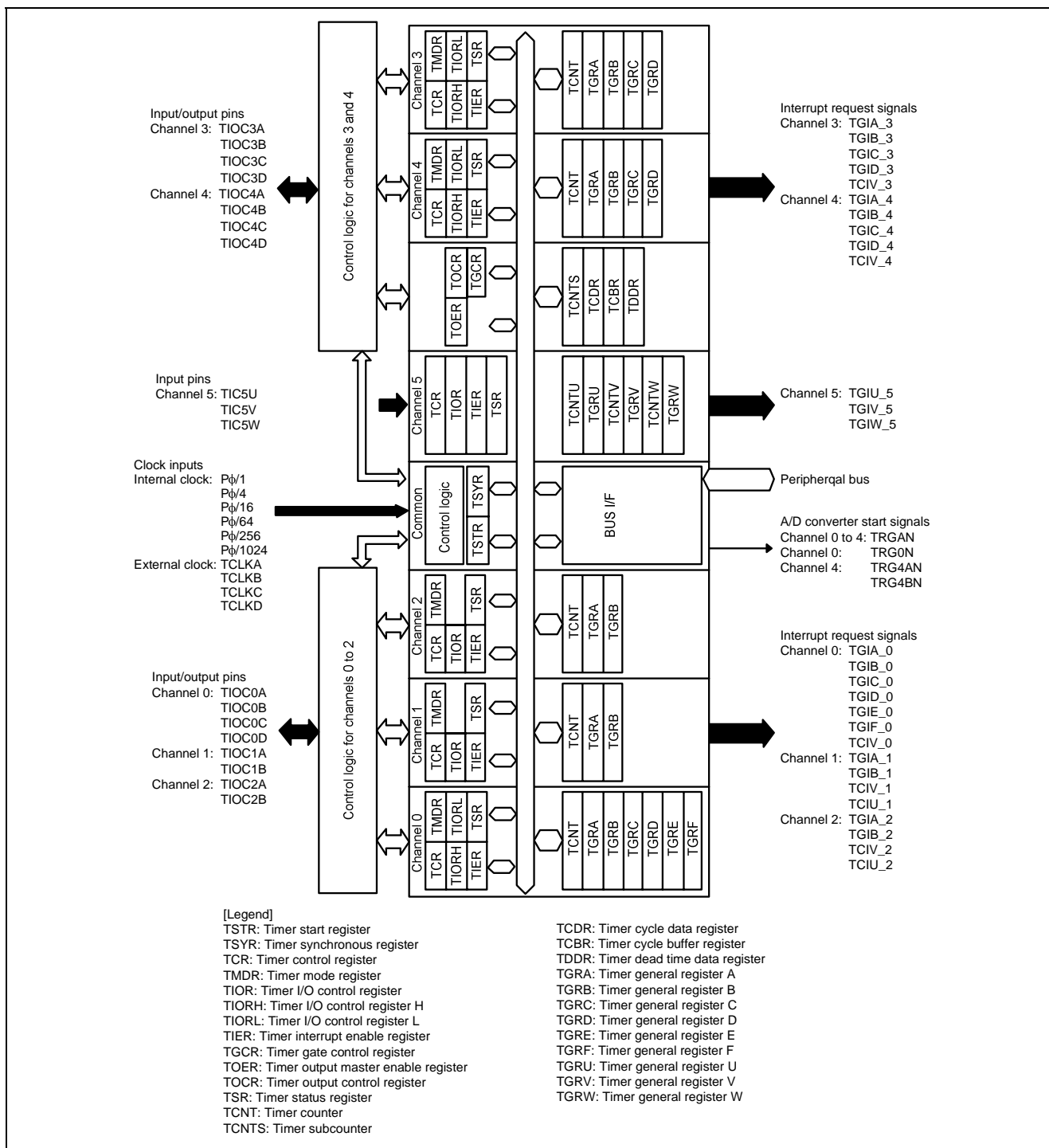
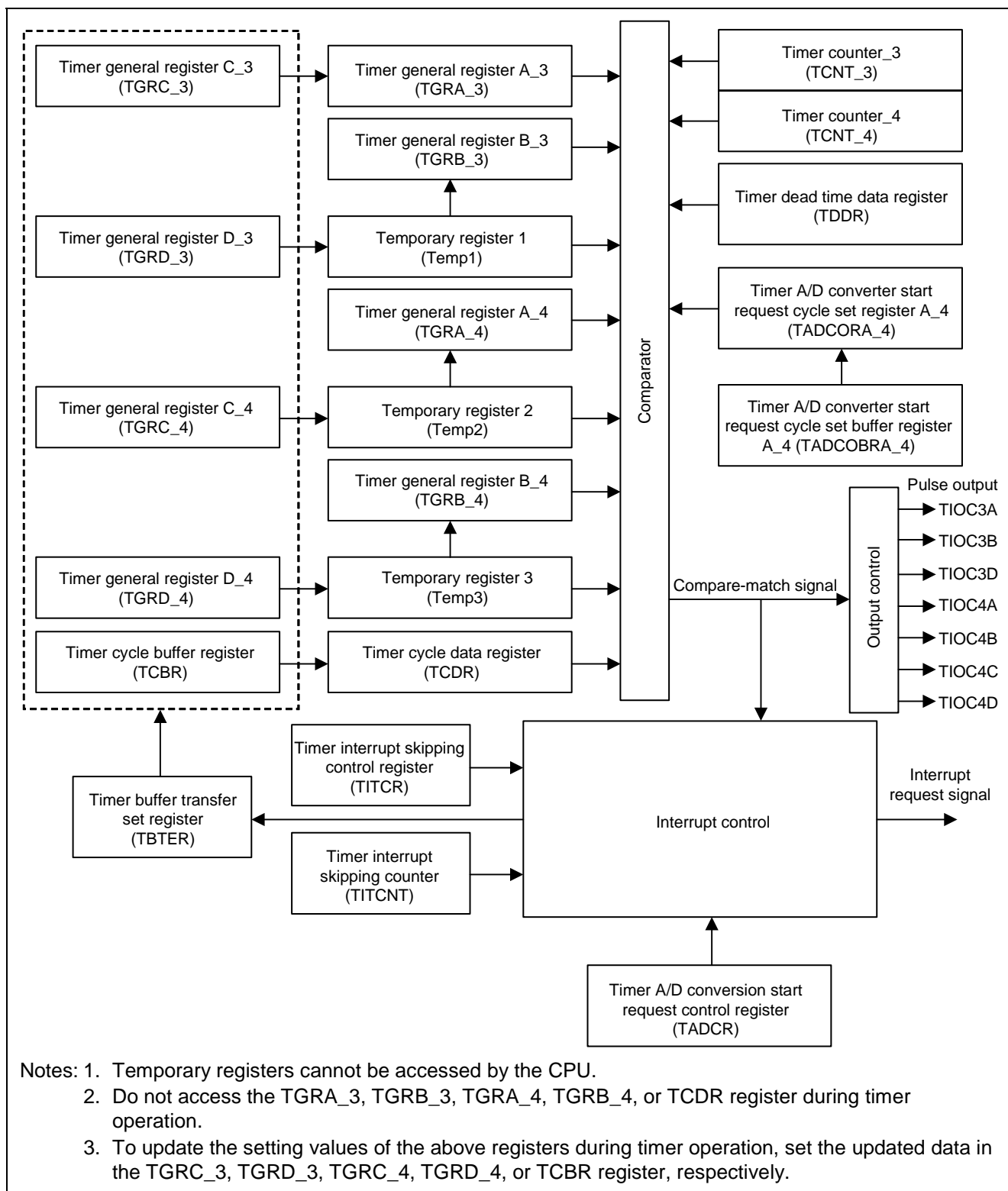


Figure 3 MTU2 Block Diagram



**Figure 4 Block Diagram of MTU2 (ch3 and ch4) as Used by A/D Conversion Start Request Delay Function**

- Timer general register A\_3 (TGRA\_3) operates as a compare register. A value equal to one-half the PWM cycle is set in TGRA\_3. To change the value of this register while the timer is operating, set the new value in timer general register C\_3 (TGRC\_3).
- Timer general register B\_3 (TGRB\_3) operates as a compare register. The duty of the PWM waveforms output by pins TIOC3B and TIOC3D is set in TGRB\_3. To change the value of this register while the timer is operating, set the new value in timer general register D\_3 (TGRD\_3).
- Timer general register C\_3 (TGRC\_3) operates as a buffer register for TGRA\_3. While the timer is operating, TGRA\_3 is updated to reflect values set in TGRC\_3.
- Timer general register D\_3 (TGRD\_3) operates as a buffer register for TGRB\_3. When a value is changed in TGRD\_3 while the timer is operating, the new value is transferred to a temporary register (Temp1) and then to TGRB\_3.
- Timer general register A\_4 (TGRA\_4) operates as a compare register. The duty of the PWM waveforms output by pins TIOC4A and TIOC4C is set in TGRA\_4. To change the value of this register while the timer is operating, set the new value in timer general register C\_4 (TGRC\_4).
- Timer general register B\_4 (TGRB\_4) operates as a compare register. The duty of the PWM waveforms output by pins TIOC4B and TIOC4D is set in TGRB\_4. To change the value of this register while the timer is operating, set the new value in timer general register D\_4 (TGRD\_4).
- Timer general register C\_4 (TGRC\_4) operates as a buffer register for TGRA\_4. While the timer is operating, TGRA\_4 is updated to reflect values set in TGRC\_4.
- Timer general register D\_4 (TGRD\_4) operates as a buffer register for TGRB\_4. While the timer is operating, TGRB\_4 is updated to reflect values set in TGRD\_4.
- Temporary registers 1, 2, and 3 (Temp1, Temp2, and Temp3) occupy a position between the buffer registers and compare registers. Data written to the buffer register is transferred to the temporary register and then to the compare register. The temporary registers cannot be accessed by the CPU.
- Timer counter 3 (TCNT\_3) is a 16-bit readable/writable counter. TCNT\_3 starts counting down when a compare match with TGRA\_3 occurs, and it starts counting up when a compare match with the timer dead time data register (TDDR) occurs.
- Timer counter 4 (TCNT\_4) is a 16-bit readable/writable counter. TCNT\_4 starts counting down when a compare match with the timer cycle data register (TCDR) occurs, and it starts counting up when the value of TCNT\_4 reaches H'0000.
- The timer dead time data register (TDDR) is a 16-bit readable/writable register. TDDR specifies the dead time for the PWM waveforms.
- The timer cycle data register (TCDR) is a 16-bit readable/writable register. TCDR specifies a value equal to one-half the PWM carrier cycle.
- The timer cycle buffer register (TCBR) operates as the buffer register for TCDR. While the timer is operating, TCDR is updated to reflect values set in TCBR.
- The timer interrupt skipping control register (TITCR) enables/disables interrupt skipping and sets the skipping count. Skipping can be enabled for the TCNT\_3 compare-match interrupt (TGIA\_3) and TCNT\_4 underflow interrupt (TCIV\_4) in complementary PWM mode. The maximum skipping count that can be specified is seven.
- The timer interrupt skipping counter (TITCNT) counts the number of interrupts that have been skipped. TITCNT is cleared when the count value matches skipping count setting.
- The timer buffer transfer set register (TBTER) enables or disables transfer from the buffer registers to temporary registers. It also specifies whether or not transfers are linked to the interrupt skipping function when transfer is not disabled.
- The timer A/D conversion start request control register (TADCR) is a 16-bit readable/writable register. It enables or disables A/D conversion start requests and specifies whether or not such requests are linked to the interrupt skipping function.
- Timer A/D converter start request cycle set register A\_4 (TADCORA\_4) is a 16-bit readable/writable register. When TCNT\_4 matches the value of this register, the corresponding A/D conversion start request is issued.
- Timer A/D converter start request cycle set buffer register A\_4 (TADCOBRA\_4) operates as the buffer register for TADCORA\_4. While the timer is operating, TADCORA\_4 is updated to reflect values set in TADCOBRA\_4.

### 2.1.2 A/D converter

In the sample program A/D module 0 is activated by MTU2 at the A/D conversion start trigger (TRG4AN), and A/D conversion takes place in single-cycle scan mode. Figure 5 is a block diagram of the A/D0 module, and its functions are described below.

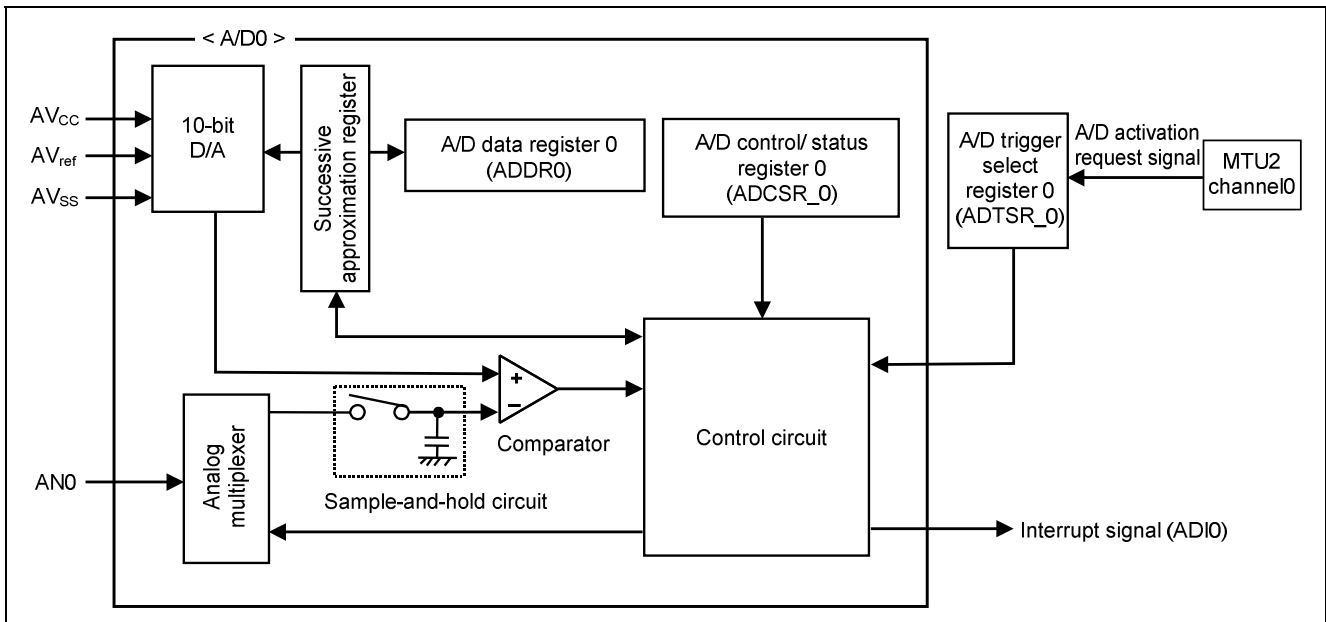


Figure 5 Block Diagram of A/D Module 0

- A/D data register 0 (ADDR0) is a 16-bit read-only register that stores the conversion result from analog input channel (AN0). The conversion data is stored in bits 15 to 6 of ADDR, and the value of the lower 6 bits is always 0.
- A/D control/status register 0 (ADCSR\_0) controls A/D conversion operation.
- A/D trigger select register 0 (ADTSR\_0) is set to external trigger for A/D conversion start requests.

## 2.2 Operation of Sample Program

Table 1 lists the settings used by the sample program and figure 6 illustrates its operation.

**Table 1 Settings of Sample Program**

Function	Item	Setting	
General	Frequency	$I\phi = 200\text{MHz}$ , $B\phi = P\phi = 50\text{MHz}$ , $M\phi = 100\text{MHz}$ , $A\phi = 50\text{MHz}$	
	Register banks used	Enabled for all interrupt levels	
	Interrupt mask level	0	
MTU2	Channels	Channels 3 and 4	
	Operating mode	Complementary PWM mode 3 (data transfer at counter peak and trough)	
	Pin functions	<ul style="list-style-type: none"> <li>• TIOC3A pin: Output toggles in synchronization with PWM cycle</li> <li>• TIOC3B pin: PWM output 1 (positive-phase waveform)</li> <li>• TIOC3D pin: PWM output 1 (negative-phase waveform)</li> <li>• TIOC4A pin: PWM output 2 (positive-phase waveform)</li> <li>• TIOC4C pin: PWM output 2 (negative-phase waveform)</li> <li>• TIOC4B pin: PWM output 3 (positive-phase waveform)</li> <li>• TIOC4D pin: PWM output 3 (negative-phase waveform)</li> </ul>	
	Active level	<ul style="list-style-type: none"> <li>• Positive-phase output: Active-low output</li> <li>• Negative-phase output: Active-low output</li> </ul>	
	Counter clock	$P\phi/4 = 12.5\text{ MHz}$	
	PWM duty	Fixed (can be updated when TGRA_3 compare-match interrupt (TGIA3) occurs)	
	Interrupt used	TGRA_3 compare-match interrupt (TGIA3), interrupt level 10	
	ADC	Module used	A/D_0
		Conversion target pin	AN0
		Conversion mode	Single-cycle scan mode
ADDR auto-clear		Disabled	
A/D conversion end interrupt		Enabled, interrupt level 10	
A/D activation source		MTU2 (TRG4AN)	
A/D conversion method		Impedance conversion circuit	
A/D conversion speed	50 states		



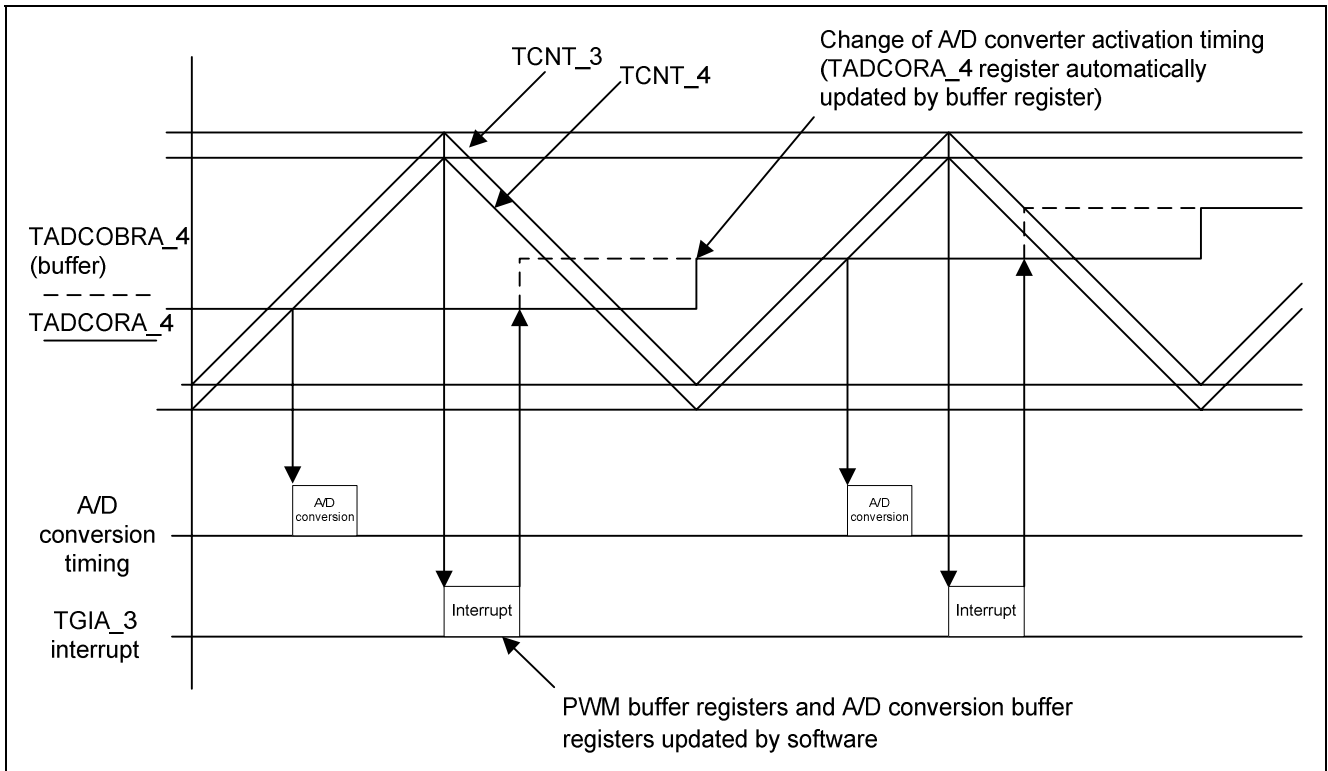


Figure 6 Operation of Sample Program

### 2.3 Setting Procedure of Sample Program

Figures 7 to 13 show the operation sequence of the sample program. For details of the various registers, see the *SH7216 Group Hardware Manual*.

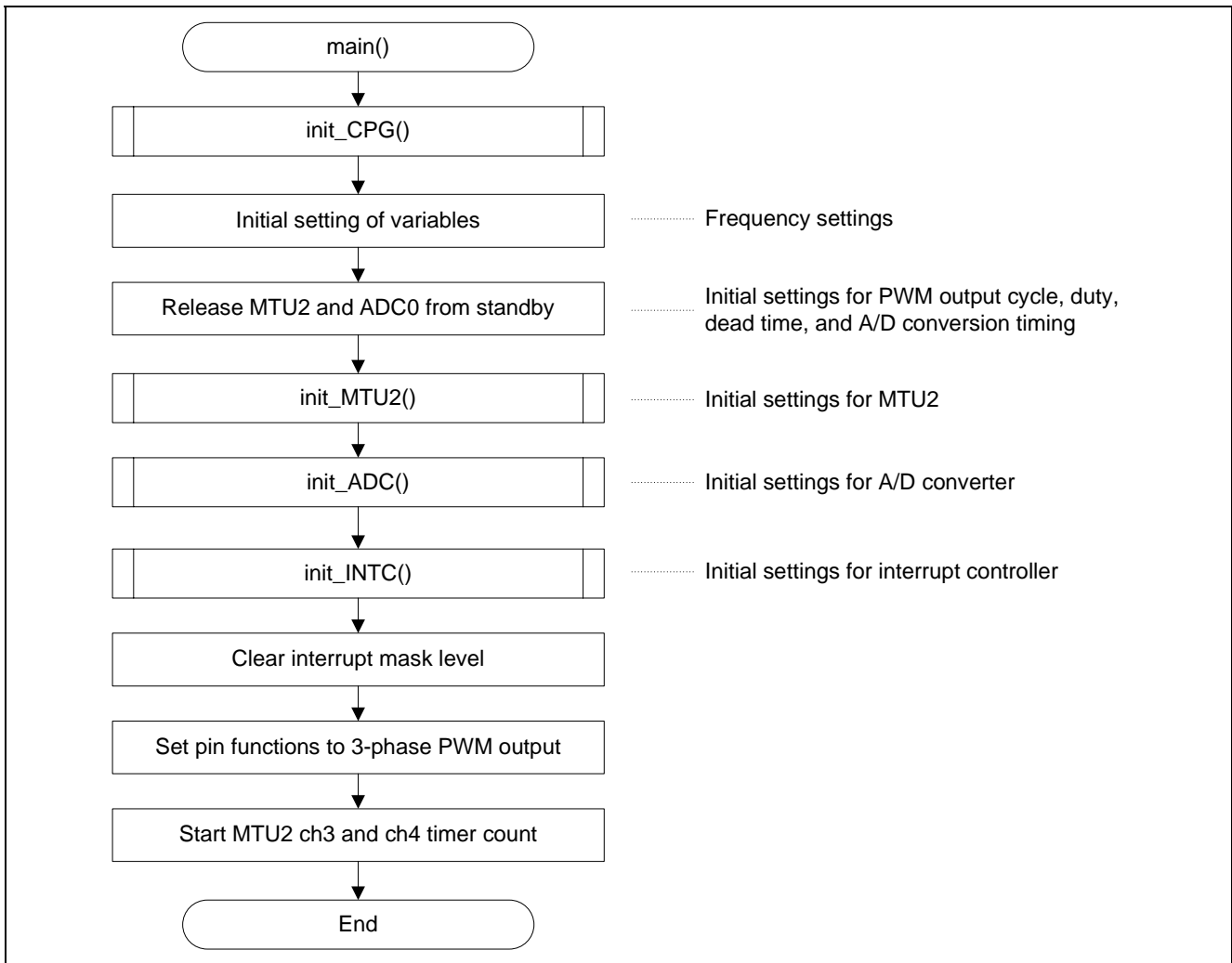


Figure 7 Main Function Sequence

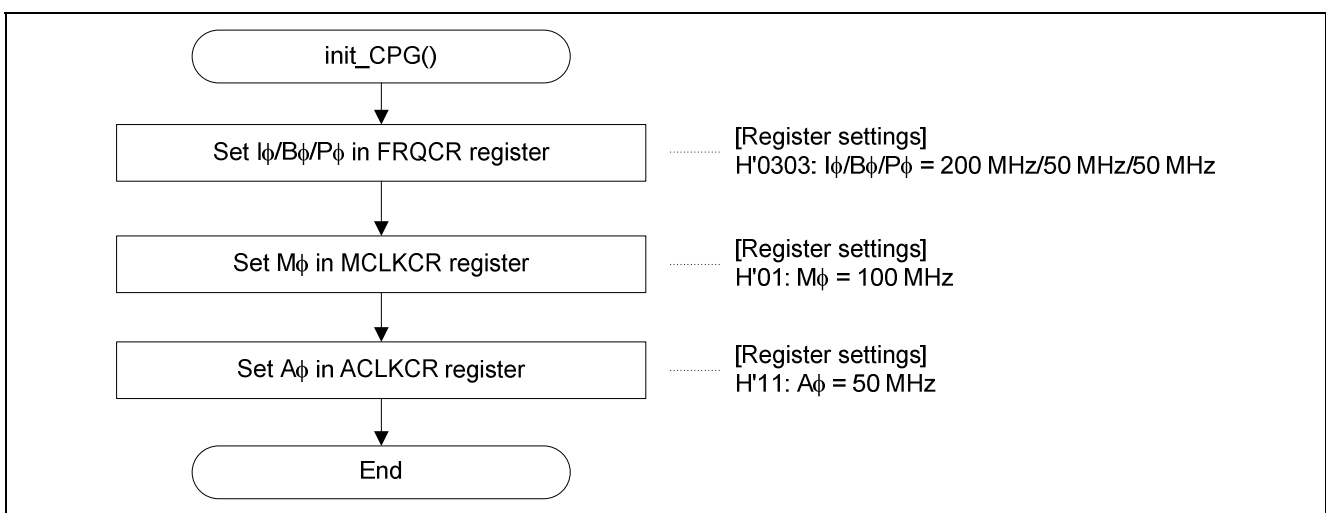


Figure 8 Frequency Setting Sequence

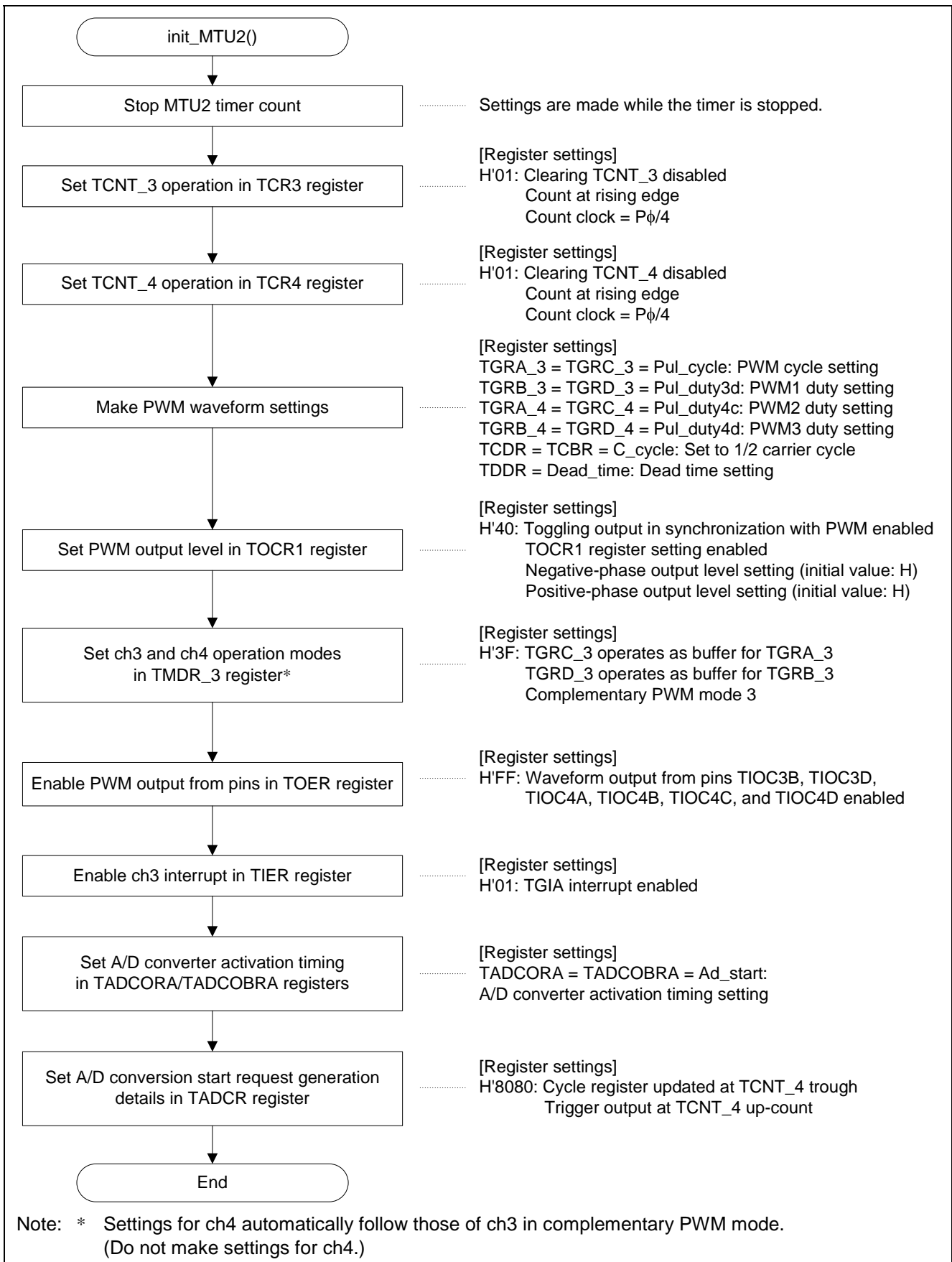


Figure 9 MTU2 Setting Sequence

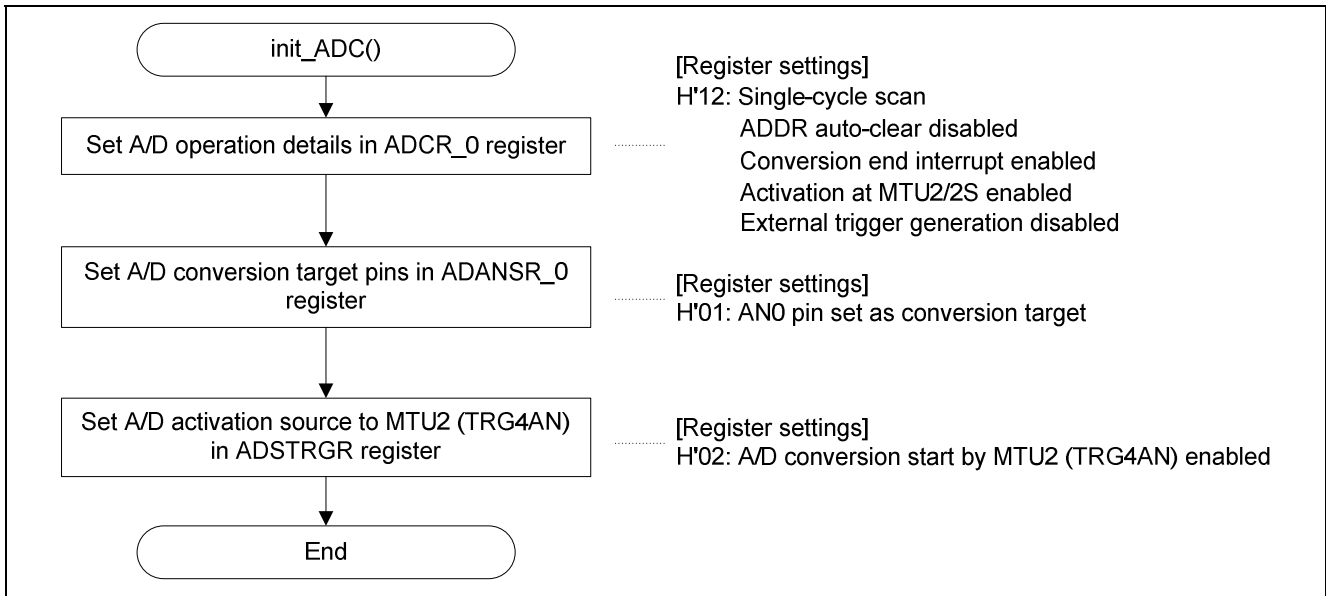


Figure 10 ADC Setting Sequence

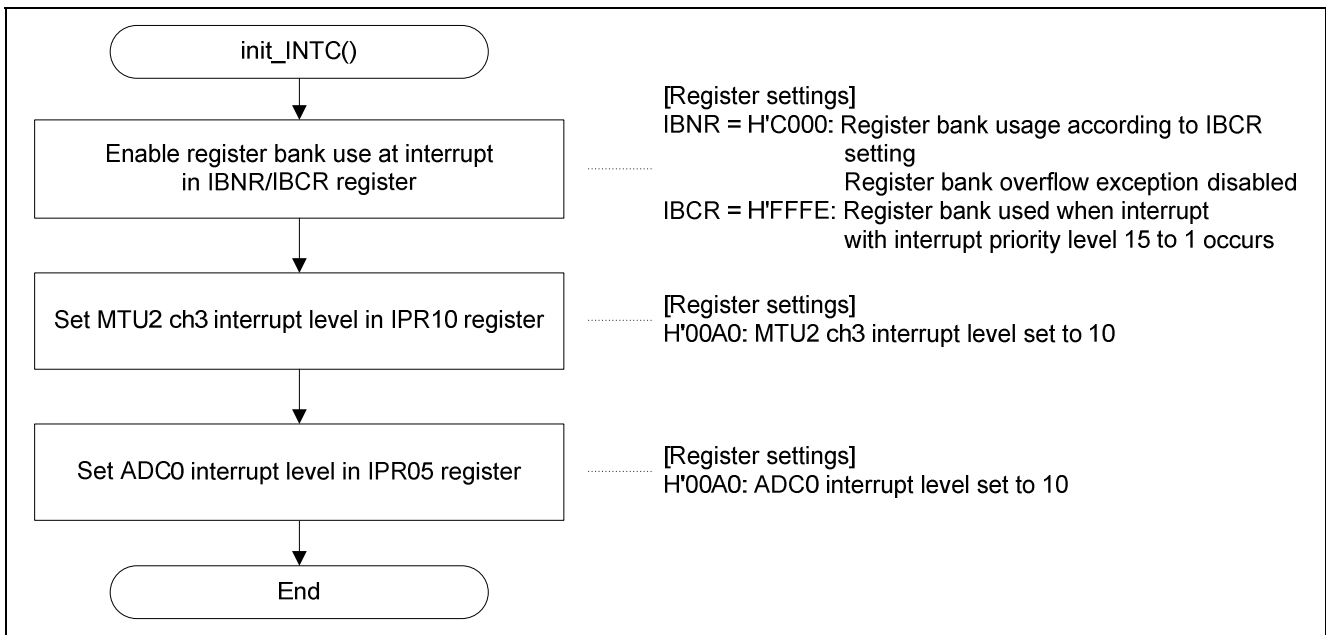


Figure 11 INTC Setting Sequence

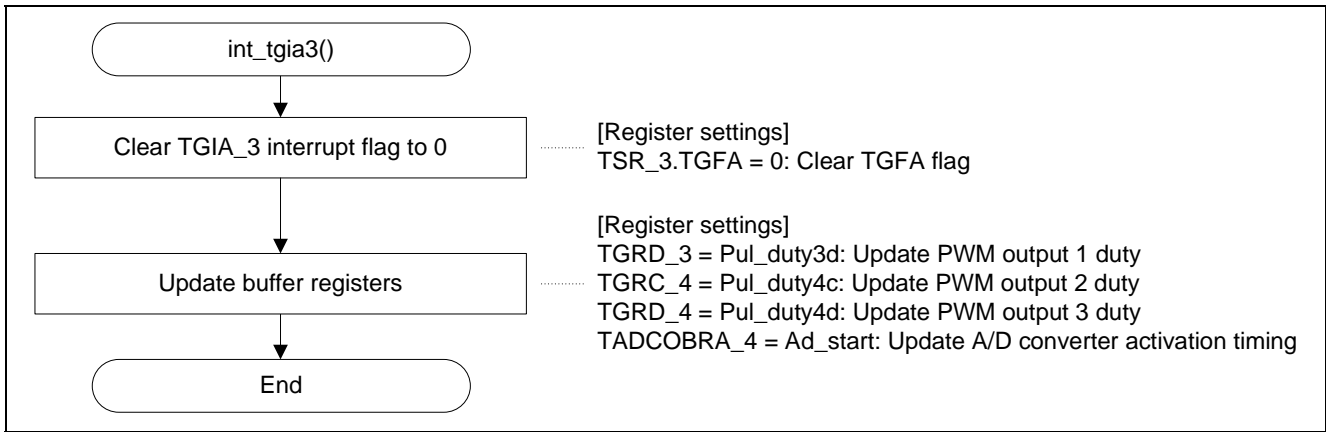


Figure 12 T GIA3 Interrupt Sequence

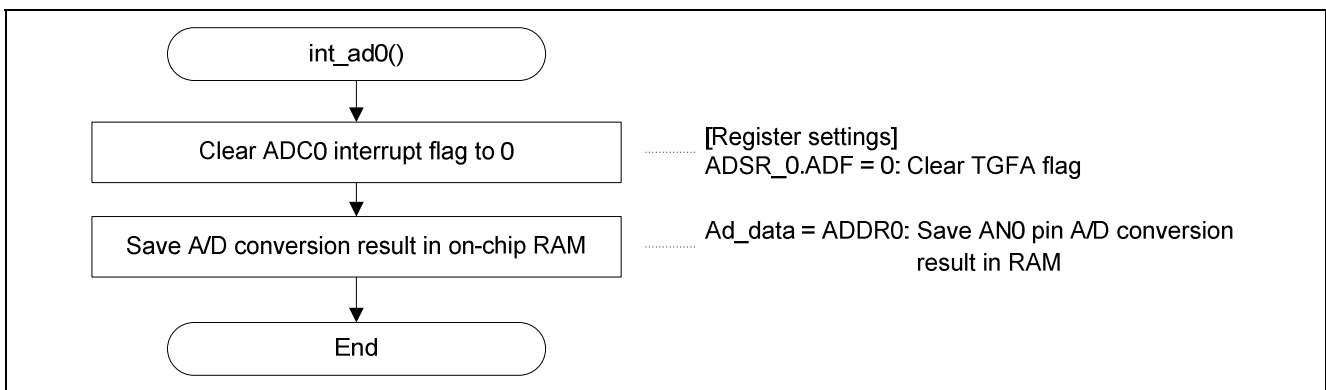


Figure 13 A/D Conversion End Interrupt Sequence

## 2.4 Register Settings of Sample Program

Table 2 lists the register settings used in the sample program.

**Table 2 Register Settings of Sample Program**

Module	Register Name	Address	Setting Value	Description
Clock pulse generator (CPG)	Frequency control register (FRQCR)	H'FFFE_0010	H'0303	STC[2:0] = B'011: $\times 1/4$ IFC[2:0] = B'000: $\times 1$ PFC[2:0] = B'011: $\times 1/4$
	MTU2S clock frequency control register (MCLKCR)	H'FFFE_0410	H'41	MSDIVS[1:0] = B'01: $\times 1/2$
	AD clock frequency control register (ACLKCR)	H'FFFE_0414	H'43	ASDIVS[1:0] = B'11: $\times 1/4$
Standby control	Standby control register 3 (STBCR3)	H'FFFE_408	H'5A	MSTP35 = B'0: MTU2 operates MSTP32 = B'0: ADC0 operates
Multi-function timer pulse unit 2 (MTU2)	Timer control register 3 (TCR_3)	H'FFFE_4200	H'01	CCLR[2:0] = B'000: TCNT3 clearing disabled CKEG[1:0] = B'00: Count at rising edge TPSC[2:0] = B'01: Count at $P\phi/4$
	Timer control register 4 (TCR_4)	H'FFFE_4201	H'01	CCLR[2:0] = B'000: TCNT4 clearing disabled CKEG[1:0] = B'00: Count at rising edge TPSC[2:0] = B'01: Count at $P\phi/4$
	Timer counter 3 (TCNT_3)	H'FFFE_4210	Dead_time	ch3 counter ch4 dead time difference setting
	Timer counter 4 (TCNT_4)	H'FFFE_4212	H'0000	ch4 counter
	Timer general register A_3 (TGRA_3)	H'FFFE_4218	Pul_cycle	Output pulse cycle setting
	Timer general register B_3 (TGRB_3)	H'FFFE_421A	Pul_duty3d	PWM output 1 duty setting
	Timer general register C_3 (TGRC_3)	H'FFFE_4224	Pul_cycle	TGRA_3 buffer register
	Timer general register D_3 (TGRD_3)	H'FFFE_4226	Pul_duty3d	TGRB_3 buffer register
	Timer general register A_4 (TGRA_4)	H'FFFE_421C	Pul_duty4c	PWM output 2 duty setting
	Timer general register B_4 (GRB_4)	H'FFFE_421E	Pul_duty4d	PWM output 3 duty setting
Timer general register C_4 (TGRC_4)	H'FFFE_4228	Pul_duty4c	TGRA_4 buffer register	

Module	Register Name	Address	Setting Value	Description
Multi-function timer pulse unit 2 (MTU2)	Timer general register D_4 (TGRD_4)	H'FFFE_422A	Pul_duty4d	TGRB_4 buffer register
	Timer cycle data register (TCDR)	H'FFFE_4214	C_cycle	Set to 1/2 carrier cycle
	Timer cycle buffer register (TCBR)	H'FFFE_4222	C_cycle	TCDR buffer register
	Timer dead time data register (TDDR)	H'FFFE_4216	Dead_time	Dead time setting
	Timer output control register 1 (TOCR1)	H'FFFE_420E	H'40	PSYE = B'1: Toggle output enabled TOCL = B'0: Writing to TOCS, OLSN, and OLSP bits enabled TOCS = B'0: TOCR1 setting enabled OLSN = B'0: Negative-phase output level setting Initial: H level Active: L level OLSP = B'0: Positive-phase output level setting Initial: H level Active: L level
	Timer output master enable register (TOER)	H'FFFE_420A	H'FF	Output on TIOC3B, TIOC4A, TIOC4B, TIOC3D, TIOC4C, and TIOC4D pins enabled
	Timer mode register_3 (TMDR_3)	H'FFFE_4202	H'3F	BFB = B'1: TGRD operates as buffer for TGRB BFA = B'1: TGRC operates as buffer for TGRA MD[3:0] = B'111: Complementary PWM mode 3 (transfer at peaks and troughs)
	Timer interrupt enable register (TIER_3)	H'FFFE_4208	H'01	TGIEA = B'1: Interrupt request (TGIA) by TGFA bit enabled
	Timer A/D conversion start request control register (TADCR)	H'FFFE_4240	H'8080	BF[1:0] = B'10: Transfer from cycle setting buffer register to cycle setting register at trough of TCNT_4 UT4AE = B'1: A/D conversion start request (TRG4AN) at TCNT_4 up-count enabled
	Timer A/D converter start request cycle set register A_4 (TADCORA_4)	H'FFFE_4244	Ad_start	A/D conversion start timing setting
	Timer A/D converter start request cycle set buffer register A_4	H'FFFE_4248	Ad_start	TADCORA_4 buffer register
	Timer start register (TSRT)	H'FFFE_4280	H'C0	CST[4:3] = B'11: TCNT_4 and TCNT_3 count operation

Module	Register Name	Address	Setting Value	Description
A/D converter (ADC)	A/D control register_0 (ADCR_0)	H'FFFF_E800	H'12	ADIE = B'1: A/D conversion end interrupt enabled TRGE = B'1: A/D conversion start at external trigger or A/D conversion start trigger from MTU2/2S enabled
	A/D start trigger select register 0 (ADSTRGR_0)	H'FFFF_E81C	H'02	STR1 = B'1: A/D conversion start by TRG4AN (MTU2)
	A/D analog input channel select register 0 (ADANSR_0)	H'FFFF_E820	H'01	ANS0 = B'1: AN0 pin set as A/D conversion target channel
Interrupt controller (INTC)	Bank number register (IBNR)	H'FFFE_080E	H'C000	BE[1:0] = B'11: Register bank usage according to IBCR setting
	Bank control register (IBCR)	H'FFFE_080C	H'FFFE	Register bank usage enabled for all interrupt priority levels
	Interrupt priority level setting register 05 (IPR05)	H'FFFE_0820	H'00A0	ADI0 interrupt priority level set to 10
	Interrupt priority level setting register 10 (IPR10)	H'FFFE_0C08	H'00A0	MTU2 ch3 interrupt (TGIA_3 to TGID_3) priority level set to 10
Pin function controller (PFC)	Port E control register L3 (PECRL3)	H'FFFE_3A12	H'4044	PE11MD[2:0] = B'100: TIOC3D pin function select PE9MD[2:0] = B'100: TIOC3B pin function select PE8MD[2:0] = B'100: TIOC3A pin function select
	Port E control register L4 (PECRL4)	H'FFFE_3A10	H'4444	PE15MD[2:0] = B'100: TIOC4D pin function select PE14MD[2:0] = B'100: TIOC4C pin function select PE13MD[2:0] = B'100: TIOC4B pin function select PE12MD[2:0] = B'100: TIOC4A pin function select
	Port E IO register L (PEIORL)	H'FFFE_3A06	H'FB00	PECRL3 and PECRL4 setting pins set to output



## 2.5 Variables Used in Sample Program

Table 3 lists the variables in the sample program.

**Table 3 Variables Used**

Label	Function	Module Used By
Pul_duty3d	PWM waveform duty of output from TIOC3D pin (set in TGRD_3)	Main routine TGRA_3 compare-match
Pul_duty4c	PWM waveform duty of output from TIOC4C pin (set in TGRC_4)	Interrupt routine
Pul_duty4d	PWM waveform duty of output from TIOC4D pin (set in TGRD_4)	
Ad_start	A/D conversion start timing (set in TADCOBRA_4)	
Dead_time	Dead time (set in TDDR)	Main routine
C_cycle	1/2 of PWM carrier cycle (set in TCBR)	
Pul_cycle	1/2 pulse cycle + dead time (set in TGRC_3)	
Ad_data	Stores A/D conversion result	A/D conversion end interrupt routine

**3. Documents for Reference**

- Software Manual  
SH-2A/SH2A-FPU Software Manual [REJ09B0051]  
(The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual  
SH7216 Group Hardware Manual [REJ09B0543]  
(The latest version can be downloaded from the Renesas Electronics Web site.)

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## Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.23.10	—	First edition issued
1.10	Feb.28.11	—	Added read after FRQCR settings

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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