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SH7211 Group

BSC SRAM Interface Settings Examples

Introduction

This application note introduces the normal space interface functions of the SH7211 bus state controller (BSC) SRAM interface and presents a connection example.

Target Devices

SH7211

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1. Preface

1.1 Specifications

- This application uses a 2 MB (1M words × 16 bits) SRAM, and connects to it with a 16-bit bus width.
- This application uses the SH7211 normal space interface functions and initializes the SRAM.

1.2 Functions Used

• Bus state controller (BSC)

1.3 Application Conditions

- Microcontroller: SH7211
- Operating frequency: Internal clock 160 MHz

Bus clock - 40 MHz Peripheral clock - 40 MHz MTU2S clock - 80 MHz A/D converter clock - 40 MHz

C compiler: Renesas Technology Corp.

SuperH RISC Engine Family C/C++ Compiler Package Version 9.01, Release 01

• Compiler options: The default settings in the HEW file (-cpu=sh2a -debug -gbr=auto -chgincpath -global_volatile=0 -opt_range=all -infinite_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Notes

• The sample program in this document has been verified under the setting conditions in the SH7211 Initial Settings Application Note. Refer to that document in conjunction with this application note.



2. The Application Example

2.1 Operational Overview of the Functions Used

The application uses the SH7211's bus state controller (BSC) to control externally connected SRAM. Table 1 lists the specifications of the SRAM used in this application and figure 1 shows the memory map.

Table 1 SRAM Specifications

Item	SRAM specification
Product No.	R1LV1616RSA-7
Bus width	16 bits
Capacity	2 MB (16 bits × 1 M word) × 1
Package	48 pins TSOP (20 x 12mm)

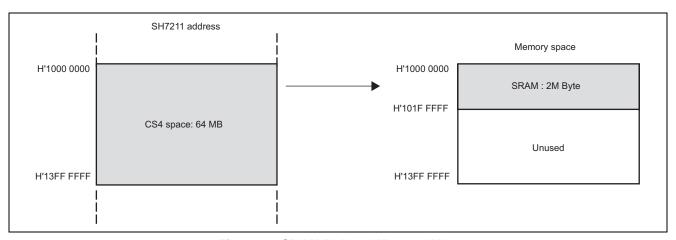


Figure 1 SRAM Related Memory Map



Figure 2 shows a sample SRAM connection circuit and table 2 lists the SH7211 pin functions. Since all pins are set to I/O port operation as the initial pin function, applications must use the pin function controller (PFC) to switch the pin functions as required.

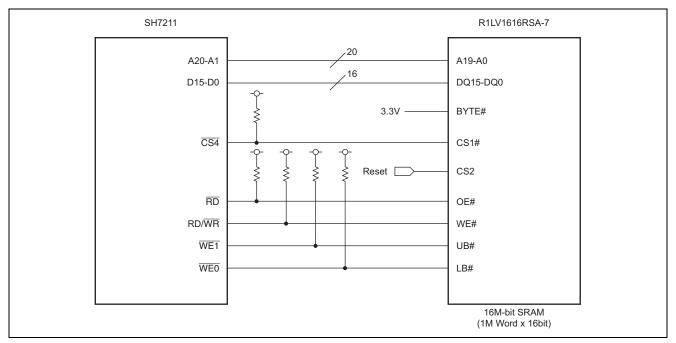


Figure 2 SRAM Connection Circuit Example

Table 2 SH7211 Pin Functions

SH7211 pin	I/O	Initial pin function	Function
A20 to A1	Output	PA14 to PA1	Address bus
D15 to D0	I/O	PD15 to PD0	Data bus
CS4	Output	PB3	Chip select
RD/WR	Output	PB4	Read or write signal
RD	Output	PB17	Read pulse signal (read data output enable signal)
WE1	Output	PB5	Byte write command for D15 to D8
WE0	Output	PB6	Byte write command for D7 to D0



2.2 Setup Procedure for the Functions Used

Table 3 lists sample settings for the bus state controller. See chapter 8, Bus State Controller, in the SH7211 Group Hardware Manual for details on the BSC module. Figure 3 shows a sample setup procedure for the bus state controller.

Table 3 Sample Bus State Controller Settings

Register	Address	Value	Function
CS4 space bus control register (CS4BCR)	H'FFFC 0014	H'1659 3400	 IWW[2:0] = B'001 Write-read/write-write interval idle: 1 idle cycle inserted IWRWD[2:0], IWRRD[2:0] = "B'011" Read-write cycle interval between different spaces, read-read cycle interval between different spaces: 4 idle cycles inserted IWRWS2:0], IWRRS[2:0] = "B'001" Read-write cycle interval between different spaces, read-read cycle interval between the same space: 1 idle cycle inserted TYPE[2:0] = B'011: SRAM with byte selection BSZ[1:0] = B'10: 16-bit bus width
CS4 space wait control register (CS4WCR)	H'FFFC 0038	H'0010 09c1	 BAS = 1 SRAM with byte selection byte access selection: WEn is asserted during read/write access cycles and RDWR is asserted with the write timing. WW[2:0] = B'000 Write access wait cycle count: The same number of cycles as WR[3:0] SW[1:0] = B'01 Address, CS4 assert -> RD, WEn assert delay cycle count: 1.5 cycles WR[3:0] = B'0001 Read access wait cycle count: 3 cycles WM = 1: External wait instruction ignored HW[1:0] = B'01 RD, WEn negate -> address, CS4 negate delay cycle count: 1.5 cycles



SH7211 Group BSC SRAM Interface Settings Examples

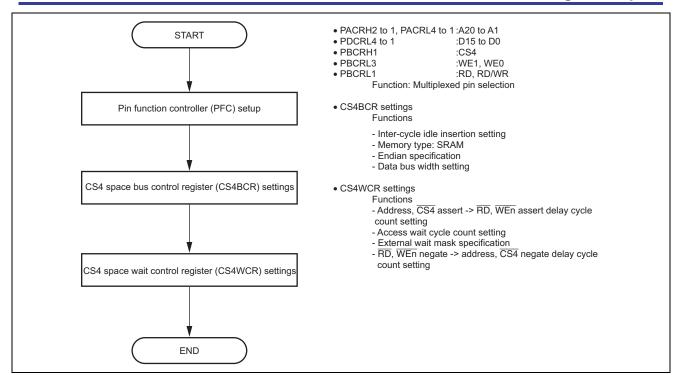


Figure 3 Bus State Controller Setup Procedure (CS4 space)



Figure 4 shows an SRAM read timing example for a 40 MHz bus clock, and figure 5 shows an SRAM write timing example for a 40 MHz bus clock.

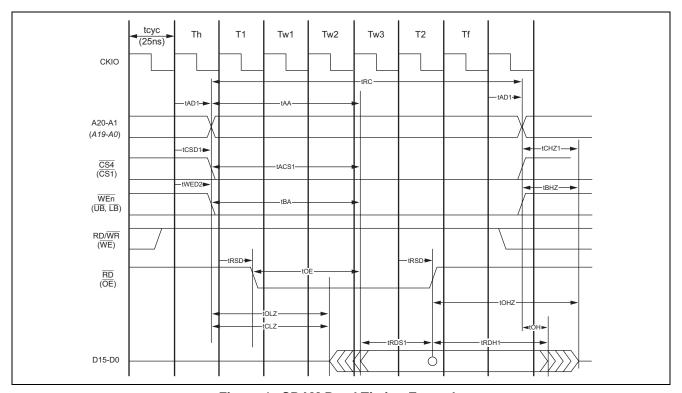


Figure 4 SRAM Read Timing Example

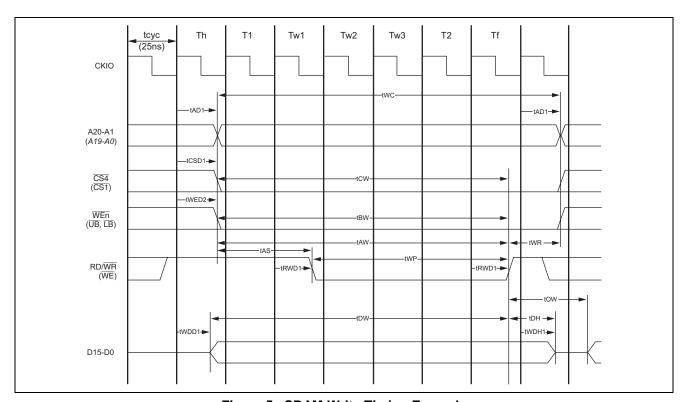


Figure 5 SRAM Write Timing Example



3. Sample Program

```
3
          System Name : SH7211 Sample Program
          File Name : bsc_sram.c
          Version
                  : 1.00.00
          Contents : SH7211 SRAM Initial Setting
7
                  : M3A-HS11
         Model
                   : SH7211
          CPU
9
          Compiler : SHC9.1.1.0
          OS
                  : none
11
12
          note
                  : <Notes>
13
                    This sample program is provided for reference
                    purposes; its operation is not guaranteed.
14
15
                    This sample program may be used for reference
16
                    purposes when developing user applications.
17
                     <Caution>
18
                    This sample programs are all reference,
2.0
                    and no one to guarantee the operation.
21
                    Please use this sample program for the technical
22
                     reference when customers develop softwares.
23
24
          Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
          AND Renesas Solutions Corp. All Rights Reserved
25
26
          history : 2008.04.02 ver.1.00.00
2.7
     #include "iodefine.h"
29
     /* ==== Prototype Declarations ==== */
31
     void io_init_sram(void);
32
33
     34
     * ID
35
     * Module overview: CS4 settings
36
37
     *_____
                 : #include "iodefine.h"
38
     *_____
39
     * Declarations : void io_init_sram(void)
40
     *-----
41
42
     * Function : This function sets up the pin function controller (PFC) and
43
                 : the bus state controller (BSC) and sets up the access timing
                 : for the CS4 space SRAM.
44
45
```

Figure 6 Sample Program Listing: bsc_sram.c (1)



```
46
       * Arguments
47
48
       * Return value : None
49
      * Notes
50
      51
52
      void io_init_sram(void)
53
        /* ==== PFC settings ==== */
54
        PFC.PBCRH1.BIT.PB18MD = 0x1;
                                     /* Set CS4# */
56
        PFC.PBCRL1.BIT.PBOMD = 0x1; /* Set RD */
57
        PFC.PBCRL1.BIT.PB1MD = 0x1;
58
                                     /* Set RDWR */
59
        PFC.PBCRL3.BIT.PB8MD = 0x1;
                                     /* Set WE0 */
60
        PFC.PBCRL3.BIT.PB9MD = 0x1;
                                     /* Set WE1 */
61
62
        PFC.PACRH2.BIT.PA20MD = 0x1;
                                     /* Set A20 */
        PFC.PACRH1.WORD = 0x1111;
                                     /* Set A19-A16 */
63
        PFC.PACRL4.WORD = 0x1111;
                                     /* Set A15-A12 */
64
                                     /* Set A11-A8 */
        PFC.PACRL3.WORD = 0x1111;
65
        PFC.PACRL2.WORD = 0 \times 1111;
                                     /* Set A7-A4 */
67
        PFC.PACRL1.BIT.PA3MD = 0x1;
                                     /* Set A3 */
                                    /* Set A2 */
68
        PFC.PACRL1.BIT.PA2MD = 0x1;
        PFC.PACRL1.BIT.PA1MD = 0x1;
                                     /* Set A1 */
69
70
                                    /* Set D15-D12 */
71
        PFC.PDCRL4.WORD = 0x1111;
72
        PFC.PDCRL3.WORD = 0x1111;
                                    /* Set D11-D8 */
73
        PFC.PDCRL2.WORD = 0x1111;
                                     /* Set D7-D4 */
74
        PFC.PDCRL1.WORD = 0 \times 1111;
                                     /* Set D3-D0 */
75
76
        /* ==== CS4BCR setting ==== */
        BSC.CS4BCR.LONG = 0x16593400ul;
77
78
                    79
                    /* IWW[2:0]="001" ;1Idle cycle */
                    /* IWRWD[2:0]="011"
                                       ;4Idle cycles */
80
                                       ;1Idle cycle */
81
                    /* IWRWS[2:0]="001"
82
                    /* IWRRD[2:0]="011" ;4Idle cycles */
                    /* IWRRS[2:0]="001" ;1Idle cycle */
83
84
                    /* TYPE[2:0]="011" ;SRAM with byte selection */
                    /* BSZ[1:0]="10" ;16bit bus width */
85
86
        /* ==== CS4WCR setting ==== */
87
        BSC.CS4WCR = 0x001009c1ul;
                    /* 0000 0000 0001 0000 0000 1001 1100 0001 */
89
                    /* BAS="1" ;RD/WR signal at the write timing */
90
                    /* WW[2:0]="000" ;same WR[3:0} setting
91
92
                    /* SW[1:0]="01"
                                     ;1.5 cycles
93
                    /* WR[3:0]="0011" ;5 wait cycles
94
                    /* WM="1"
                                ;External wait input is ignored
                    /* HW[1:0]="01" ;1.5 cycles
95
96
      }
       /* End of File */
```

Figure 7 Sample Program Listing: bsc sram.c (2)



4. Reference Documents

 Software Manual SH-2A, SH2A-FPU Software Manual, Rev. 3.00 (The latest version can be downloaded from the Renesas Technology Web site.)

 Hardware Manual SH7211 Group Hardware Manual, Rev. 2.00 (The latest version can be downloaded from the Renesas Technology Web site.)

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