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SH7145 Group

DMA in Single Address Mode

Introduction

This application note describes data transfer by the DMAC (Direct Memory Access Controller) module in single address mode. The DMAC performs high-speed data transfer in one bus cycle from external SRAM to an external device with DACK (transfer request acknowledge signal).

Target Device

SH7145F

Contents

1. Specifications

The DMAC (Direct Memory Access Controller) of the SH7145 is used to perform DMA data transfer in single address mode. Data is transferred from external SRAM to a device with DACK (transfer request acknowledge signal). The transfer request mode of the DMAC is set to external request, and five 32-bit data items (or a total of 20 bytes) are transferred.

Figure 1 illustrates data transfer by the DMAC; table 1 shows the DMAC settings.

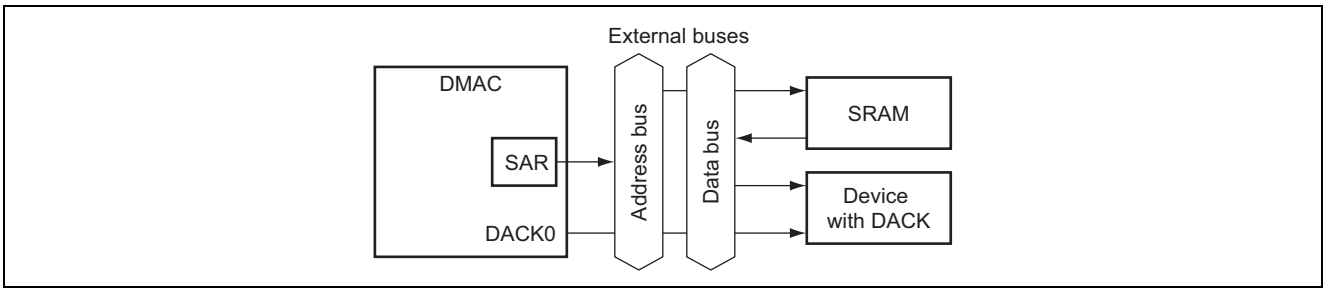


Figure 1 Data Transfer Using DMAC

Table 1 DMAC Settings

Setting Item	Description
Address mode	Single address mode
Transfer request	External request (input to the $\overline{\text{DREQ}}$ pin)
Detection of transfer request	Detection on the falling edge of the $\overline{\text{DREQ}}$ pin
Number of transfers	Five times (A total of 20 bytes of data is transferred.)
Bus mode	Burst mode
Transfer source address	SRAM [H'00400000] allocated to CS1 space (Auto-incremented according to the data size after transfer.)
Transfer data size	Longword (32 bits)
DACK signal	Output as an active-low signal.
Interrupt	Transfer end interrupt is enabled.

2. Description of Functions

In this sample task, the DMAC is used for DMA transfer of data from external SRAM connected to the SH7145 to a device with DACK.

2.1 DMAC (Direct Memory Access Controller)

Data transfer is performed in single address mode. Figure 2 is a block diagram of DMAC module channel 0 (ch0); below, functions are explained referring to figure 2.

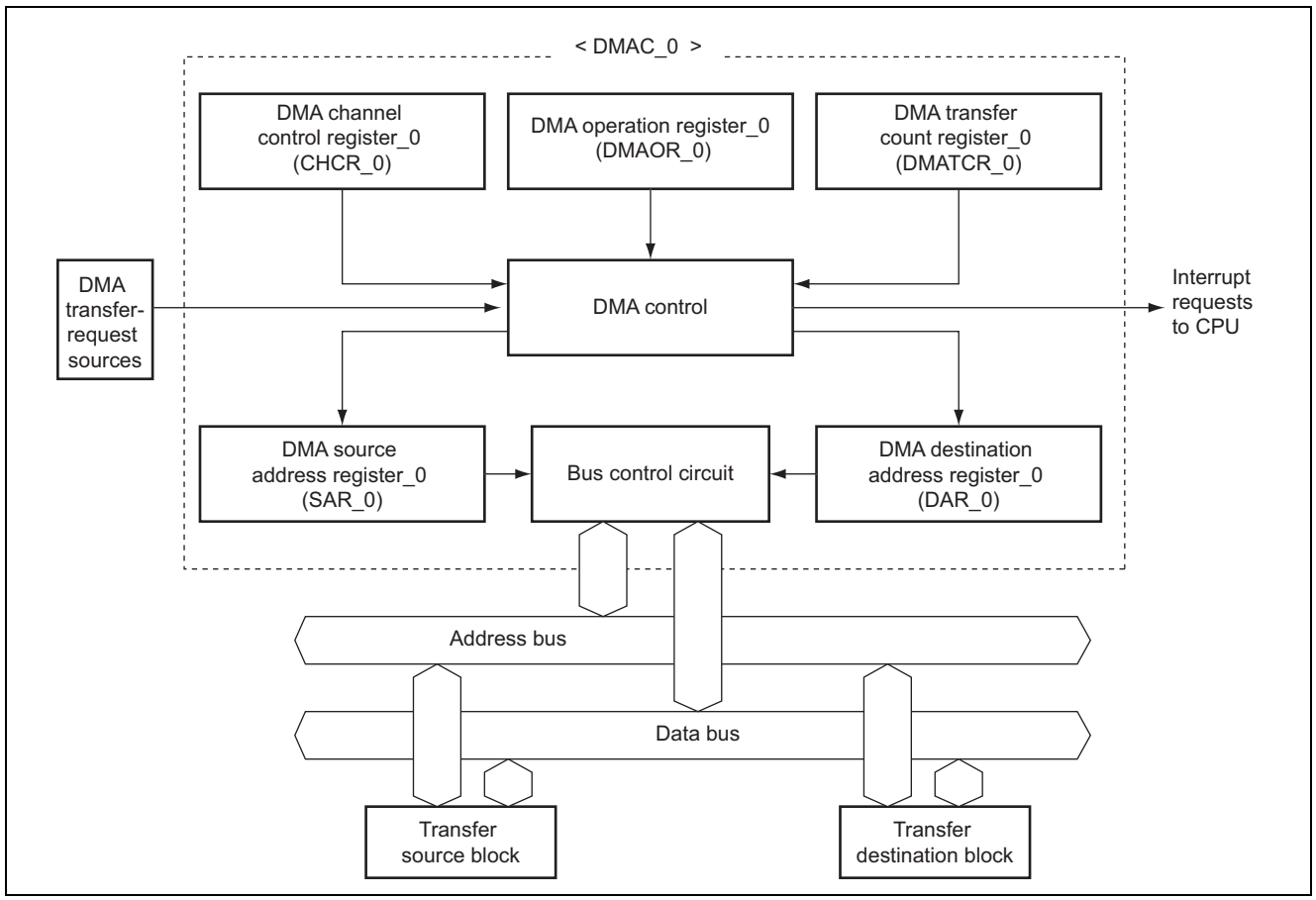


Figure 2 DMAC Block Diagram (ch0)

- The DMAC can perform high-speed data transfer, in place of the CPU, between external devices with DACK (transfer request acknowledge signal), external memory devices, memory-mapped external devices, and on-chip peripheral modules.
- The DMAC can be activated by either an external request or a request from an on-chip module. The on-chip modules that can generate DMAC activating requests are MTU, A/D1, SCI0, and SCI1. When auto-request is set by the CHCR_0 register, DMA transfer can be performed by the DMAC alone by setting the DE bit in CHCR_0 to 1.
- The DMA source address register_0 (SAR_0) is a 32-bit register which specifies the transfer source address. SAR_0 has a counting function that can be selected by the DMA channel control register_0 (CHCR_0) from among three modes: fixed, auto-increment, and auto-decrement modes. During DMA operation, SAR_0 always indicates the next transfer source address.
- The DMA destination address register_0 (DAR_0) is a 32-bit register which specifies the transfer destination address. DAR_0 has a counting function that can be selected by the DMA channel control register_0 (CHCR_0) from among three modes: fixed, auto-increment, and auto-decrement modes. During DMA operation, DAR_0 always indicates the next transfer destination address.
- The DMA transfer count register_0 (DMATCR_0) is a 32-bit register which specifies the number of transfers. The lower 24 bits are used to specify the number of transfers while the upper eight bits of this register are always 0. When writing, the upper eight bits should always be set to 0. If the DMATCR_0 is set to H'000000, this is recognized as the maximum value, and 16,777,216 transfers are performed. During DMAC operation, this register is auto-decremented and indicates the number of remaining transfers .
- The DMA channel control register_0 (CHCR_0) is a 32-bit register which specifies the operation mode, transfer method, and other parameters for channel 0.
- The DMA operation register (DMAOR) is a 16-bit register which specifies the transfer mode for the entire DMAC.

3. Description of Operation

Figure 3 shows the operation timing.

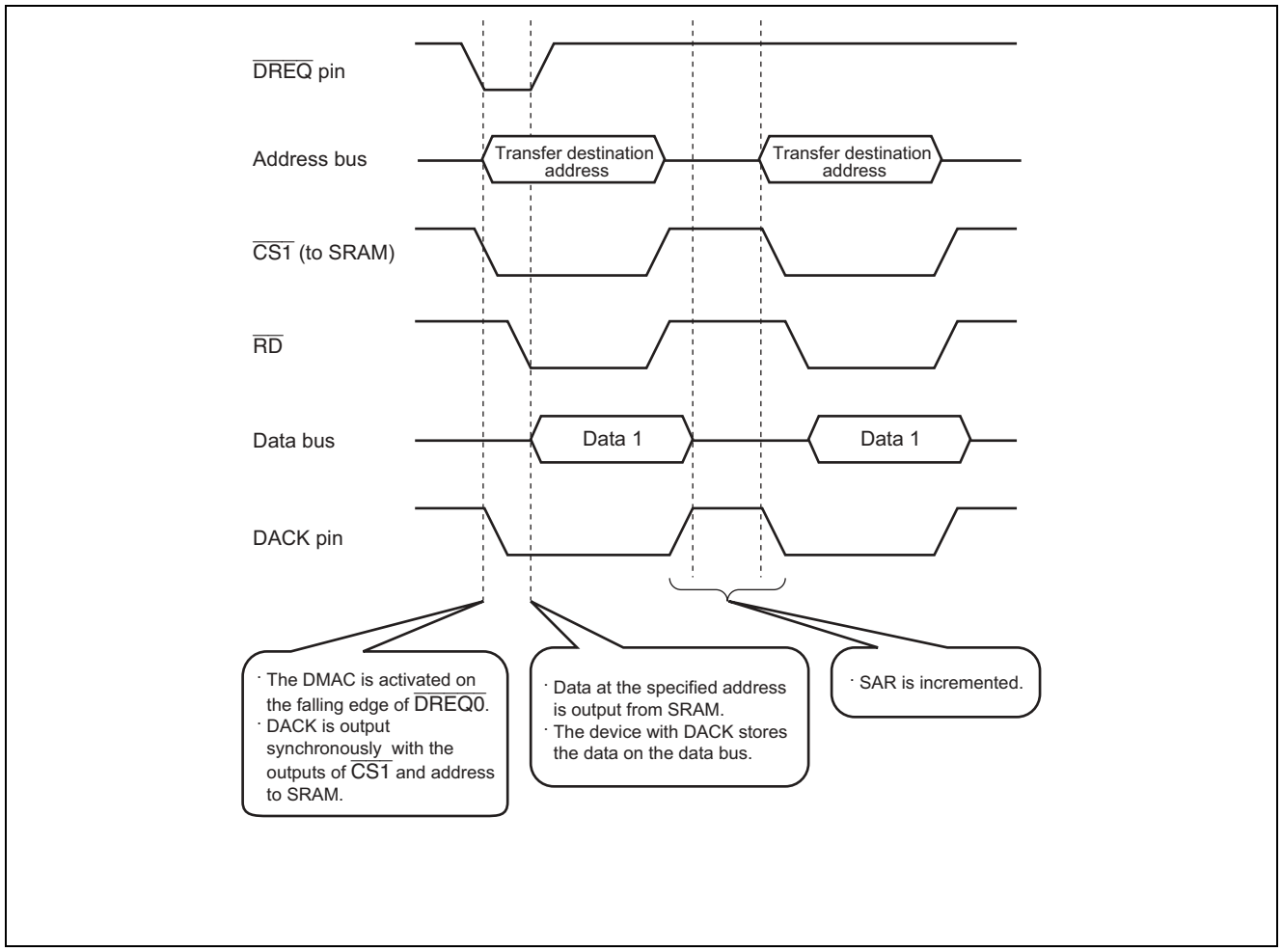


Figure 3 Operation in Single Address Mode

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main	Sets up the DMAC and pin functions, and starts transfer by the DMAC.
Transfer end interrupt routine	cmt_int	Stops DMAC operation

4.2 Internal Registers

Tables 3 to 5 describe the internal registers used in this sample task. The settings are the values used in this sample task and are different from their initial values.

Table 3 Description of Internal Registers (1)

Register Name	Bit	Bit Name	Setting	Function
MSTCR1				Module standby control register 1
	9	MSTP25	0	DMAC Standby Control
	8	MSTP24	0	When MSTP25 = 0 and MSTP24 = 0, the standby state of the DMAC is cancelled.
DMAOR			H'0001	DMAC operation register
	15 to 10	—	0	Reserved
	9	PR1	0	Priority Mode 1, 0
	8	PR0	0	These bits specify the priority order of channels for execution.
	7 to 3	—	0	Reserved
	2	AE	0	Address Error Flag
	1	NMIF	0	NMI Flag
	0	DME	1	DMAC Master Enable When DME = 1, enables operation on all channels of the DMAC.

Table 4 Description of Internal Registers (2)

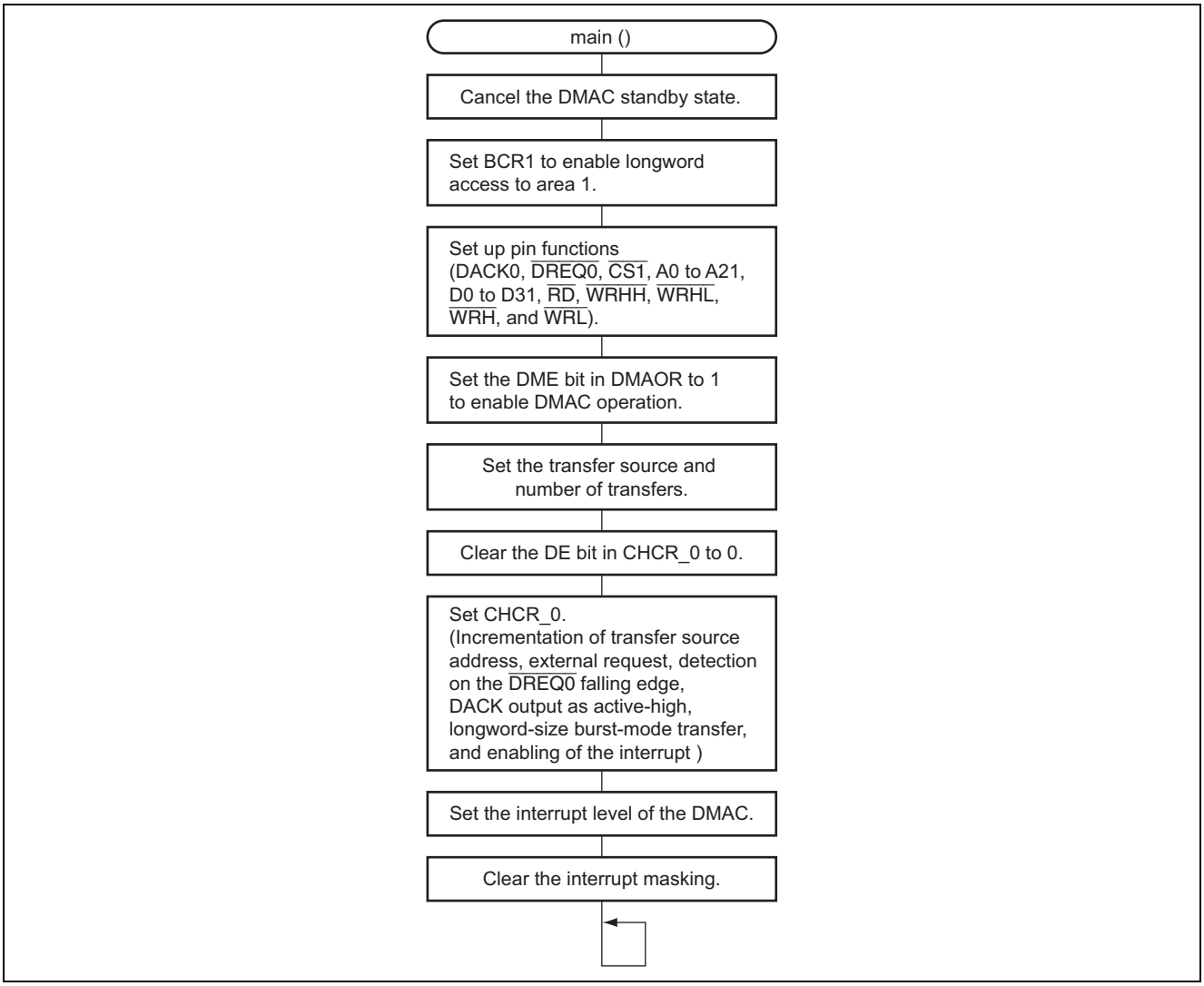
Register Name	Bit	Bit Name	Setting	Function
CHCR_0			H'00001275	DMA channel control register_0
	31 to 21	—	0	Reserved
	20	DI	0	Direct/Indirect Select Only valid for channel 3. Invalid in this sample task because only channel 0 is used.
	19	RO	0	Source Address Reload Only valid for channel 2. Invalid in this sample task because only channel 0 is used.
	18	RL	0	Request Check Level When RL = 0, DRAK output is active-high.
	17	AM	0	Acknowledge Mode Invalid in single address mode.
	16	AL	0	Acknowledge Level When AL = 0, DACK output is active-high.
	15	DM1	0	Destination Address Mode 1, 0
	14	DM0	0	Invalid when the transfer destination is a device with DACK in single address mode.
	13	SM1	0	Source Address Mode 1, 0
	12	SM0	1	When SM1 = 1 and SM0 = 1, the transfer source address is incremented.
	11	RS3	0	Resource Select 3, 2, 1, 0
	10	RS2	0	These bits specify the transfer request source.
	9	RS1	1	When RS [3, 2, 1, 0] = 0010, “external request while the transfer destination is a device with DACK” is selected.
	8	RS0	0	
	7	—	1	Reserved
	6	DS	1	$\overline{\text{DREQ}}$ Select When DS = 1, external requests are detected on the falling edge of the $\overline{\text{DREQ}}$ pin.
	5	TM	1	Transmit Mode When TM = 1, transfers are performed in burst mode.
	4	TS1	1	Transmit Size 1, 0
	3	TS0	0	When TS [1,0] = 10, transfers are performed in longword size.
	2	IE	1	Interrupt Enable When IE = 1, an interrupt request is issued after the specified number of transfers have ended.
	1	TE	0	Transfer End This bit is set to 1 when the specified number of transfers have ended.
	0	DE	1	DMAC Enable When DE = 1, the operation on the corresponding channel is enabled.
BCR1			H'602F	Bus control register
	5	A1LG	1	Longword Access Setting for CS1 Space When A1LG = 1, CS1 space is accessed in longword.

Table 5 Description of Internal Registers (3)

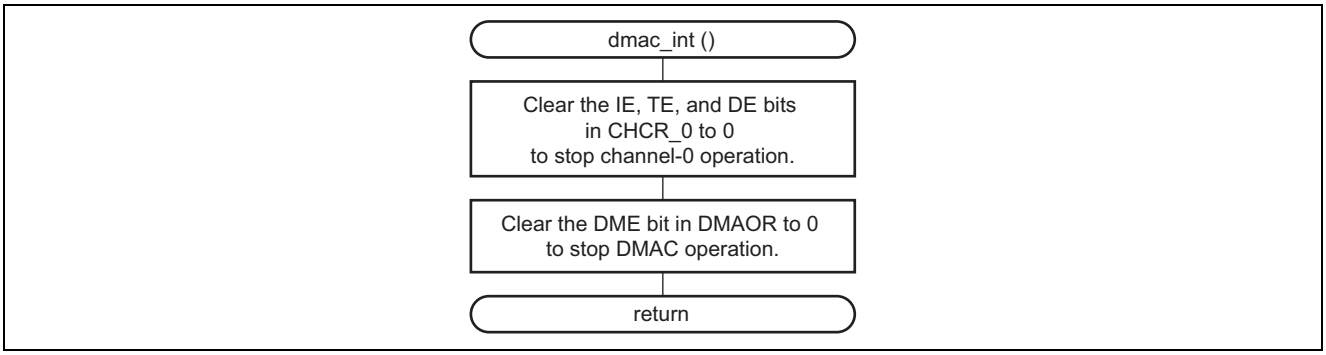
Register Name	Bit	Bit Name	Setting	Function
PACRL2				Port-A control register L2
	5	PA2MD1	1	These bits set the port A pin to function as $\overline{\text{DREQ0}}$.
	4	PA2MD0	0	
PECRL1				Port-E control register L1
	13	PA14MD1	1	These bits set the port E pin to function as DACK0.
	12	PA14MD0	0	
PACRH			H'5000	Port-A control register H Sets port A pins to function as $\overline{\text{WRHH}}$ and $\overline{\text{WRHL}}$.
PACRL1			H'1540	Port-A control register L1 Sets port A pins to function as $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, and $\overline{\text{CS1}}$.
PBCR1			H'000A	Port-B control register 1 Sets port B pins to function as A21 and A20.
PBCR2			H'A005	Port-B control register 2 Sets port B pins to function as A19 to A16.
PCCR			H'FFFF	Port-C control register Sets port C pins to function as A15 to A0.
PDCRH1			H'5555	Port-D control register H1 Sets port D pins to function as D31 to D24.
PDCRH2			H'5555	Port-D control register H2 Sets port D pins to function as D23 to D16.
PDCRL1			H'FFFF	Port-D control register L1 Sets port D pins to function as D15 to D0, in combination with PDCRL2.
PDCRL2			H'0000	Port-D control register L2 Sets port D pins to function as D15 to D0, in combination with PDCRL1.

5. Flowchart

5.1 Main Routine



5.2 Transfer End Interrupt Routine



6. Program Listing

```
/***********************************************************************************************/
/* SH7145F Application Note                                                                    */
/*                                                                                             */
/* Function                                                                                    */
/*    :DMAC0(Single Address Mode)                                                              */
/*                                                                                             */
/* External input clock         :12.5MHz                                                       */
/* Internal CPU clock           :50MHz                                                         */
/* Internal peripheral clock    :25MHz                                                         */
/*                                                                                             */
/* Written        2003/12        Rev.1.0                                                       */
/***********************************************************************************************/

#include "iodefine.h"
#include <machine.h>

/***********************************************************************************************/
/*  Symbol Definition                                                                          */
/***********************************************************************************************/
#define NUM          5
#define SRAM_ADDR    0x00400000

/***********************************************************************************************/
/*  Function Define                                                                            */
/***********************************************************************************************/
void main(void);

void dmac_int(void);
void dummy_f(void);

/***********************************************************************************************/
/* Main Program                                                                                */
/***********************************************************************************************/
void main( void )
{
    P_STBY.MSTCR1.BIT.MSTP25 = 0;
    P_STBY.MSTCR1.BIT.MSTP24 = 0;                  /* Disable DMAC standby mode                */

    // Set BSC
    P_BSC.BCR1.BIT.A1LG = 0x1;                     /* Area 1 is long-word access               */

    // Sset pin function
    P_PORTA.PACRL2.BIT.PA2MD = 0x2;                /* Set PA2 -> DREK0                         */
    P_PORTE.PECRL1.BIT.PE14MD = 0x2;               /* Set PE14 -> DACK0                        */

    P_PORTD.PDCRH1.WORD = 0x5555;
    P_PORTD.PDCRH2.WORD = 0x5555;
    P_PORTD.PDCRL1.WORD = 0xFFFF;
    P_PORTD.PDCRL2.WORD = 0x0000;                  /* Set PD31-0 -> D31-0                      */
```

```
    P_PORTB.PBCR1.WORD  |= 0x000A;                 /* Set A21,A20                          */
    P_PORTB.PBCR2.WORD  |= 0xA005;                 /* Set A19-A16                          */
    P_PORTC.PCCR.WORD   = 0xFFFF;                  /* Set A15-A0                           */
    P_PORTA.PACRH.WORD  |= 0x5000;                 /* Set WRHH,WRHL                        */
    P_PORTA.PACRL1.WORD |= 0x1540;                 /* Set RD,WRH,WRL,CS1                   */

    // Set DMAC
    P_DMAC.DMAOR.BIT.DME = 1;                      /* DMAC enable                          */

    P_DMAC0.SAR0 = SRAM_ADDR;                      /* Set of source address                */
    P_DMAC0.DMATCR0 = NUM;                         /* Set of times of transmission         */

    P_DMAC0.CHCR0.BIT.DE = 0;                      /* Clear DE bit                         */

    P_DMAC0.CHCR0.LONG = 0x00001274;
            // [1-21]  = 0    : Reserve
            // [20]    = 0    : Direct address mode
            // [19]    = 0    : Source address is not reload
            // [18]    = 0    : DRAK is high-active
            // [17]    = 0    : DACK outputs is read cycle
            // [16]    = 0    : DACK is high-active
            // [15-14] = 0    : Transmission address is fix
            // [13-12] = 2    : Source address is increment
            // [11-8]  = 2    : Auto-request
            // [7]     = 0    : Reserve
            // [6]     = 1    : DREQ is detected with falling edge
            // [5]     = 1    : Burst mode
            // [4-3]   = 2    : Long word size
            // [2]     = 1    : DEI0 interrupt enable
            // [1]     = 0    : Transfer end
            // [0]     = 0    : DMAC0 disable

    P_INTC.IPRC.BIT.DMAC0 = 10;                    /* Set DEI0 interrupt level             */
    set_imask(0);                                  /* Clear interrupt mask level           */

    P_DMAC0.CHCR0.BIT.DE = 1;                      /* DMAC0 transmission start             */

    while(1);                                      /* LOOP                                 */
}
```

```
/************************************************************************************************/
/*  Interruption Program                                                                        */
/************************************************************************************************/
/************************************************************************************************/
/*  DEI0 Interruption Program                                                                   */
/************************************************************************************************/
#pragma interrupt(dmac_int)
void dmac_int(void)
{
    // Transmission end process
    P_DMAC0.CHCR0.LONG &= 0xFFFFFFF8;              /* Clear IE,TE,DE bit                       */

    P_DMAC.DMAOR.WORD &= 0xFFFE;                   /* DMAC disable                             */
}

/************************************************************************************************/
/*  Other Interruption Program                                                                  */
/************************************************************************************************/
#pragma interrupt(dummy_f)
void dummy_f(void)
{
    /* Other Interrupt */
}
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.16.04	—	First edition issued

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