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Renesas Electronics Corporation

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SH7144/45 Group

Complementary PWM 3-Phase Output

1. Specifications

Three-phase PWM waveform output is performed with a non-overlapping relationship between positive and negative phases, as shown in figure 1.

The duty cycle can be changed between 0% and 100% by setting an arbitrary value in RAM.

$$\text{Duty cycle} = \frac{\text{Pulse high width}}{\text{Pulse period}} \times 100 (\%)$$

Toggle waveform output is performed synchronized with the period.

When operating with on-chip peripheral clock $P\phi = 40.0 \text{ MHz}$, the output pulse period can be set arbitrarily in the range 50.0 ns to 1.63 ms.

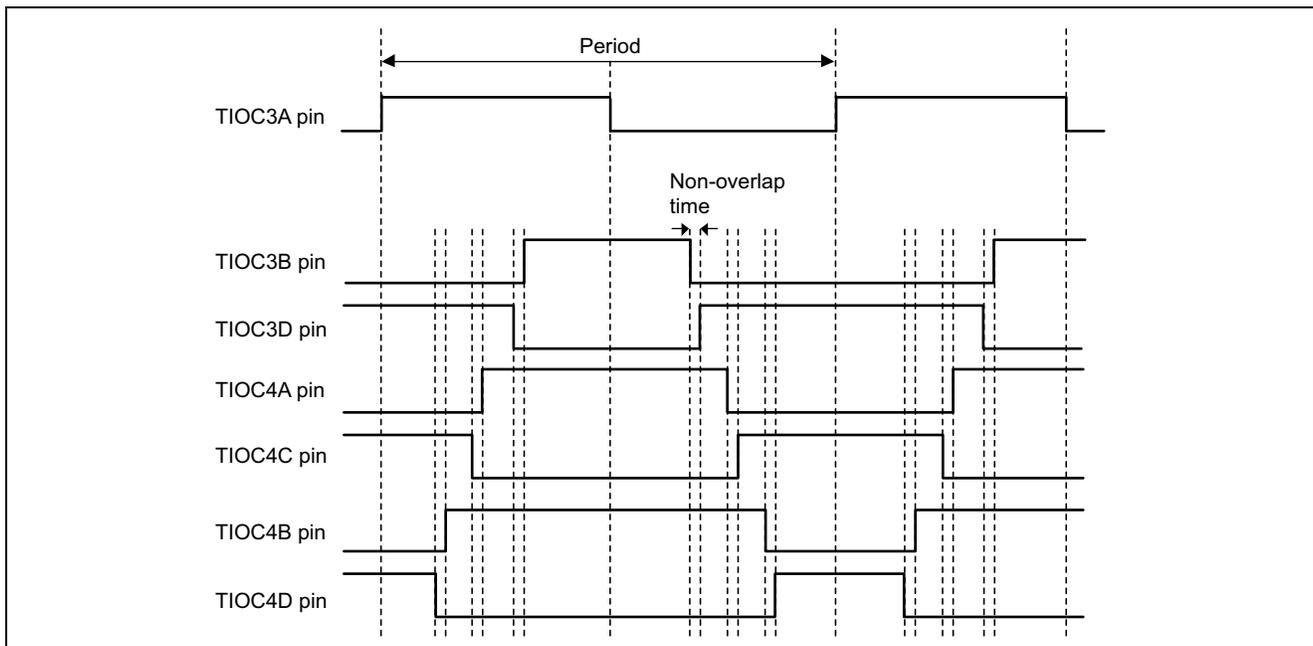


Figure 1 Complementary PWM 3-Phase Output Waveforms

2. Functions Used

In this sample task, 3-phase PWM waveform output with a non-overlapping relationship between positive and negative phases is performed using MTU channels 3 and 4.

Figure 2 shows a block diagram of the MTU/ch3, ch4 as used in this sample task. This sample task uses the following functions.

- A function that performs 3-phase PWM waveform output with a non-overlapping relationship between positive and negative phases (complementary PWM mode)
- A function that transfers buffer register (TGRC/D_3, TGRC/D_4) contents to compare registers (TGRA/B_3, TGRA/B_4) when a compare match occurs
- A function that outputs a toggle waveform synchronized with the PWM waveform period

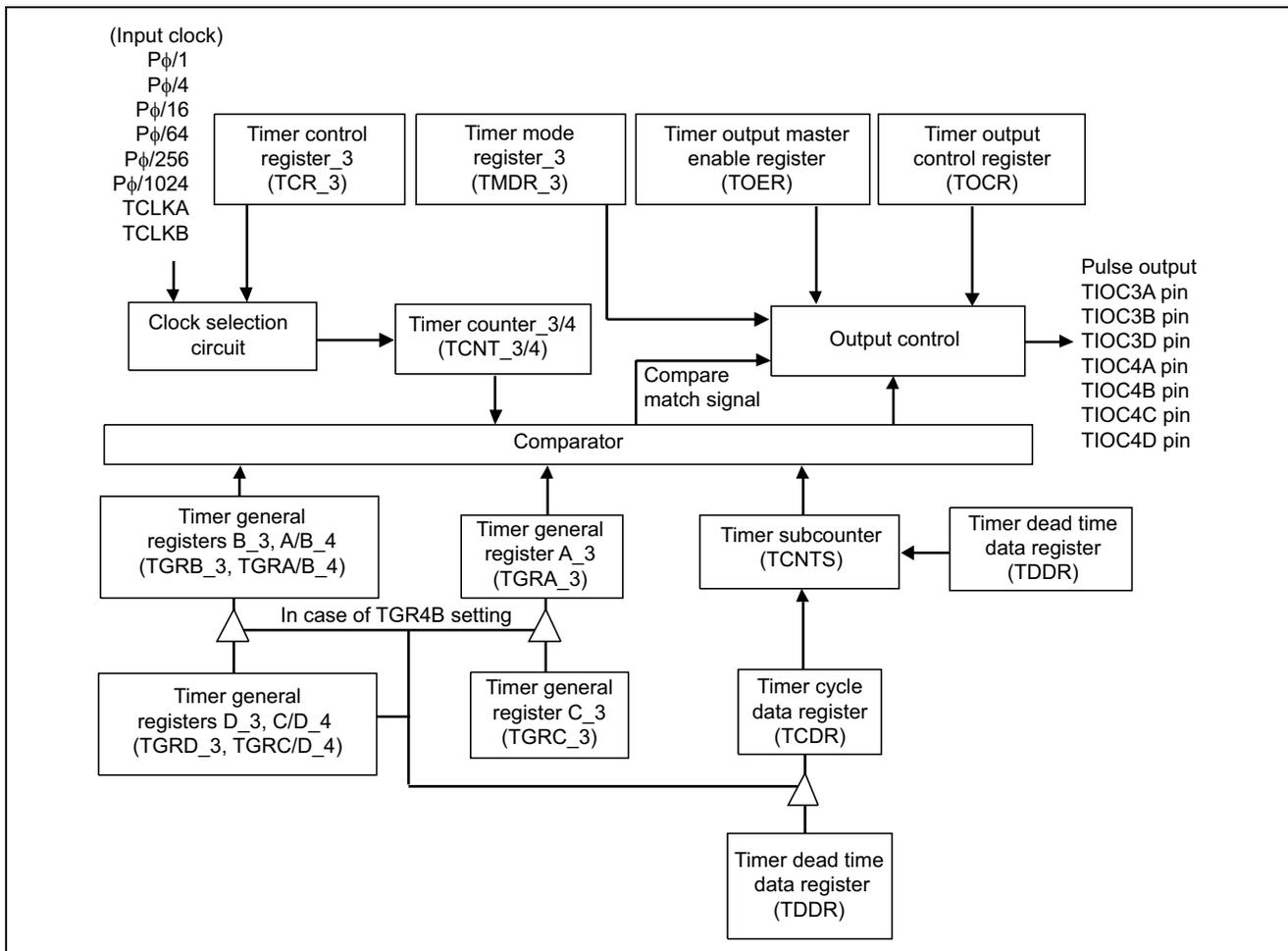


Figure 2 Block Diagram of MTU/ch3, ch4

Table 1 shows the function assignments used in this task. PWM pulses are output by assigning MTU functions as shown in the table.

Table 1 Function Assignments

Pin or Register Name	Function Assignment
TIOC3A	Toggle output synchronized with PWM period
TIOC3C	PWM output 1
TIOC3D	Negative-phase waveform in non-overlapping relationship with PWM output 1
TIOC4A	PWM output 2
TIOC4B	PWM output 3
TIOC4C	Negative-phase waveform in non-overlapping relationship with PWM output 2
TIOC4D	Negative-phase waveform in non-overlapping relationship with PWM output 3
TOCR	Enabling/disabling of toggle output synchronized with PWM period
TOER	MTU output pin output enabling/disabling
TCR_3	Selection of ch3 timer counter clearing source and input clock
TMDR_3	Ch3, ch4 set to complementary PWM mode
TGRA_3	TCNT_3 upper-limit value setting (1/2 carrier period + dead time)
TGRC_3	TGRA_3 buffer register
TGRB_3	Output pulse transition point setting (compare register)
TGRA_4	
TGRB_4	
TGRC_4	TGRA_4 buffer register
TGRD_4	TGRB_4 buffer register
TDDR	Dead time setting
TCDR	TCNT_4 upper-limit value setting (1/2 carrier period)
TCBR	TCDR buffer register

3. Principles of Operation

Figure 3 illustrates the principles of operation. Complementary PWM waveform output is performed by SH7145 hardware and software processing.

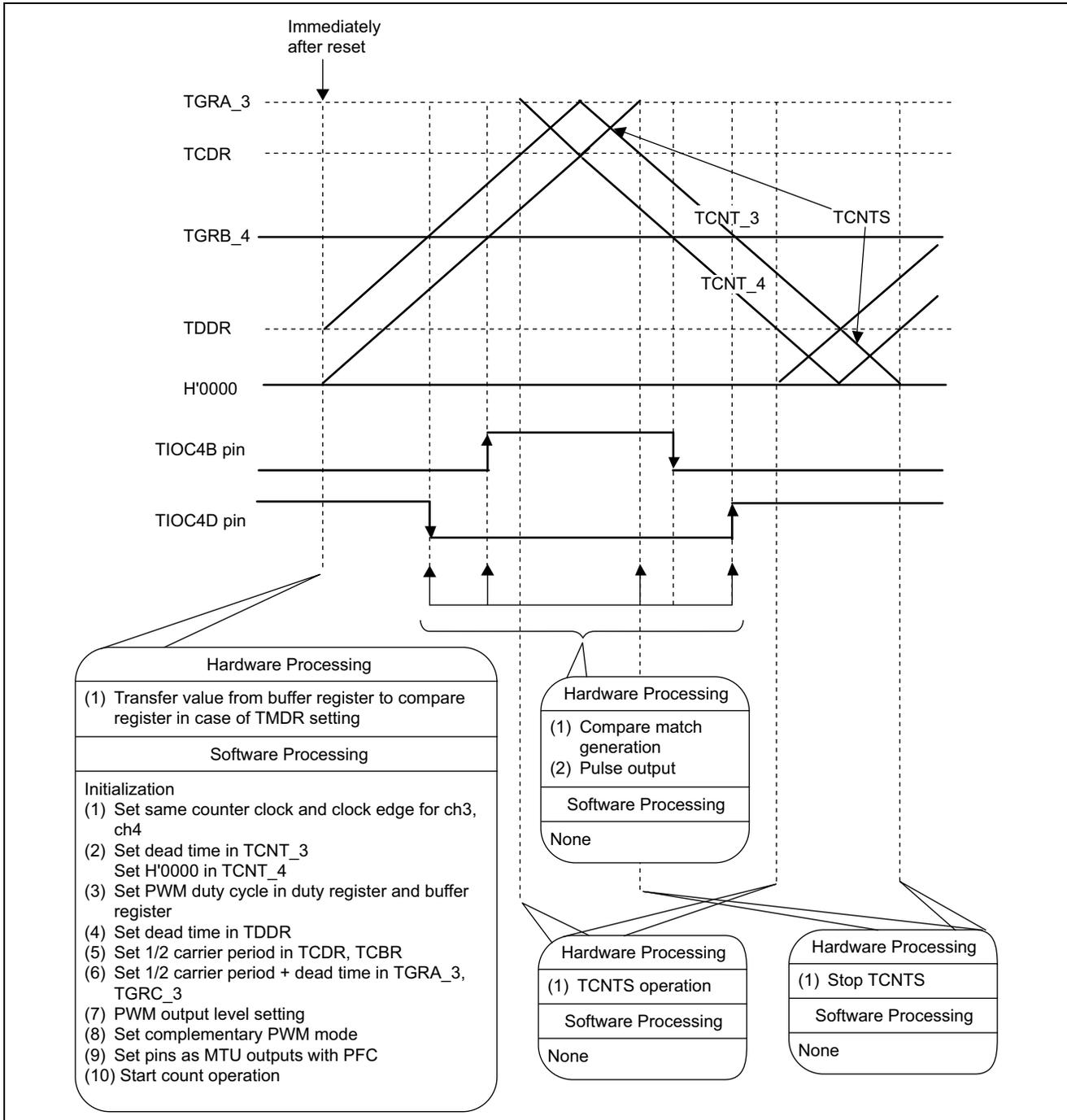


Figure 3 Principles of Operation of Complementary PWM Single-Phase Waveform Output

Figure 4 shows the PWM waveform output method. When complementary PWM mode is set, the following rules apply to data transfer and compare operations.

- Data Transfer
 - In period T_a , data written to a buffer register is always transferred to a temporary register.
 - In period T_{b1} , when the transfer mode is set to transfer at the peak, data is not transferred from a buffer register to a temporary register. In period T_{b2} , the operation is the same as in period T_a . Similarly, when a trough setting is made, data is not transferred in period T_{b2} .
 - Data transfer to a buffer register can be performed arbitrarily.
- Compare Match
 - In period T_b , two registers—the temporary register and compare register—and three counters—TCNT_3/4 and TCNTS—are compared, and the PWM waveform is controlled.
 - In area (a), pre-change data and compare matches (3) and (4) have priority.
 - In area (b), post-change data and compare matches (1) and (2) have priority.

Generation of a compare match whereby the output waveform goes to the active level (compare match (1) or (3)) occurs only after generation of a compare match whereby the respective output waveform goes to the positive level (compare match (4) or (2)).

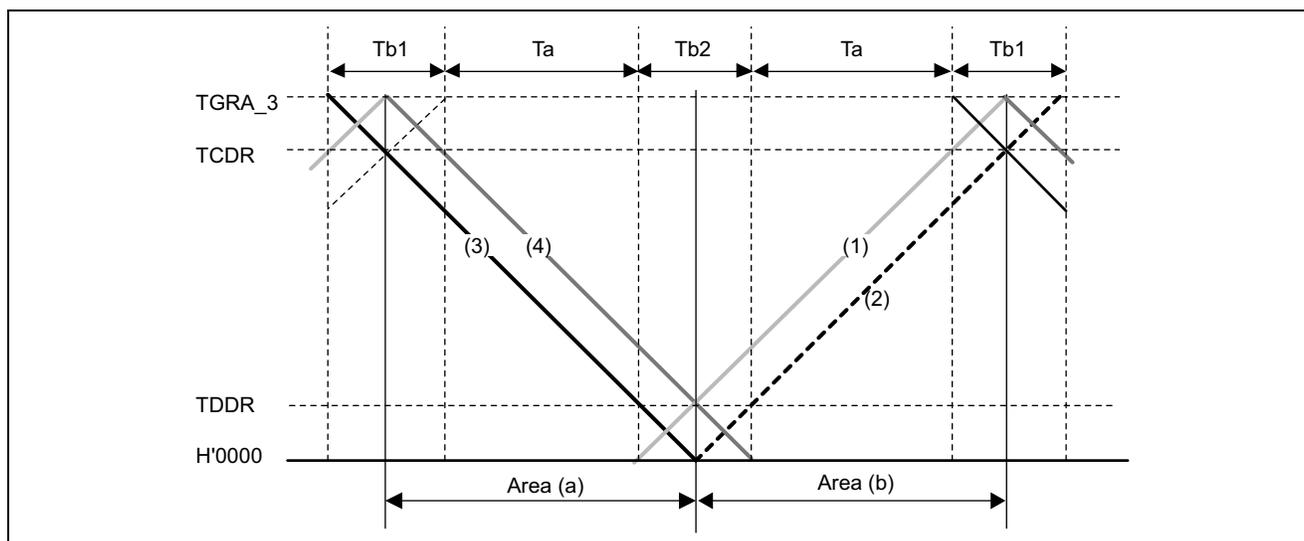


Figure 4 Principles of Operation of PWM Waveform Output Method

Figure 5 illustrates the principles of operation. Complementary PWM waveform output is performed by SH7145 hardware and software processing.

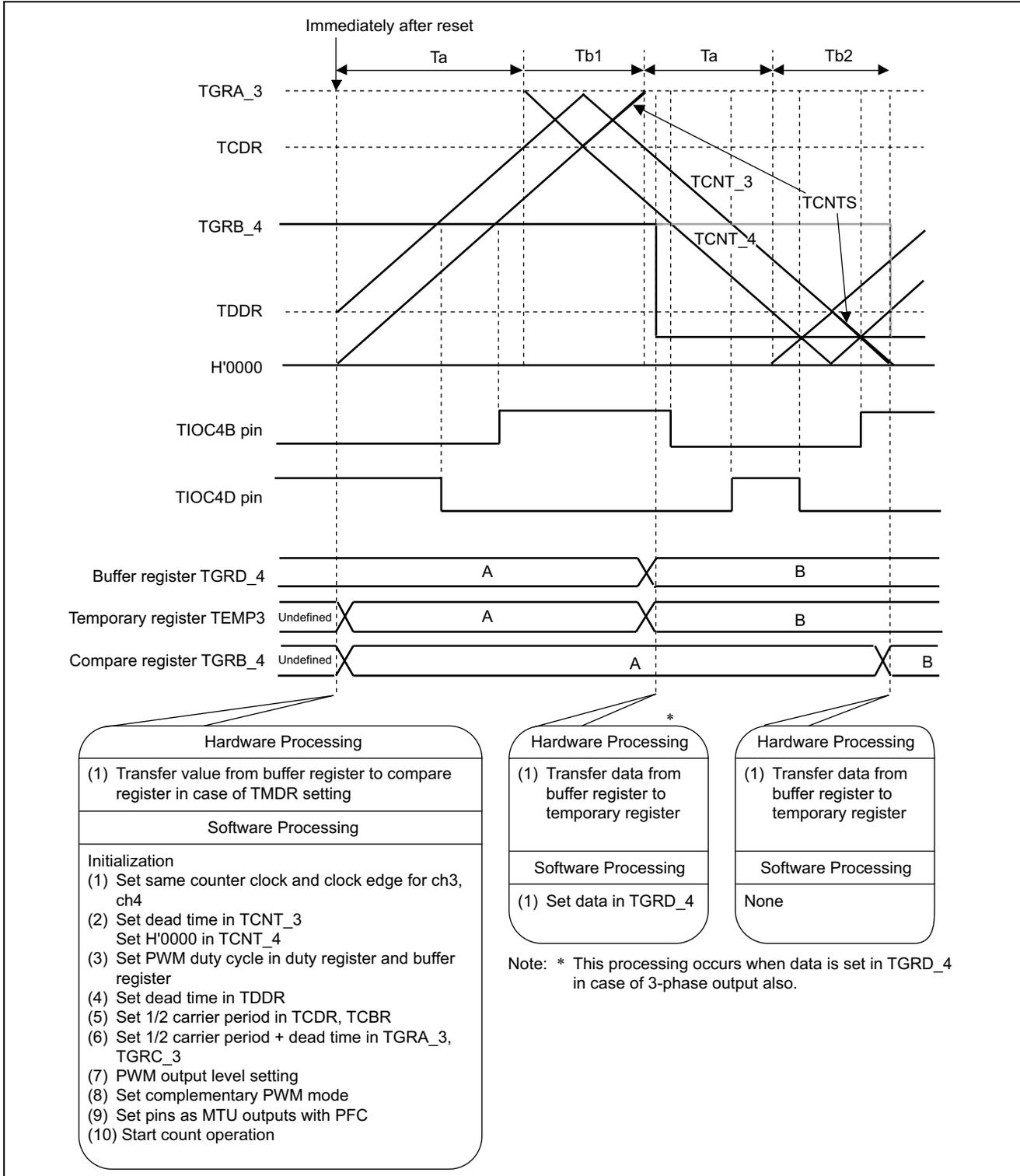


Figure 5 Principles of Operation of Complementary PWM Single-Phase Waveform Output

Figure 6 illustrates the principles of operation. Three-phase PWM output is performed from the ch3 and ch4 PWM output pins (TIOC3B/D, TIOC4A/B/C/D) by SH7145 hardware and software processing as shown in the figure.

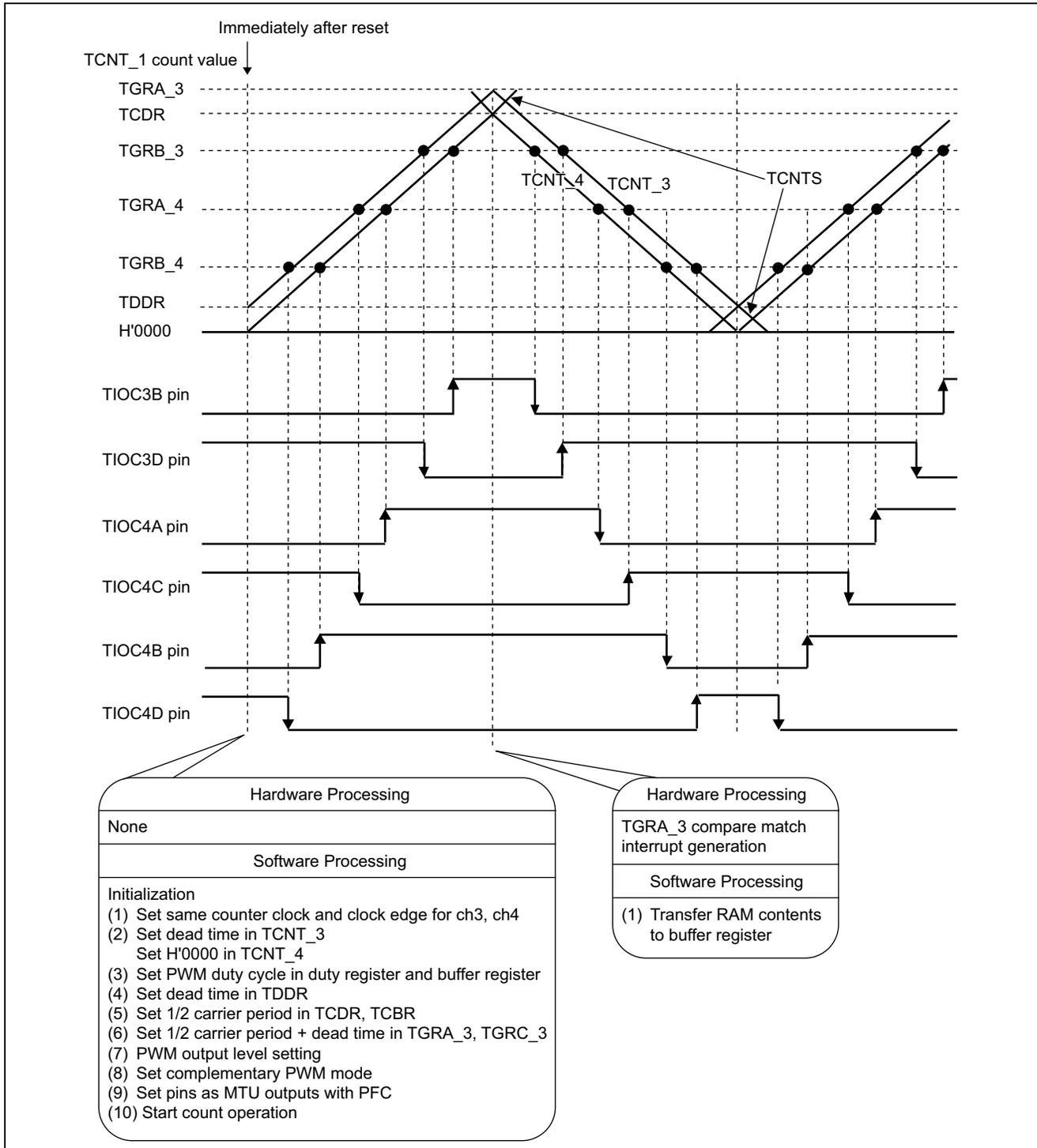


Figure 6 Principles of Operation of PWM Waveforms

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	comple	Complementary PWM output setting
Data setting	setdata	Sets waveform transition timing in buffer register

(2) Arguments

Label or Register Name	Function	Data Length	Module	Input/Output
pul_cyc1	Used to set pulse 1/2 period + dead time value Pulse period is calculated using following equation: Pulse period (ns) = timer value × φ period (25.0 ns at 40.0 MHz operation)	1 word	Main routine	Input
pul_duty3d	Used to set TIOC pin output waveform transition timing			
pul_duty4c				
pul_duty4d				
c_cyc	PWM carrier period register value setting			
dead_time	Non-overlap time setting		Main routine Data setting	

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_STBY.MSTCR2	MTU module standby mode clearing	H'FFFF861E	H'd0fd
P_PORTE.PEIORL	Sets TIOC3B/D, TIOC4A/B/C/D pins as outputs	H'FFFF83B4	H'fb00
P_PORTE.PECRL1	Sets pin functions as TIOC3B/D, TIOC4A/B/C/D	H'FFFF83B8	H'5545
P_MTU34.TCR_3	MTU/ch3 counter clock and clock edge setting	H'FFFF8200	H'01
P_MTU34.TCR_4	MTU/ch4 counter clock and clock edge setting	H'FFFF8201	H'01
P_MTU34.TIER_3	Enables TGIA_3 interrupt	H'FFFF8208	H'41
P_MTU34.TGRA_3	1/2 carrier period + dead time setting	H'FFFF8218	pul_cyc1
P_MTU34.TGRC_3	P_MTU34.TGRA_3 buffer register (same value set as P_MTU34.TGRA_3)	H'FFFF8224	pul_cyc1
P_MTU34.TCNT_3	Dead time setting	H'FFFF8210	dead_time
P_MTU34.TCNT_4	H'0000 set	H'FFFF8212	H'0000
P_MTU34.TGRB_3	Setting of PWM duty cycle output from TIOC3B, TIOC3D	H'FFFF821A	pul_duty3d
P_MTU34.TGRA_4	Setting of PWM duty cycle output from TIOC4A, TIOC4C	H'FFFF821C	pul_duty4c
P_MTU34.TGRB_4	Setting of PWM duty cycle output from TIOC4B, TIOC4D	H'FFFF821E	pul_duty4d
P_MTU34.TGRD_3	P_MTU34.TGRB_3 buffer register (same value set as P_MTU34.TGRB_3)	H'FFFF8226	pul_duty3d

Register Name	Function	Address	Set Value
P_MTU34.TGRC_4	P_MTU34.TGRA_4 buffer register (same value set as P_MTU34.TGRA_4)	H'FFFF8228	pul_duty4c
P_MTU34.TGRD_4	P_MTU34.TGRB_4 buffer register (same value set as P_MTU34.TGRB_4)	H'FFFF822A	pul_duty4d
P_MTU34.TDDR	Dead time setting	H'FFFF8216	dead_time
P_MTU34.TCDR	1/2 carrier period setting	H'FFFF8214	c_cyc
P_MTU34.TCBR	P_MTU34.TCDR buffer register (same value set as P_MTU34.TCDR)	H'FFFF8222	c_cyc
P_MTU34.TOCR	Enabling of toggle output synchronized PWM period, and positive-phase/negative phase output level setting	H'FFFF820B	H'43
P_MTU34.TMDR_3	Sets complementary PWM mode	H'FFFF8202	H'ff
P_MTU34.TOER	Output enable setting for PWM waveform output pins	H'FFFF820A	H'ff
P_INTC.IPRE	Sets 15 as MTU channel 3 interrupt priority level	H'FFFF8350	H'00f0

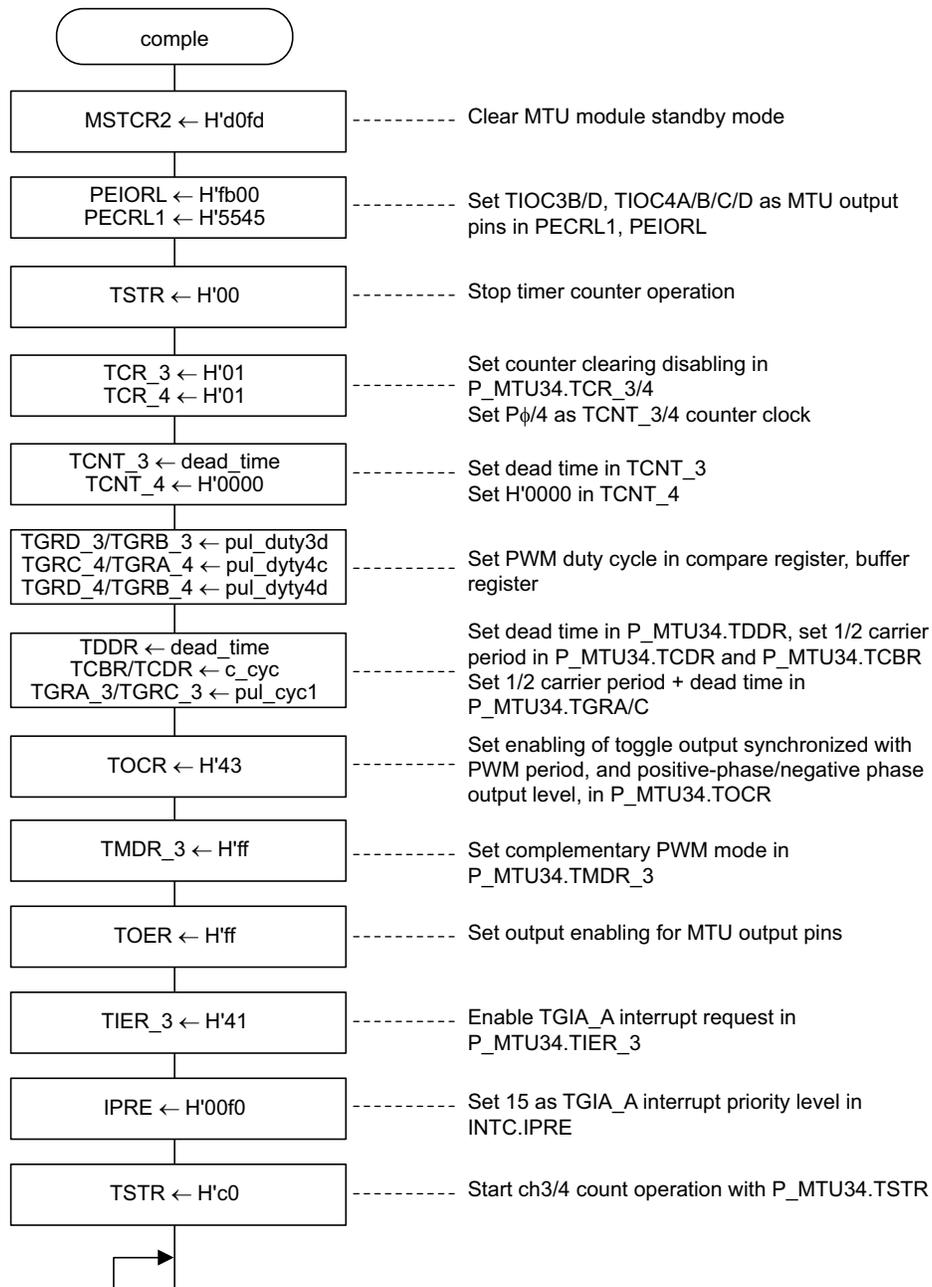
(4) RAM Used

This sample application does not use any RAM apart from the arguments.

Note: SH7145 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```

/*-----*/
/*          INCLUDE FILE          */
/*-----*/
#include <machine.h>
#include "iodefine_7145F.h"
/*-----*/
/*          PROTOTYPE          */
/*-----*/
extern void comple(void);
#pragma interrupt(setdata)
/*-----*/
/*          RAM ALLOCATION          */
/*-----*/
#define pul_cycl      (*(unsigned short *)0xffffe000)
#define pul_duty3d   (*(unsigned short *)0xffffe002)
#define pul_duty4c   (*(unsigned short *)0xffffe004)
#define pul_duty4d   (*(unsigned short *)0xffffe006)
#define c_cyc        (*(unsigned short *)0xffffe008)
#define dead_time    (*(unsigned short *)0xffffe00a)
/*-----*/
/*          MAIN PROGRAM          */
/*-----*/
void comple(void)
{
    P_STBY.MSTCR2.WORD = 0xd0fd;      /* MTU module standby mode clear */
    P_PORTE.PEIORL.WORD = 0xfb00;    /* TIOC3B/D,TIOC4A/B/C/D = output */
    P_PORTE.PECRL1.WORD = 0x5545;

    P_MTU34.TSTR.BYTE = 0x00;        /* Stop timer count */
    P_MTU34.TCR_3.BYTE = 0x01;       /* Don't clear TCNT_3 */
    P_MTU34.TCR_4.BYTE = 0x01;       /* Don't clear TCNT_4 */
    P_MTU34.TCNT_3 = dead_time;      /* Set dead time */
    P_MTU34.TCNT_4 = 0x0000;

    P_MTU34.TGRD_3 = pul_duty3d;     /* TGRB_3 buffer register */
    P_MTU34.TGRB_3 = pul_duty3d;     /* PWM output1 compare register */
    P_MTU34.TGRC_4 = pul_duty4c;     /* TGRA_4 buffer register */
    P_MTU34.TGRA_4 = pul_duty4c;     /* PWM output2 compare register */
    P_MTU34.TGRD_4 = pul_duty4d;     /* TGRB_4 buffer register */
    P_MTU34.TGRB_4 = pul_duty4d;     /* PWM output3 compare register */
    P_MTU34.TDDR = dead_time;        /* Dead time register */
    P_MTU34.TCBR = c_cyc;            /* 1/2 carrier period */
    P_MTU34.TCDR = c_cyc;            /* TCDR buffer register */
    P_MTU34.TGRA_3 = pul_cycl;        /* 1/2 carrier period + dead time */
    P_MTU34.TGRC_3 = pul_cycl;        /* TGRA_3 buffer register */
    P_MTU34.TOCR.BYTE = 0x43;        /* Timer output control register */
    P_MTU34.TMDR_3.BYTE = 0xff;      /* Set complementary-pwm mode */
    P_MTU34.TOER.BYTE = 0xff;        /* Timer output enable register */
    P_MTU34.TIER_3.BYTE = 0x41;      /* Timer interrupt enable register */

    INTC.IPRE.WORD = 0x00f0;         /* Set initialize level = 15 */
    set_imask(0x0);                 /* Set imask level = 0 */
    P_MTU34.TSTR.BYTE = 0xc0;        /* Start timer counter3/4 */
}

```

```
while(1);                                /* Loop */

void setdata()
{
    P_MTU34.TSR_3.BYTE &= 0xfe;          /* interrupt flag clear */
    P_MTU34.TCBR = c_cyc;
    P_MTU34.TGRC_3 = pul_cycl;
    P_MTU34.TGRD_3 = pul_duty3d;
    P_MTU34.TGRC_4 = pul_duty4c;
    P_MTU34.TGRD_4 = pul_duty4d;
}
```

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