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April 1st, 2010
Renesas Electronics Corporation

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SH7080/SH7146/SH7125/SH7200 Series

Synchronous Operation of MTU2 and MTU2S Timers

Introduction

This application note discusses synchronous operation of the MTU2 and MTU2S timers,

Target Device

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 40 MHz
- C compiler: Ver. 7.1.04 of Renesas C compiler

Contents

1. Specifications

(1) The MTU2 and the MTU2S start counting simultaneously.
(2) The MTU2 and the MTU2S count upward using channel 3, and the counters are cleared on compare-match between TGRA_3 and TGRA_3S.
(3) Toggle output synchronized with the compare-match period is output from the TIOC3A and the TIOC3AS pins.
(4) The MTU2 and the MTU2S perform counting with a 40-MHz clock.
(5) By running the MTU2 and MTU2S under the same conditions, the same waveforms are output by the two different modules.

Note: Synchronous starting of counters is possible in all operating modes. Two synchronous PWM waveforms can be produced by using the MTU2 and MTU2S in complementary PWM mode.

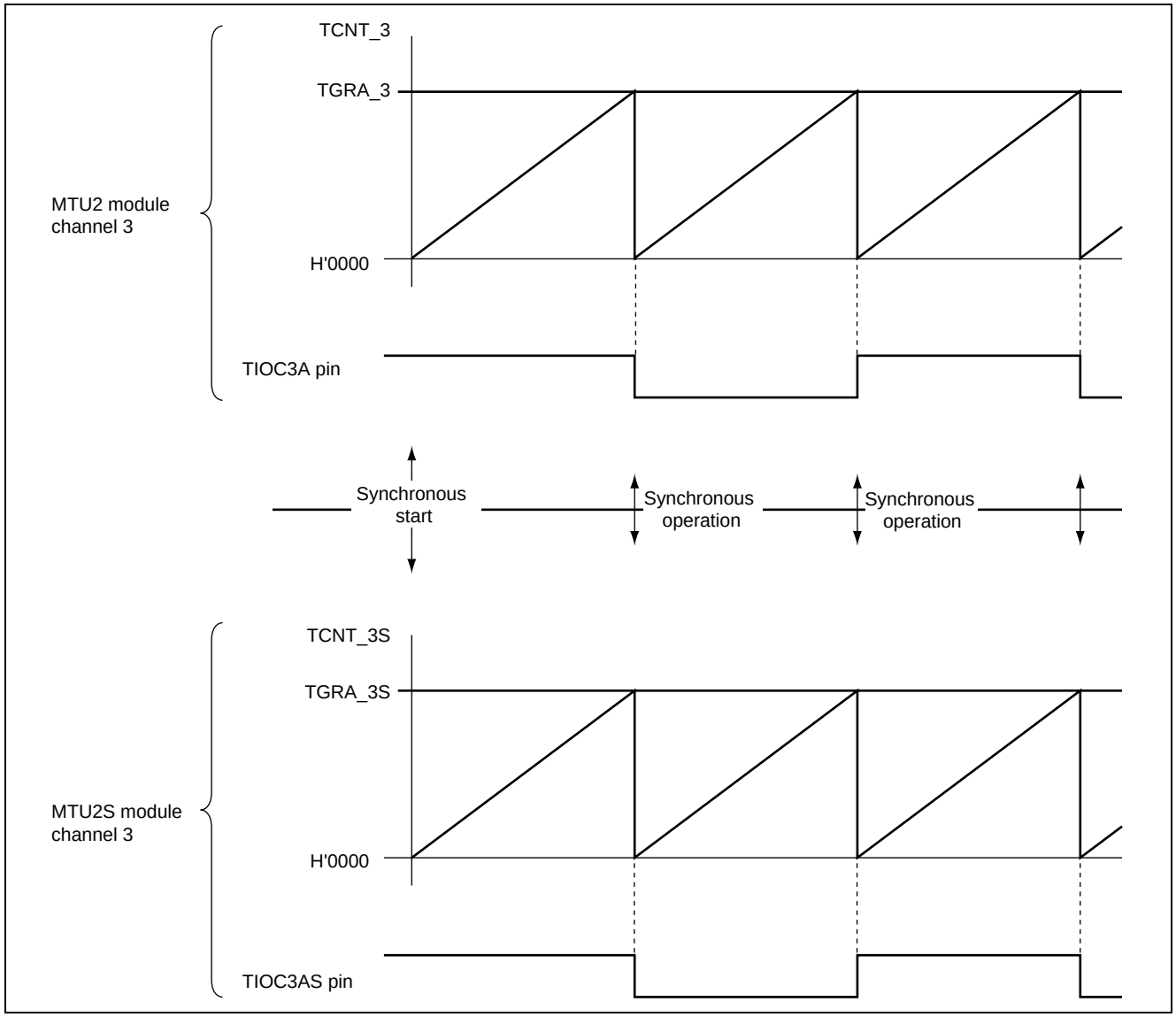


Figure 1 Synchronous Start of MTU2 and MTU2S Timers

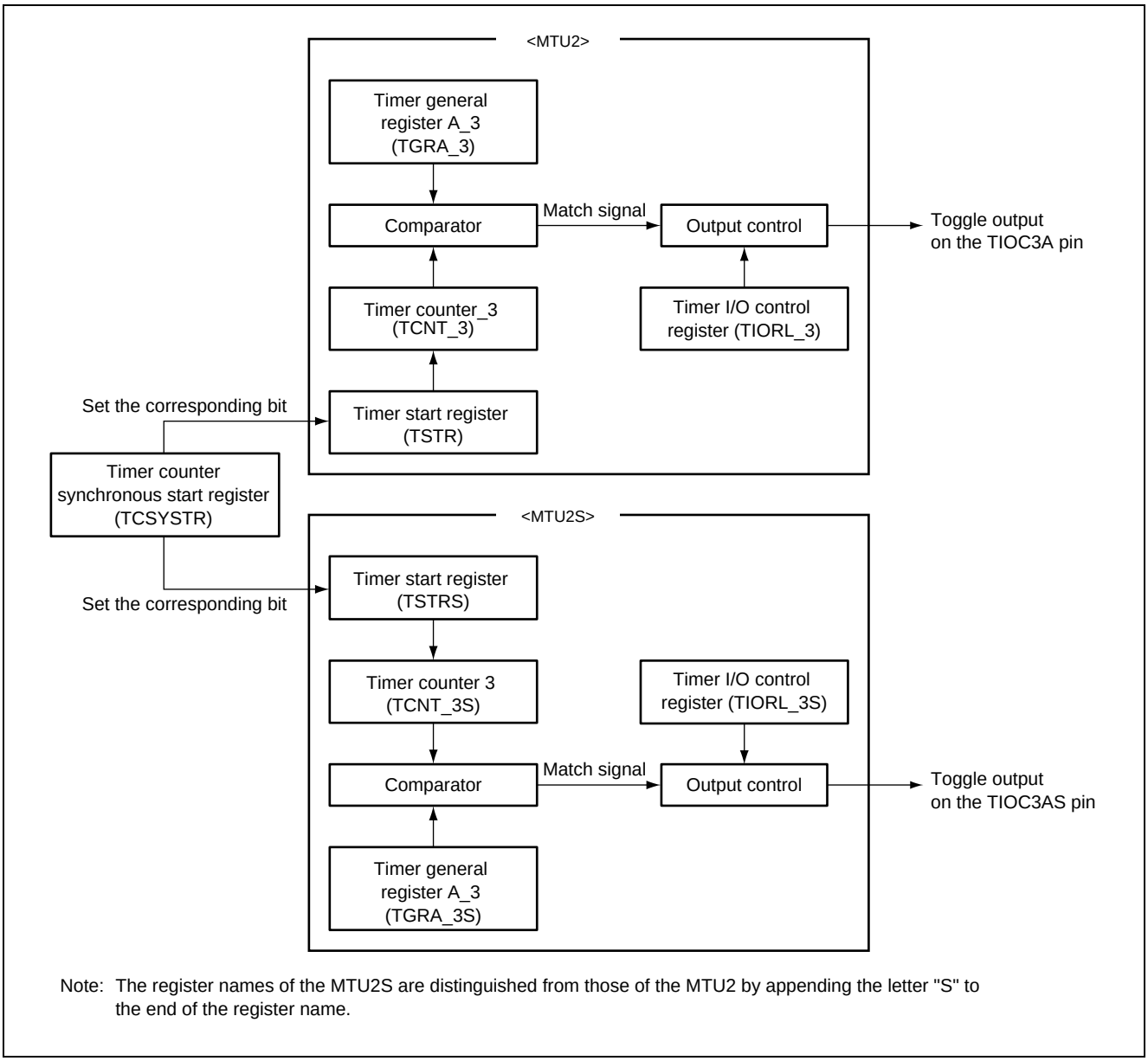
2. Description of Functions

In this sample task, counting operation is performed using channel 3 of the MTU2 and the MTU2S. The operating mode is normal mode.

Synchronous starting of counters is possible on channels, 0, 1, 2, 3 and 4 of the MTU2 and channels 3 and 4 of the MTU2S. Synchronous starting of counters is not possible on channel 5 of the MTU2 and MTU2S.

Figure 2 shows a block diagram of a part of the functions used in this sample task, with an explanation of the function noted below.

The MTU2S has the same configurations and functions as the channels 3, 4 and 5 of the MTU2.



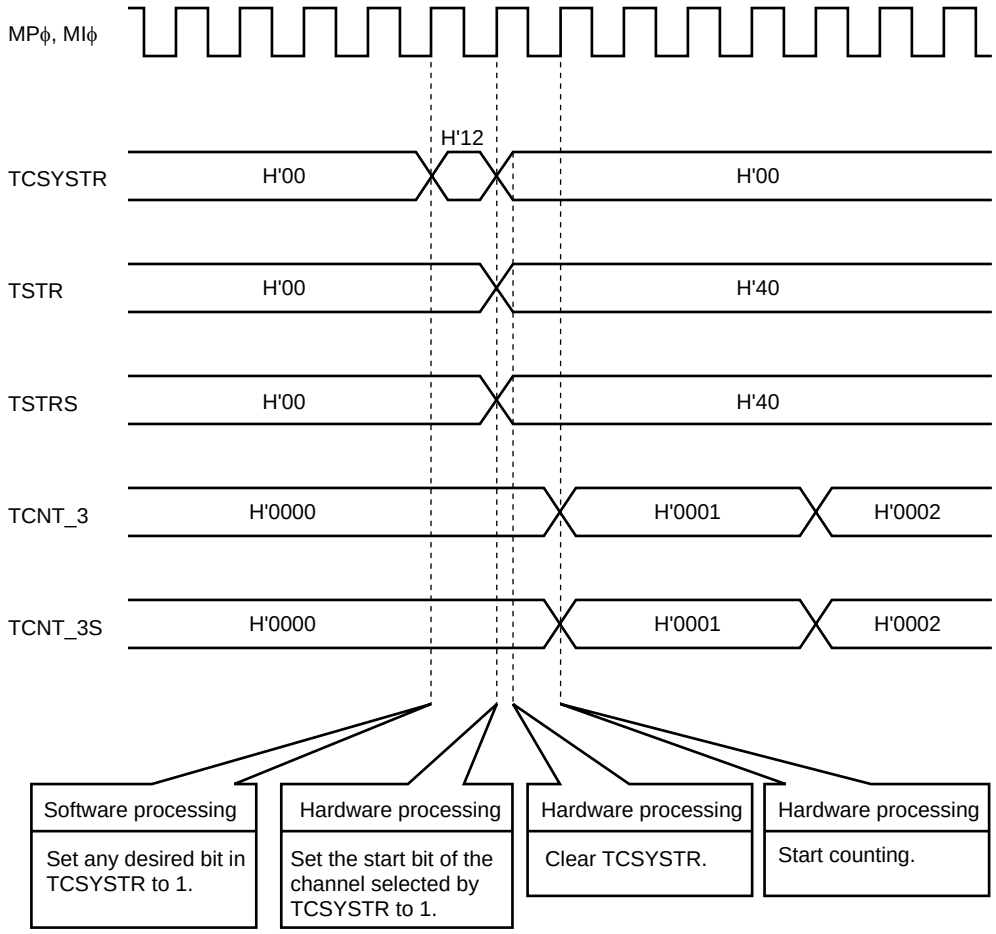
Note: The register names of the MTU2S are distinguished from those of the MTU2 by appending the letter "S" to the end of the register name.

Figure 2 Block Diagram of MTU2 (ch3) and MTU2S (ch3)

- The timer counter_3/3S (TCNT_3/3S) is a 16-bit readable/writable counter. This counter cannot be accessed in 8-bit units and must be accessed in 16-bit units.
- The timer general register A_3/3S (TGRA_3/3S) is a 16-bit readable/writable register. TGRA_3/3S operates as a compare register that is always compared with TCNT_3.
- The timer I/O control register L_3/3S (TIORL_3/3S) is a 16-bit readable/writable register. TIORL_3/3S sets the functions of the TGRA_3/3S and the TIOC3A/3AS pin.
- The timer start register/S (TSTR/S) is an 8-bit readable/writable register. TSTR/S starts/stops counting by TCNT_3/3S.
- The timer counter synchronous start register (TCSYSTR) is an 8-bit readable/writable register. TCSYSTR enables synchronous starting of the MTU2 and MTU2S counters. When the bit in TCSYSTR for the counter to be started synchronously is set to 1, the corresponding bit in TSTR of the MTU2 or MTU2S is set. The bit in TCSYSTR is automatically cleared after the relevant counter of the MTU2 or MTU2S has been started.

3. Description of Operation

Figure 3 explains how the MTU2 and MTU2S timers start synchronously.



Notes: 1. The counter clock for TCNT_3 is MPϕ/1 and that for TCNT_3S is MIϕ /1.
2. The counters count the rising edges.
3. Since TCSYSTR is a register in the MTU2 module, it operates synchronously with MPϕ.
4. To stop the timer, clear the corresponding bit in the TSTR register.

Figure 3 Synchronous Starting of MTU2 and MTU2S Timers

4. Description of Software

4.1 Modules

Table 1 describes the module of this sample task.

Table 1 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Makes initial settings of the MTU2 and MTU2S and starts the timer counters.

4.2 Internal Registers

Table 2 shows the registers used in this sample task. Note that the settings in the tables are the values used in this sample task, and are different from the initial values.

Table 2 Description of Internal Registers

Register	Bit	Bit Name	Function	Setting
FRQCR			Frequency Control Register Specifies the ratios for dividing the output frequency of the PLL circuit to generate operating clocks. FRQCR = H'0249 sets the division ratios as follows. Internal clock: ×1 Bus clock: ×1/2 Peripheral clock: ×1/2 MTU2S clock: ×1/2 MTU2 clock: ×1/2	H'0249
STBCR4			Standby Control Register 4	H'3F
	7	MSTP23	Module Stop 23 Clock is supplied to MTU2S when MSTP23 = b'0.	0
	6	MSTP22	Module Stop 22 Clock is supplied to MTU2 when MSTP22 = b'0.	0
PECRL3			Port E Control Register L3	H'0001
	15	—	Reserved	0
	14	PE11MD2	PE11 Mode	0
	13	PE11MD1	Selects PE11 (general I/O) as the pin function when	0
	12	PE11MD0	PE11MD2 to PE11MD0 = b'000.	0
	11	—	Reserved	0
	10	PE10MD2	PE10 Mode	0
	9	PE10MD1	Selects PE10 (general I/O) as the pin function when	0
	8	PE10MD0	PE10MD2 to PE10MD0 = b'000	0

Register	Bit	Bit Name	Function	Setting
PECRL3	7	—	Reserved	0
	6	PE9MD2	PE9 Mode	0
	5	PE9MD1	Selects PE9 (general I/O) as the pin function when	0
	4	PE9MD0	PE9MD2 to PE9MD0 = b'000.	0
	3	—	Reserved	0
	2	PE8MD2	PE8 Mode	0
	1	PE8MD1	Selects TIOC3A as the pin function when PE8MD2 to	0
	0	PE8MD0	PE8MD0 = b'001.	1
PDCRH4			Port D Control Register H4	H'3000
	15	—	Reserved	0
	14	—		0
	13	PD31MD1	PD31 Mode	1
	12	PD31MD0	Selects TIOC3AS as the pin function when PD31MD1 and PD31MD0 = b'11.	1
	11	—	Reserved	0
	10	—		0
	9	PD30MD1	PD30 Mode	0
	8	PD30MD0	Selects PD30 (general I/O) as the pin function when PD30MD1 and PD30MD0 = b'00.	0
	7	—	Reserved	0
	6	—		0
	5	PD29MD1	PD29 Mode	0
	4	PD29MD0	Selects PD29 (general I/O) as the pin function when PD29MD1 and PD29MD0 = b'00.	0
	3	—	Reserved	0
	2	—		0
	1	PD28MD1	PD28 Mode	0
	0	PD28MD0	Selects PD28 (general I/O) as the pin function when PD28MD1 and PD28MD0 = b'00.	0

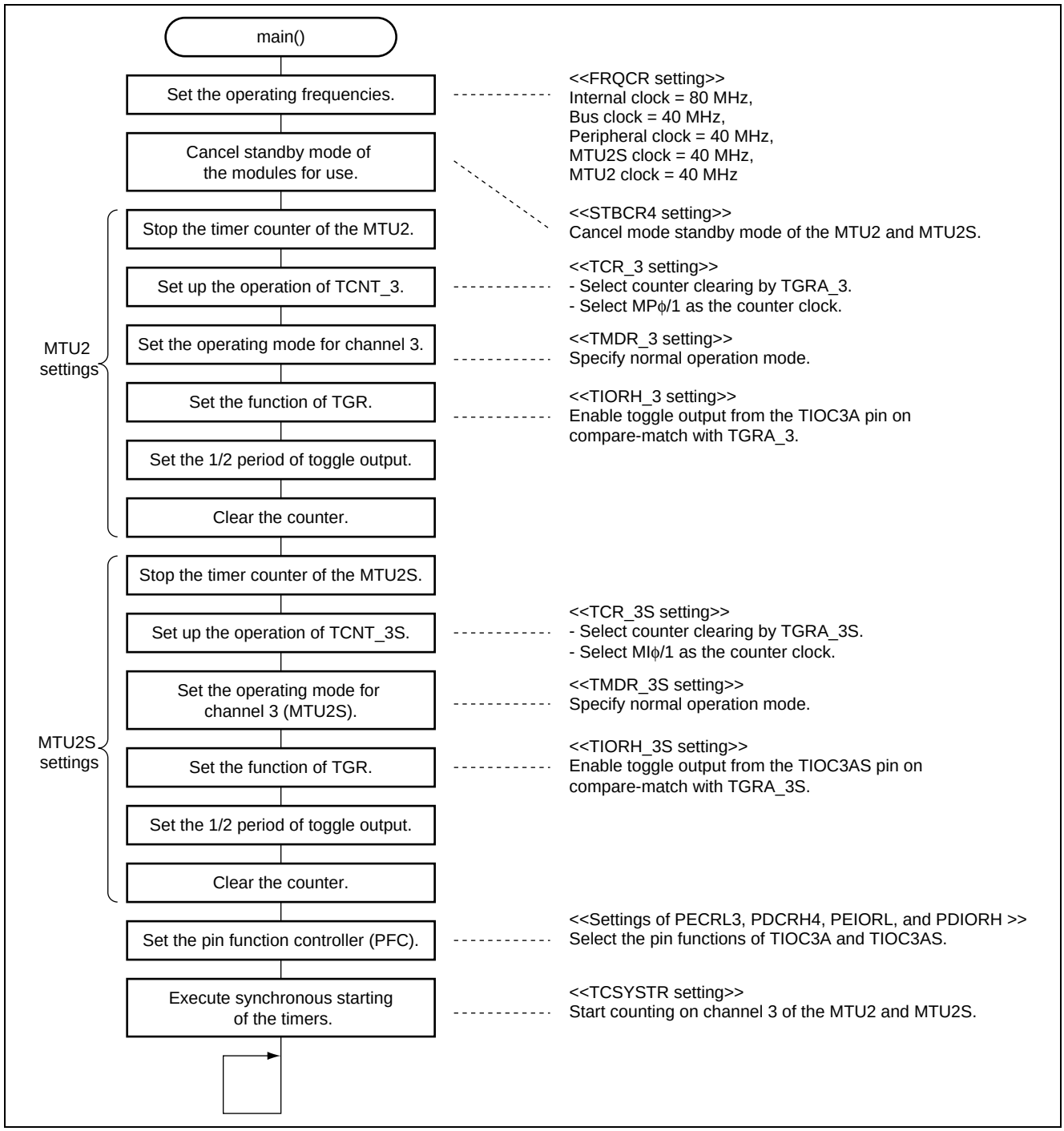
Register	Bit	Bit Name	Function	Setting
TSTR			Timer Start Register	H'00
	7	CTS4	Counter Start 4 When CTS4 = b'0, TCNT_4 stops counting.	0
	6	CTS3	Counter Start 3 When CTS3 = b'0, TCNT_3 stops counting.	0
	5	—	Reserved	0
	4	—		0
	3	—		0
	2	CTS2	Counter Start 2 When CTS2 = b'0, TCNT_2 stops counting.	0
	1	CTS1	Counter Start 1 When CTS1 = b'0, TCNT_1 stops counting.	0
	0	CTS0	Counter Start 0 When CTS0 = b'0, TCNT_0 stops counting.	0
TCR_3			Timer Control Register_3	H'20
	7	CCLR2	Counter Clear 2, 1, 0	0
	6	CCLR1	Clears TCNT_3 on compare-match with TGRA_3 when	0
	5	CCLR0	CCLR2 to CCLR0 = b'001.	1
	4	CKEG1	Clock Edge 1, 0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_3 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2, 1, 0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'000, the clock source for	0
	0	TPSC0	TCNT_3 is MPϕ/1.	0
TMDR_3			Timer Mode Register_3	H'00
	7	—	Reserved	0
	6	—	Reserved	0
	5	BFB	Buffer Operation B When BFB = b'0, TGRB_3 and TGRD_3 operate normally.	0
	4	BFA	Buffer Operation A When BFA=b'0, TGRA_3 and TGRC_3 operate normally.	0
	3	MD3	Mode 3, 2, 1, 0	0
	2	MD2	When MD3 to MD0 = b'0000, the MTU2 operates in	0
	1	MD1	normal operation mode.	0
	0	MD0		0

Register	Bit	Bit Name	Function	Setting
TIORH_3			Timer I/O Control Register H_3	H'07
	7	IOB3	I/O control B3 to B0	0
	6	IOB2	When IOB3 to IOB0 = b'0000, TGRB_3 operates as an	0
	5	IOB1	output compare register and the output on the TIOC3B pin	0
	4	IOB0	is held.	0
	3	IOA3	I/O control A3 to A0	0
	2	IOA2	When IOA3 to IOA0 = b'0111, TGRA_3 operates as an	1
	1	IOA1	output compare register and the TIOC3A pin initially	1
	0	IOA0	outputs high level and toggles the output on compare-match.	1
TGRA_3			Timer General Register A_3 Sets the period of compare-match with TCNT_3	H'A000
TCNT_3			Timer Counter _3	H'0000
TSTRS			Timer Start Register S	H'00
	7	CTS4	Counter Start 4 When CTS4 = b'0, TCNT_4S stops counting	0
	6	CTS3	Counter Start 3 When CTS3 = b'0, TCNT_3S stops counting.	0
	5	—	Reserved	0
	4	—		0
	3	—		0
	2	—		0
	1	—		0
	0	—		0
TCR_3S			Timer Control Register_3S	H'20
	7	CCLR2	Counter Clear 2, 1, 0	0
	6	CCLR1	Clears TCNT_3S on compare match with TGRA_3S when	0
	5	CCLR0	CCLR2 to CCLR0 = b'001.	1
	4	CKEG1	Clock Edge 1,0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_3S counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2, 1, 0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'000, the clock source for	0
	0	TPSC0	TCNT_3S is MIϕ/1.	0

Register	Bit	Bit Name	Function	Setting
TMDR_3S			Timer Mode Register_3S	H'00
	7	—	Reserved	0
	6	—	Reserved	0
	5	BFB	Buffer Operation B When BFB = b'0, TGRB_3S and TGRD_3S operate normally.	0
	4	BFA	Buffer Operation A When BFA=b'0, TGRA_3S and TGRC_3S operate normally.	0
	3	MD3	Mode 3,2,1,0	0
	2	MD2	When MD3 to MD0 = b'0000, the MTU2S operates in	0
	1	MD1	normal mode.	0
	0	MD0		0
TIORH_3S			Timer I/O Control Register H_3S	H'07
	7	IOB3	I/O control B3 to B0	0
	6	IOB2	When IOB3 to IOB0 = b'0000, MTU2S_TGRB_3 operates	0
	5	IOB1	as an output compare register and the output on the	0
	4	IOB0	TIOC3B pin is held.	0
	3	IOA3	I/O control A3 to A0	0
	2	IOA2	When IOA3 to IOA0 = b'0111, TGRA_3S operates as an	1
	1	IOA1	output compare register and the TIOC3A pin initially	1
	0	IOA0	outputs high level and toggles the output on compare-match.	1
TGRA_3S			Timer General Register A_3S Sets the period of compare-match with TCNT_3S	H'A000
TCNT_3S			Timer Counter_3S	H'0000

Register	Bit	Bit Name	Function	Setting
TCSYSTR			Timer Counter Synchronous Start Register	H'12
	7	SCH0	Synchronous Start 0 When SCH0 = b'0, TCNT_0 of MTU2 doesn't start synchronously.	0
	6	SCH1	Synchronous Start 1 When SCH1 = b'0, TCNT_1 of MTU2 doesn't start synchronously.	0
	5	SCH2	Synchronous Start 2 When SCH2 = b'0, TCNT_2 of MTU2 doesn't start synchronously.	0
	4	SCH3	Synchronous Start 3 When SCH3 = b'1, TCNT_3 of MTU2 starts synchronously.	1
	3	SCH4	Synchronous Start 4 When SCH4 = b'0, TCNT_4 of MTU2 doesn't start synchronously.	0
	2	—	Reserved	0
	1	SCH3S	Synchronous Start 3S When SCH3S = b'1, TCNT_3 of MTU2S starts synchronously	1
	0	SCH4S	Synchronous Start 4S When SCH4S = b'0, TCNT_4 of MTU2S doesn't start synchronously.	0

5. Flowchart


main()
Set the operating frequencies.
<<FRQCR setting>>
Internal clock = 80 MHz,
Bus clock = 40 MHz,
Peripheral clock = 40 MHz,
MTU2S clock = 40 MHz,
MTU2 clock = 40 MHz
Cancel standby mode of the modules for use.
<<STBCR4 setting>>
Cancel mode standby mode of the MTU2 and MTU2S.
MTU2 settings
Stop the timer counter of the MTU2.
Set up the operation of TCNT_3.
<<TCR_3 setting>>
- Select counter clearing by TGRA_3.
- Select MPϕ/1 as the counter clock.
Set the operating mode for channel 3.
<<TMDR_3 setting>>
Specify normal operation mode.
Set the function of TGR.
<<TIORH_3 setting>>
Enable toggle output from the TIOC3A pin on compare-match with TGRA_3.
Set the 1/2 period of toggle output.
Clear the counter.
MTU2S settings
Stop the timer counter of the MTU2S.
Set up the operation of TCNT_3S.
<<TCR_3S setting>>
- Select counter clearing by TGRA_3S.
- Select MIϕ/1 as the counter clock.
Set the operating mode for channel 3 (MTU2S).
<<TMDR_3S setting>>
Specify normal operation mode.
Set the function of TGR.
<<TIORH_3S setting>>
Enable toggle output from the TIOC3AS pin on compare-match with TGRA_3S.
Set the 1/2 period of toggle output.
Clear the counter.
Set the pin function controller (PFC).
<<Settings of PECRL3, PDCRH4, PEIORL, and PDIORH >>
Select the pin functions of TIOC3A and TIOC3AS.
Execute synchronous starting of the timers.
<<TCSYSTR setting>>
Start counting on channel 3 of the MTU2 and MTU2S.

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