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SH7080/SH7146/SH7125/SH7200 Series

Activating the A/D Converter Using Compare-Match on MTU2 Channel 0

Introduction

This application note discusses activating the A/D converter by using compare match with TGRE_0 on channel 0 (ch0) of the MTU2. This function enables A/D conversion at the desired timing while, for instance, a PWM waveform is output.

Target Device

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler: Ver. 7.1.04 of Renesas C compiler

Contents

1. Specifications

In this task sample, channel 0 (ch0) of MTU2 is used to activate the A/D converter and performs A/D conversion of the voltage applied to the AN0 pin. The specifications for this sample task are as shown below.

- MTU2 ch0 operates in PWM mode 1 and outputs PWM waveforms from the TIOC0A pin.
- MTU2 ch0 activates the A/D converter by compare match with TGRE_0.
- The result of A/D conversion is stored to on-chip RAM.
- The A/D converter operates in single mode.
- When A/D conversion has been performed three times, the timer counter of MTU2 ch0 stops counting.

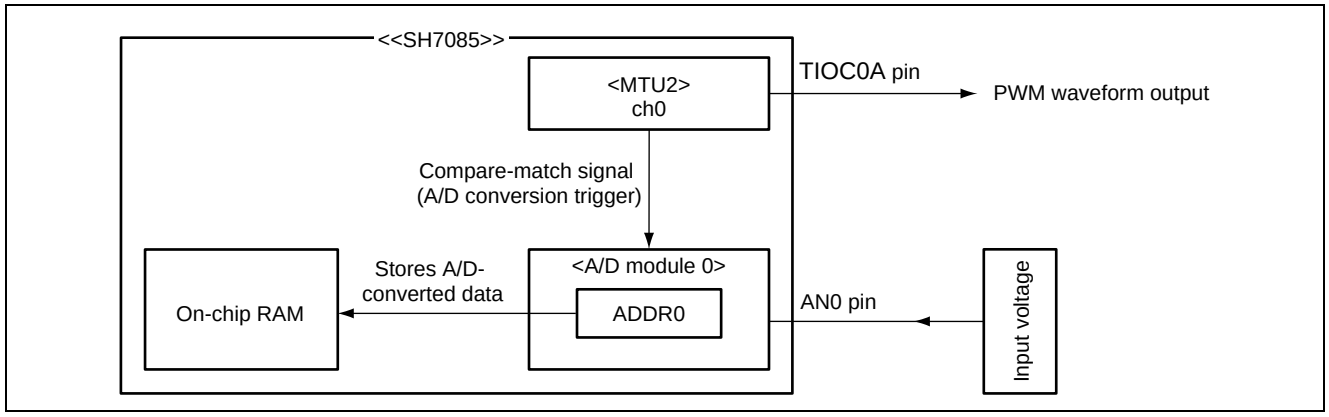


Figure 1 Block Diagram of A/D Conversion Controlled by MTU2

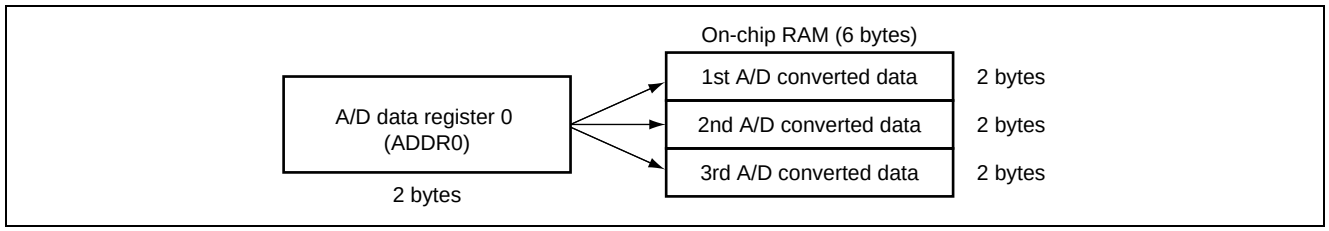


Figure 2 Storing A/D Converted Data to On-chip RAM

2. Description of Functions

In this sample task, the A/D converter is activated by compare match on MTU2 ch0.

2.1 MTU2 (Multi-Function Timer Pulse Unit 2)

Channel 0 of the MTU2 is used in PWM mode 1. Figure 3 shows a block diagram of MTU2 ch0 and its registers are described below.

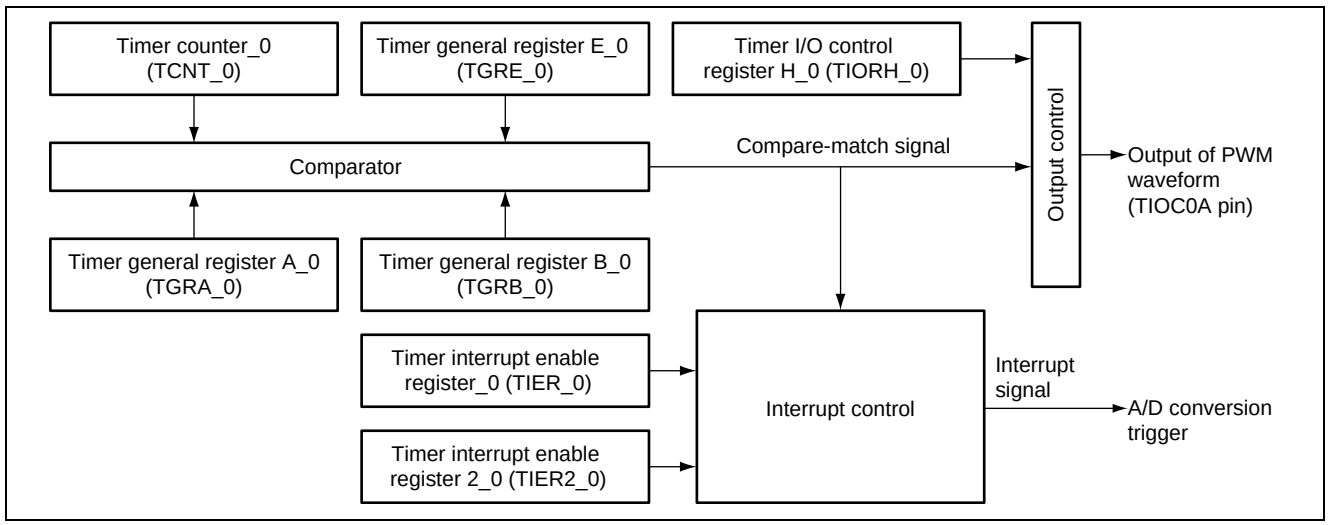


Figure 3 Block Diagram of MTU2 ch0

- The timer general register A_0 (TGRA_0) operates as a compare register. The period of PWM waveform is set in TRGA_0.
- The timer general register B_0 (TGRB_0) operates as a compare register. The duty cycle of PWM waveform is set in TGRB_0.
- The timer general register E_0 (TGRE_0) operates as a compare register. The timing of A/D conversion is set in TGRE_0.
- The timer counter_0 (TCNT_0) is a 16-bit readable/writable counter. TCNT_0 is cleared on compare match with TGRA_0.
- The timer I/O control register H_0 (TIORH_0) is an 8-bit readable/writable register that specifies the functions of TGRA_0 and TGRB_0 and the output level of the TIOC0A pin.
- The timer interrupt enable register_0 (TIER_0) is an 8-bit readable/writable register that enables or disables interrupt requests.
- The timer interrupt enable register 2_0 (TIER2_0) is an 8-bit readable/writable register that enables or disables interrupt requests related to TGRE_0 and TGRF_0 and activation of the A/D converter using TGRE_0.

2.2 A/D Converter

In this sample task, the A/D module 0 is activated by the A/D conversion trigger generated by the MTU2, and performs A/D conversion in single mode. Figure 4 shows a block diagram of the A/D 0 module, with a description of the functions noted below.

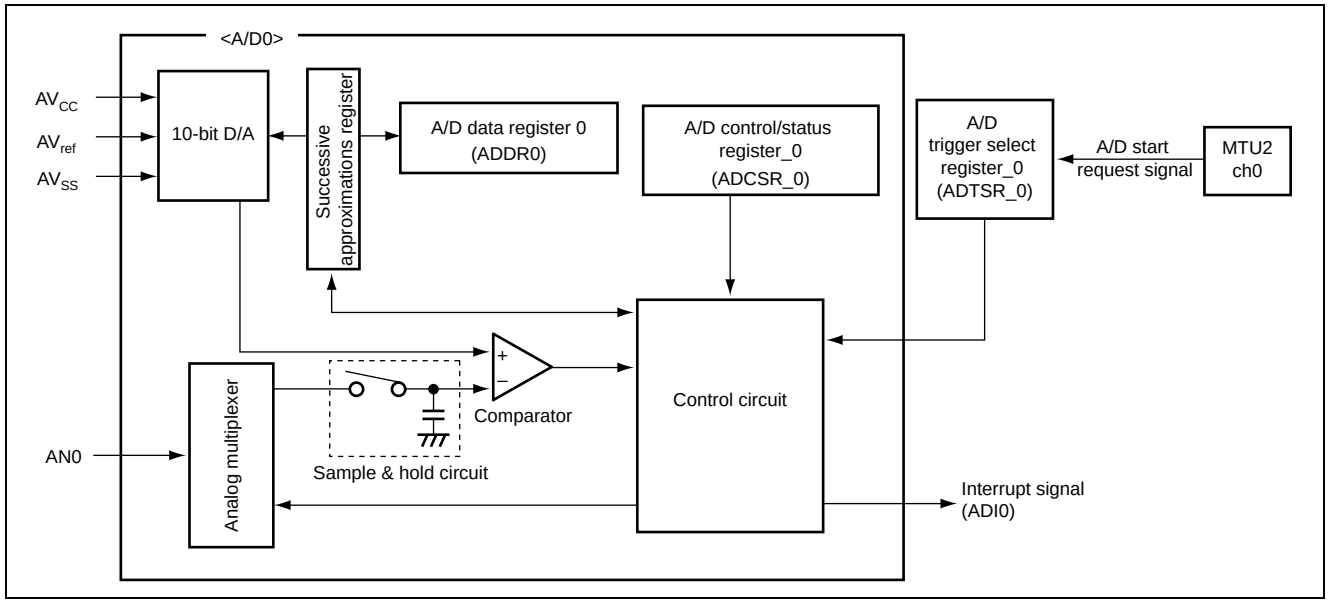


Figure 4 Block Diagram of A/D Module 0

- The A/D data register 0 (ADDR0) is a 16-bit read only register that is used to store the A/D-converted result of the data input from the analog input channel (AN0). The converted data is stored to the upper 10 bits (bits 15 to 6), and the lower 6 bits are always 0.
- The A/D control/status register_0 (ADCSR_0) controls A/D conversion operation.
- The A/D trigger select register_0 (ADTSR_0) selects an external trigger to start A/D conversion.

3. Description of Operation

Figure 5 illustrates the operation of this sample task, and table 1 describes the operation in terms of software and hardware processing.

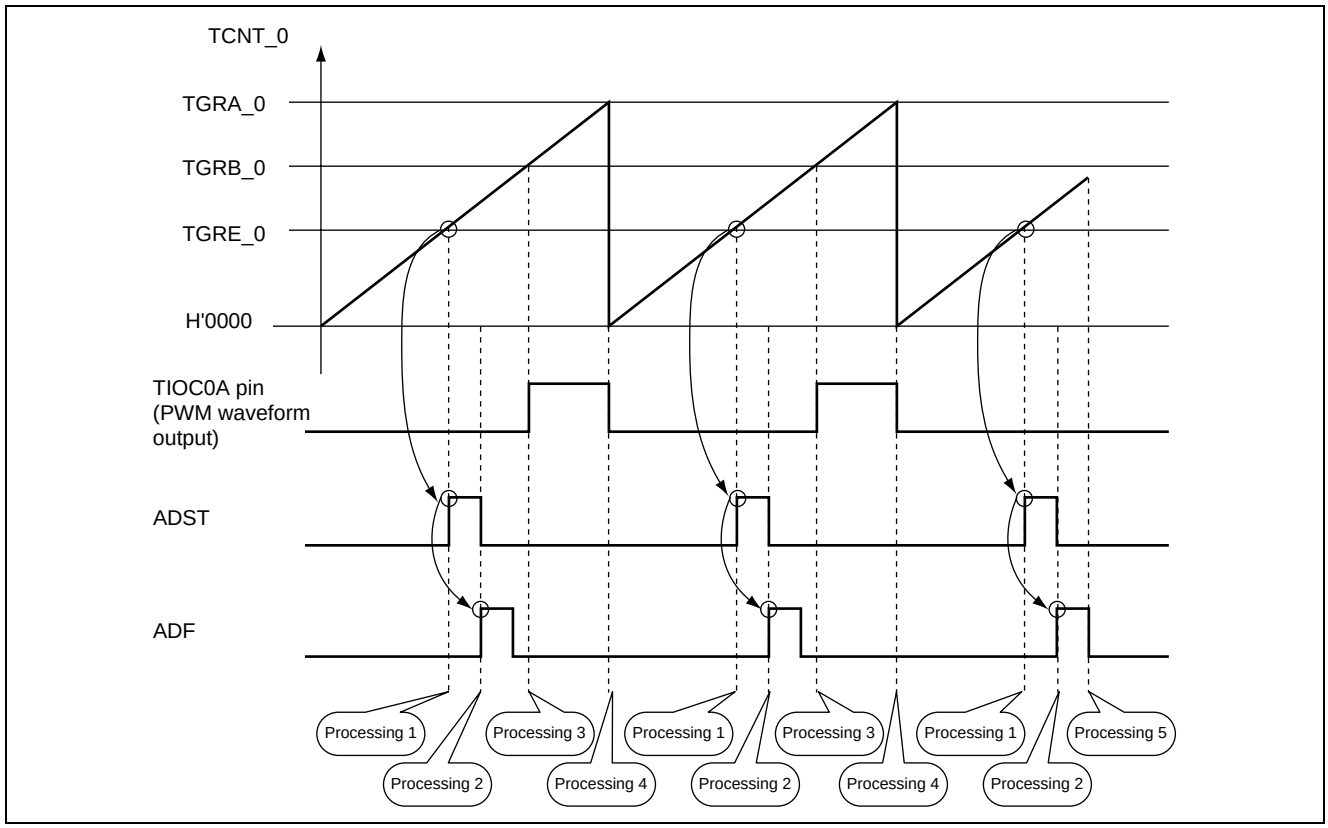


Figure 5 Principles of Operation

Table 1 Software and Hardware Processing

	Software Processing	Hardware Processing
Processing 1	—	Activate the A/D converter on compare-match between TCNT_0 and TGRE_0. (Start A/D conversion.)
Processing 2	• Clear the ADF flag at an A/D conversion end interrupt. • Store the result of A/D conversion to on-chip RAM.	• Set the ADF flag to 1 on completion of A/D conversion. • Generate an A/D conversion end interrupt.
Processing 3	—	Output a high level from the TIOC0A pin on compare-match between TCNT_0 and TGRB_0.
Processing 4	• Clear the TGFA_0 flag at a TGRA_0 compare-match interrupt. • Update the duty cycle (TGRB_0) and A/D conversion timing (TGRE_0).	• Output a low level from TIOC0A pin on compare-match between TCNT_0 and TGRA_0. • Clear TCNT_0. • Generate a TGRA_0 compare-match interrupt.
Processing 5	Clear the CTS0 bit in the TSTR register.	Stop the timer counter of MTU2 ch0.

4. Description of Software

4.1 Modules

Table 2 describes the modules of this sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main0	Makes initial settings of the MTU2 and A/D converter and starts the timer counter.
TGRA_0 interrupt routine	int_tgia0()	Updates the duty cycle and period of A/D converter activation.
A/D conversion end interrupt routine	int_ad0()	Stores the result of A/D conversion to on-chip RAM and stops the timer counter.

4.2 Internal Registers

Table 3 shows the registers used in this sample task. Note that the settings in the tables are the values used in this sample task, and are different from their initial values.

Table 3 Description of Internal Registers

Register	Bit	Bit Name	Function	Setting
FRQCR			Frequency Control Register Specifies the ratios for dividing the output frequency of the PLL circuit to generate operating clocks. FRQCR = H'0241 sets the division ratios as follows. Internal clock: ×1 Bus clock: ×1/2 Peripheral clock: ×1/2 MTU2S clock: ×1 MTU2 clock: ×1/2	H'0241
STBCR4			Standby Control Register 4	H'BE
	6	MSTP22	Module Stop 22 Clock is supplied to MTU2 when MSTP22 = b'0.	0
	0	MSTP16	Module Stop 16 Clock is supplied to AD_0 when MSTP16 = b'0.	0
PECRL1			Port E Control Register L3	H'0001
	15	—	Reserved	0
	14	PE3MD2	PE3 Mode	0
	13	PE3MD1	Selects PE3 (general I/O) as the pin function when	0
	12	PE3MD0	PE3MD2 to PE3MD0 = b'000.	0
	11	—	Reserved	0
	10	PE2MD2	PE2 Mode	0
	9	PE2MD1	Selects PE2 (general I/O) as the pin function when	0
	8	PE2MD0	PE2MD2 to PE2MD0 = b'000.	0

Register	Bit	Bit Name	Function	Setting
PECRL1	7	—	Reserved	0
	6	PE1MD2	PE1 Mode	0
	5	PE1MD1	Selects PE1 (general I/O) as the pin function when	0
	4	PE1MD0	PE1MD2 to PE1MD0 = b'000.	0
	3	—	Reserved	0
	2	PE0MD2	PE0 Mode	0
	1	PE0MD1	Selects TIOC0A as the pin function when PE0MD2 to	0
	0	PE0MD0	PE0MD0 = b'001.	1
PEIORL			Port E I/O Register L	H'0001
	0	PE0IOR	Sets the PE0 (TIOC0A) pin to function as an output pin when PE0IOR = b'1.	1
IPRD			Interrupt Priority Register D Sets the TGIA_0 interrupt level of the MTU2 to 10. the interrupt level of TGIA_0 to 10.	H'A000
IPRK			Interrupt Priority Register K Sets the ADI_0 interrupt level of the A/D converter to10.	H'A000
ADCSR_0			A/D Control/Status Register_0	H'5880
	15	ADF	A/D End Flag	0
	14	ADIE	A/D Interrupt Enable Enables ADI interrupts when ADIE = b'1.	1
	13	—	Reserved	0
	12	OPON	Operational Amplifier ON Enables the operational amplifier when OPON = b'1.	1
	11	TRGE	Trigger Enable Specifies to start A/D conversion by an external trigger or MTU2 (MTU2S) trigger when TRGE = b'1.	1
	10	—	Reserved	0
	9	CONADF	ADF Control The setting of this bit is invalid because single mode is used in this sample task.	0
	8	STC	State Control Sets the A/D conversion time to 50 states when STC = b'0.	0
	7	CKSL1	Clock Select 1,0	1
	6	CKSL0	Selects Pϕ/2 as the clock for A/D conversion when CKSL1 and CKSL0 = b'10.	0
	5	ADM1	A/D Mode 1,0	0
	4	ADM0	Selects single mode operation when ADM1 and ADM0 = b'00.	0
	3	ADCS	A/D Continuous Scan Specifies single-cycle scanning when ADCS = b'0.	0
	2	CH2	Channel Select 2,1,0	0
	1	CH1	Selects AN0 as the analog input channel for A/D	0
	0	CH0	conversion when CH2 to CH0 = b'000.	0

Register	Bit	Bit Name	Function	Setting
ADTSR_0			A/D Trigger Select Register_0 Selects compare match (TRG0N) on MTU2 ch0 as the A/D conversion trigger for A/D module 0.	H'0002
TCR_0			Timer Control Register_0	H'21
	7	CCLR2	Counter Clear 2, 1, 0	0
	6	CCLR1	When CCLR2 to CCLR0 = b'001, TCNT_0 is cleared on	0
	5	CCLR0	compare match with TGRA_0.	1
	4	CKEG1	Clock Edge 1, 0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_0 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler	0
	1	TPSC1	When TPSC2 to TPSC0 = b'001, the clock source for	0
	0	TPSC0	TCNT_0 is MPϕ/4.	1
TMDR_0			Timer Mode Register_0	H'02
	7	—	Reserved	0
	6	BFE	Buffer Operation E Selects normal operation of TGRE_0 and TGRF_0 when BFE = b'0.	0
	5	BFB	Buffer Operation B Selects normal operation of TGRB_0 and TGRD_0 when BFB = b'0.	0
	4	BFA	Buffer Operation A Selects normal operation of TGRA_0 and TGRC_0 when BFA = b'0.	0
	3	MD3	Mode 3, 2, 1, 0	0
	2	MD2	The timer operates in PWM mode 1 when MD3 to MD0 =	0
	1	MD1	b'0010.	1
	0	MD0		0
TIORH_0			Timer I/O Control Register	H'21
	7	IOB3	I/O Control B3 to B0	0
	6	IOB2	When IOB3 to IOB0 = b'0010, the TIOC0A pin outputs 1	0
	5	IOB1	on compare match with TGRB_0 and its initial output is 0.	1
	4	IOB0		0
	3	IOA3	I/O Control A3 to A0	0
	2	IOA2	When IOA3 to IOA0 = b'0001, the TIOC0A pin outputs 0	0
	1	IOA1	on compare match with TGRA_0 and its initial output is 0.	0
	0	IOA0		1

Register	Bit	Bit Name	Function	Setting
TIER_0			Timer Interrupt Enable Register_0	H'01
	7	TTGE	A/D Conversion Start Request Enable Disables generation of A/D conversion start requests by compare match with TGRA_0 when TTGE = b'0.	0
	6	—	Reserved	0
	5	—	Reserved	0
	4	TCIEV	Overflow Interrupt Enable Disables interrupt requests by TCFV when TCIEV = b'0.	0
	3	TGIED	TGR Interrupt Enable D Disables interrupt requests by the TGFD bit when TGIED = b'0.	0
	2	TGIEC	TGR Interrupt Enable C Disables interrupt requests by the TGFC bit when TGIEC = b'0.	0
	1	TGIEB	TGR Interrupt Enable B Disables interrupt requests by the TGFB bit when TGIEB = b'0.	0
	0	TGIEA	TGR Interrupt Enable A Enables interrupt requests by the TGFA bit when TGIEA = b'1.	1
TIER2_0			Timer Interrupt Enable Register 2_0	H'80
	7	TTGE2	A/D Conversion Start Request Enable 2 Enables generation of A/D conversion start requests by compare match with TGRE_0 when TTGE2 = b'1.	1
	6	—	Reserved	0
	5	—		0
	4	—		0
	3	—		0
	2	—		0
	1	TGIEF	TGR Interrupt Enable F Disables interrupt requests by the TGFF bit when TGIEF = b'0.	0
	0	TGIEE	TGR Interrupt Enable E Disables interrupt requests by the TGFE bit when TGIEE = b'0.	0
TGRA_0			Timer General Register A_0 On compare match between TCNT_0 and TGRA_0, the counter (TCNT_0) is cleared and 0 is output from the TIOC0A pin. The period of PWM waveform is set in this register.	Pul_cyc
TGRB_0			Timer General Register B_0 On compare match between TCNT_0 and TGRB_0, 1 is output from the TIOC0A pin. The duty cycle of PWM waveform is set in this register.	Duty

Register	Bit	Bit Name	Function	Setting
TGRE_0			Timer General Register E_0 On compare match between TCNT_0 and TGRB_0, the A/D converter is activated. The timing of A/D converter activation is set in this register.	Ad_start
TCNT_0			Timer Counter_0 The timer counter for channel 0	H'0000
TSTR			Timer Start Register	H'01
	7	CTS4	Count Start 4 TCNT_4 stops counting when CTS4 = b'0.	0
	6	CTS3	Count Start 3 TCNT_3 stops counting when CTS3 = b'0.	0
	5	—	Reserved	0
	4	—	Reserved	0
	3	—	Reserved	0
	2	CTS2	Count Start 2 TCNT_2 stops counting when CTS2 = b'0.	0
	1	CTS1	Count Start 1 TCNT_1 stops counting when CTS1 = b'0.	0
	0	CTS0	Count Start 0 TCNT_0 starts counting when CTS0 = b'1.	1

4.3 Arguments

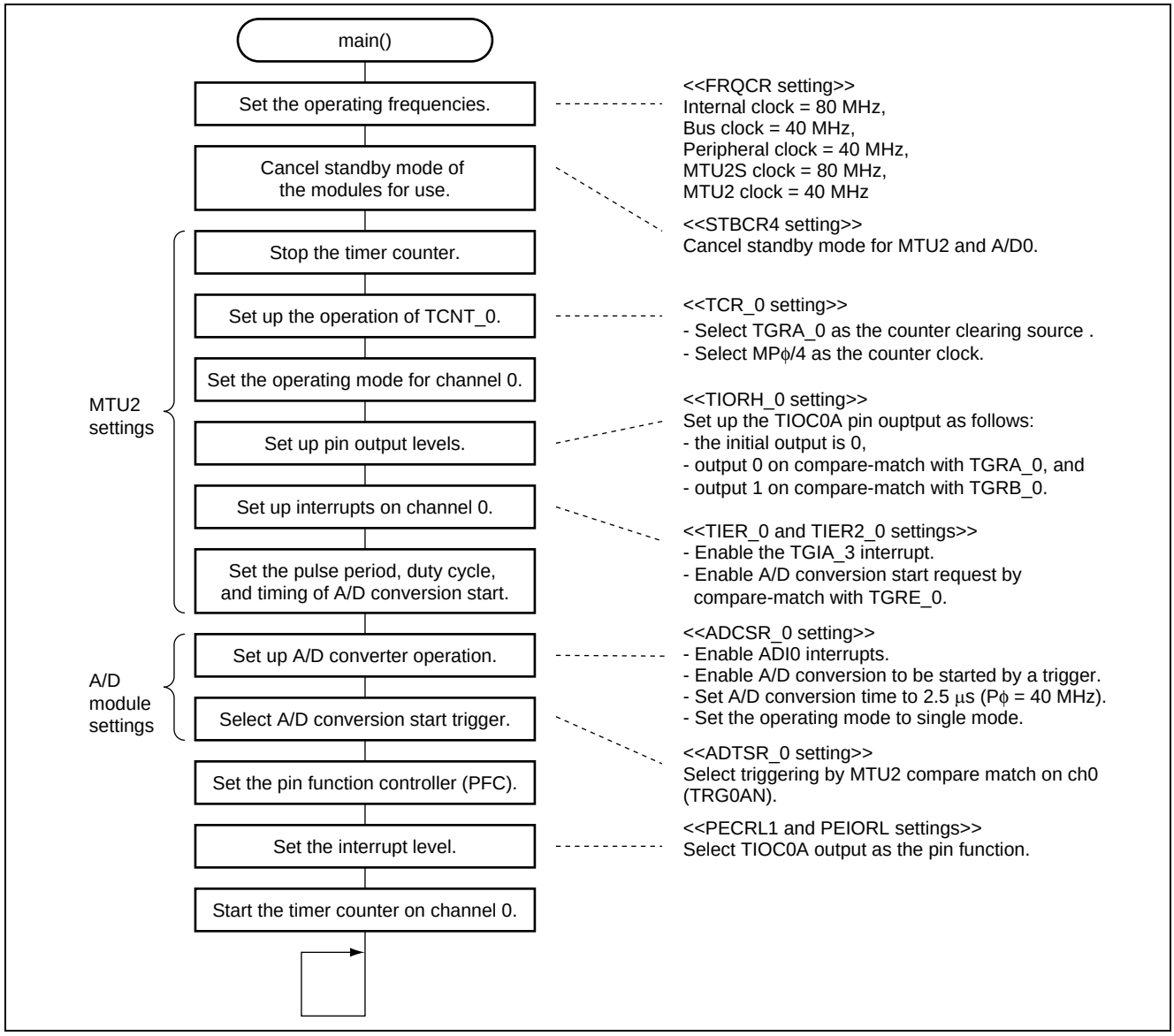
Table 4 describes the arguments used in this sample task.

Table 4 Description of Arguments

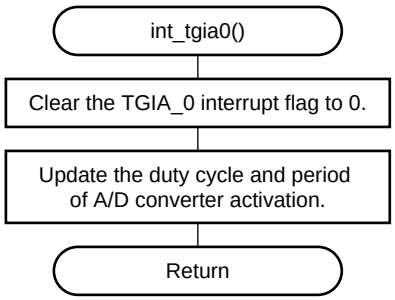
Label	Description	Used in
Pul_cyc	Period of PWM waveform (set in TGRA_0)	Main routine, TGRA_0 compare-match interrupt routine
Duty	Duty cycle of PWM waveform (set in TGRB_0)	
Ad_start	A/D conversion start timing (set in TGRE_0)	
Ad_data[0-2]	Storage of A/D conversion results	A/D conversion end interrupt routine
Ad_count	Counter that counts the number of A/D conversion	

5. Flowchart

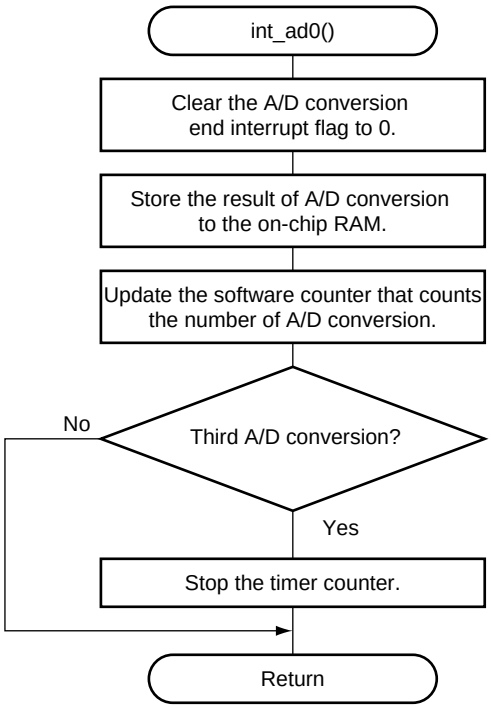
5.1 Main Routine



5.2 TGRA_0 Compare Match Interrupt Routine



5.3 A/D Conversion End Interrupt Routine



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