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April 1st, 2010
Renesas Electronics Corporation

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1. Specifications

Seven-phase PWM output allowing the pulse high width and duty to be varied is performed as shown in figure 1. When operating with on-chip peripheral clock $P\phi = 20.0$ MHz, the output PWM period can be set arbitrarily in the range 100 ns to 3.27 ms.

![Figure 1 Example of PWM Output](image-url)
2. Functions Used

In this sample task, 7-phase PWM output is performed by synchronous operation of MTU ch0 to ch2.

Figure 2 shows a block diagram of the MTU as used in this sample task.

This sample task uses the following MTU functions.

- A function that outputs pulses automatically by hardware without software intervention (output compare)
- A function that clears a counter when a compare match occurs (counter clearing)
- A function that reverses output each time a compare match occurs (toggle output)

![Figure 2 Block Diagram of Synchronous Clearing](image-url)
Table 1 shows the function assignments used in this task. PWM pulses are output by assigning MTU functions as shown in the table.

### Table 1  MTU Function Assignments

<table>
<thead>
<tr>
<th>Pin or Register Name</th>
<th>Function</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIOC0B</td>
<td>Pins</td>
<td>PWM pulse output pins</td>
</tr>
<tr>
<td>TIOC0C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC0D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC1A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC1B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC2A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC2B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSYR</td>
<td>Register</td>
<td>Ch0/1/2 synchronous operation</td>
</tr>
<tr>
<td>TCR_0/1/2</td>
<td>Register</td>
<td>Selection of ch0/1/2 timer counter clearing sources and input clocks</td>
</tr>
<tr>
<td>TGRA_0</td>
<td>Register</td>
<td>PWM period setting</td>
</tr>
<tr>
<td>TGRB_0</td>
<td>Registers</td>
<td>Duty value setting</td>
</tr>
<tr>
<td>TGRD_0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRA_1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRB_1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRA_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRB_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMDR_0/1/2</td>
<td>Register</td>
<td>Operation of ch0/1/2 in PWM Mode 2</td>
</tr>
</tbody>
</table>
### 3. Operation

Figure 3 illustrates the principles of operation of this sample task. Seven-phase PWM output is performed from the ch0/1/2 PWM output pins (TIOC0B/C/D, TIOC1A/B, TIOC2A/B) by SH7046 hardware and software processing as shown in the figure.

![Principles of Operation of PWM Output (7-Phase)
Using Sawtooth Waveform Generation](image)

**Figure 3** Principles of Operation of PWM Output (7-Phase)
Using Sawtooth Waveform Generation
4. Software

(1) Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>pwm_2</td>
<td>PFC and PWM output setting</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label or Register Name</th>
<th>Function Assignment</th>
<th>Data Length</th>
<th>Module</th>
<th>Input/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>pul_cyc0a</td>
<td>Used to set timer value for pulse period</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td></td>
<td>Pulse period is calculated using following equation:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pulse period (ns) = timer value × φ period</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(50.0 ns at 20.0 MHz operation)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty0b</td>
<td>Used to set TIOC pin output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty0c</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty0d</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty1a</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty1b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty2a</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty2b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(3) Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function Assignment</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_STBY.MSTCR2</td>
<td>Module standby mode clearing</td>
<td>H'FFFF861E</td>
<td>H'd2fd</td>
</tr>
<tr>
<td>P_PORTE.PEIORL</td>
<td>Used to set multiplex pins as timer output pins</td>
<td>H'FFFF83B4</td>
<td>H'00fe</td>
</tr>
<tr>
<td>P_PORTE.PECRL2</td>
<td>TIOC0B/C/D, TIOC1A/B, TIOC2A/B</td>
<td>H'FFFF83BA</td>
<td>H'5554</td>
</tr>
<tr>
<td>P_MTU34.TSYR</td>
<td>Synchronous operation set for timer counters 0/1/2</td>
<td>H'FFFF8241</td>
<td>H'O7</td>
</tr>
<tr>
<td>P_MTU0.TCR_0</td>
<td>Used to select TGRA_0 compare match set as timer counter clearing source, and Pφ/1 as input clock</td>
<td>H'FFFF8260</td>
<td>H'O20</td>
</tr>
<tr>
<td>P_MTU1.TCR_1</td>
<td></td>
<td>H'FFFF8280</td>
<td>H'O60</td>
</tr>
<tr>
<td>P_MTU2.TCR_2</td>
<td></td>
<td>H'FFFF82A0</td>
<td>H'O60</td>
</tr>
<tr>
<td>P_MTU0.TGRA_0</td>
<td>PWM period setting</td>
<td>H'FFFF8268</td>
<td>pul_cyc0</td>
</tr>
<tr>
<td>P_MTU0.TGRB_0</td>
<td>Used to set timer counter value causing high output from TIOC0B</td>
<td>H'FFFF826A</td>
<td>pul_duty0b</td>
</tr>
<tr>
<td>P_MTU0.TGRC_0</td>
<td>Used to set timer counter value causing high output from TIOC0C</td>
<td>H'FFFF826C</td>
<td>pul_duty0c</td>
</tr>
<tr>
<td>P_MTU0.TGRD_0</td>
<td>Used to set timer counter value causing high output from TIOC0D</td>
<td>H'FFFF826E</td>
<td>pul_duty0d</td>
</tr>
<tr>
<td>P_MTU1.TGRA_1</td>
<td>Used to set timer counter value causing high output from TIOC1A</td>
<td>H'FFFF8288</td>
<td>pul_duty1a</td>
</tr>
<tr>
<td>P_MTU1.TGRB_1</td>
<td>Used to set timer counter value causing high output from TIOC1B</td>
<td>H'FFFF828A</td>
<td>pul_duty1b</td>
</tr>
<tr>
<td>P_MTU2.TGRA_2</td>
<td>Used to set timer counter value causing high output from TIOC2A</td>
<td>H'FFFF82A8</td>
<td>pul_duty2a</td>
</tr>
<tr>
<td>P_MTU2.TGRB_2</td>
<td>Used to set timer counter value causing high output from TIOC2B</td>
<td>H'FFFF82AA</td>
<td>pul_duty2b</td>
</tr>
<tr>
<td>Register Name</td>
<td>Function Assignment</td>
<td>Address</td>
<td>Set Value</td>
</tr>
<tr>
<td>--------------</td>
<td>----------------------</td>
<td>---------------</td>
<td>-----------</td>
</tr>
<tr>
<td>P_MTU0.TIORH_0</td>
<td>Sets TGRA_0 initial output 0, 0 output on output compare, TGRB_0 initial output 0, 1 output on output compare</td>
<td>H'FFFFF8262</td>
<td>H'20</td>
</tr>
<tr>
<td>P_MTU0.TIORL_0</td>
<td>Sets TGRC_0 initial output 0, 1 output on output compare, TGRD_0 initial output 0, 1 output on output compare</td>
<td>H'FFFFF8263</td>
<td>H'22</td>
</tr>
<tr>
<td>P_MTU1.TIOR_1</td>
<td>Sets TGRA_1 initial output 0, 1 output on output compare, TGRB_1 initial output 0, 1 output on output compare</td>
<td>H'FFFFF8282</td>
<td>H'22</td>
</tr>
<tr>
<td>P_MTU1.TIOR_2</td>
<td>Sets TGRA_2 initial output 0, 1 output on output compare, TGRB_2 initial output 0, 1 output on output compare</td>
<td>H'FFFFF82A2</td>
<td>H'22</td>
</tr>
<tr>
<td>P_MTU0.TMDR_0</td>
<td>Used to set PWM Mode 2 as operating mode of each channel</td>
<td>H'FFFFF8261</td>
<td>H'c3</td>
</tr>
<tr>
<td>P_MTU1.TMDR_1</td>
<td></td>
<td>H'FFFFF8281</td>
<td>H'c3</td>
</tr>
<tr>
<td>P_MTU2.TMDR_2</td>
<td></td>
<td>H'FFFFF82A1</td>
<td>H'c3</td>
</tr>
</tbody>
</table>

(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.
5. Flowcharts

(1) Main routine

```plaintext
pwm_2

MSTCR2 ← H'2d2fd

PEIORL ← H'00fe
PECRL2 ← H'5654

TCR_0 ← H'20
TCR_1 ← H'80
TCR_2 ← H'60

TGRA_0 ← pul_cyc0

TGRB_0 ← pul_duty0b
TGRC_0 ← pul_duty0c
TGRD_0 ← pul_duty0d
TGRA_1 ← pul_duty1a
TGRB_1 ← pul_duty1b
TGRA_2 ← pul_duty2a
TGRB_2 ← pul_duty2b

TIORH_0 ← H'20
TIORL_0 ← H'22
TIOR_1 ← H'22
TIOR_2 ← H'22

TMDR_0 ← H'c3
TMDR_1 ← H'c3
TMDR_2 ← H'c3

TSYR ← H'07

TSTR ← H'07
```

- Clear MTU module standby mode
- Set TIOC0B/C/D, TIOC1A/B, TIOC2A/B as outputs in P_PORTE.PECRL2
- Set TGRA_0 as counter clearing source in P_MTU0.TCR_0, set synchronous clearing in P_MTU1.TCR_1, P_MTU2.TCR_2
- Set pulse period in P_MTU0.TGRA_0
- Set duty values in P_MTU0.TGRB/C/D_0, P_MTU1.TGRA/B_1, P_MTU2.TGRA/B_2
- SET wave output values in TIOR
- Set PWM Mode 2 in TMDR_0/1/2
- Set synchronous operation for ch0/1/2
- Enable ch0/1/2 count operation with P_MTU34.TSTR
6. Program Listing

/****************************************************************************
/* INCLUDE FILE */
****************************************************************************/
#include<machine.h>
#include"iodefine_7046.h"
****************************************************************************/
/* PROTOTYPE */
****************************************************************************/
void pwm_2(void);
****************************************************************************/
/* RAM ALLOCATION */
****************************************************************************/
#define pul_cyc0 (*(unsigned short *)0xffffd000)
#define pul_duty0b (*(unsigned short *)0xffffd002)
#define pul_duty0c (*(unsigned short *)0xffffd004)
#define pul_duty0d (*(unsigned short *)0xffffd006)
#define pul_duty1a (*(unsigned short *)0xffffd008)
#define pul_duty1b (*(unsigned short *)0xffffd00a)
#define pul_duty2a (*(unsigned short *)0xffffd00c)
#define pul_duty2b (*(unsigned short *)0xffffd00e)
/*****************************************************************************/
/* MAIN PROGRAM */
/*****************************************************************************/
void pwm_2(void)
{
    P_STBY.MSTCR2.WORD =0xd2fd; /* Clear module standby mode */
    P_PORTE.PEIORL.WORD = 0x00fe; /* TIOC0B/C/D,TIOC1A/B,TIOC2A/B output */
    P_PORTE.PECRL2.WORD = 0x5554;
    P_MTU0.TCR_0.BYTE = 0x20; /* Counter clear by TGRA_0 */
    P_MTU0.TIORH_0.BYTE = 0x20;
    P_MTU0.TIORL_0.BYTE = 0x22;
    P_MTU0.TCNT_0 = 0x0000;
    P_MTU0.TGRA_0 = pul_cyc0; /* Set general register */
    P_MTU0.TGRB_0 = pul_duty0b;
    P_MTU0.TGRC_0 = pul_duty0c;
    P_MTU0.TGRD_0 = pul_duty0d;
    P_MTU0.TMDR_0.BYTE = 0xc3; /* PWM mode2 */
    P_MTU1.TCR_1.BYTE = 0x60; /* Counter clear by TGRA_0 */
    P_MTU1.TIOR_1.BYTE = 0x22;
    P_MTU1.TCNT_1 = 0x0000;
    P_MTU1.TGRA_1 = pul_duty1a; /* Set general register */
    P_MTU1.TGRB_1 = pul_duty1b;
    P_MTU1.TMDR_1.BYTE = 0xc3; /* PWM mode2 */
    P_MTU2.TCR_2.BYTE =0x60; /* Counter clear by TGRA_0 */
    P_MTU2.TIOR_2.BYTE = 0x22;
    P_MTU2.TCNT_2 = 0x0000;
    P_MTU2.TGRA_2 = pul_duty2a; /* Set general register */
    P_MTU2.TGRB_2 = pul_duty2b;
    P_MTU2.TMDR_2.BYTE = 0xc3; /* PWM mode2 */
}
P_MTU34.TSYR.BYTE = 0x07;
P_MTU34.TSTR.BYTE = 0x07;  /* Start timer counter */
while(1);
}
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