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April 1st, 2010
Renesas Electronics Corporation

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SH7046 Group
PWM 4-Phase Output

1. Specifications

Using MTU PWM mode 1, 4-phase PWM output is performed based on a set duty value and period.

In PWM mode 1, an arbitrary period can be set for each channel. Two outputs are possible for each of ch0, ch3, and ch4, and one output for each of ch1 and ch2. Thus for ch0, ch3, and ch4, waveforms can be generated with a different high width within the same period.

A duty of 0% to 100% can be set with a 1/65,535 resolution.

![Diagram of PWM Output](image-url)
2. Functions Used

In this sample task, 4-phase PWM output is performed using MTU ch1 to ch3.

In PWM mode 1, PWM output is generated with TGRA paired with TGRB, and TGRC paired with TGRD. By using ch0 to ch4, a maximum of 8-phase PWM output is possible.

Figure 2 shows a block diagram of the MTU as used in this sample task.

![Block Diagram of MTU/ch1, ch2, ch3]
Table 1 shows the function assignments used in this sample task. PWM pulses are output by assigning MTU functions as shown in the table.

**Table 1 Function Assignments**

<table>
<thead>
<tr>
<th>Pin or Register Name</th>
<th>Function</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIOC1A</td>
<td>Pins</td>
<td>PWM pulse output pins</td>
</tr>
<tr>
<td>TIOC2A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC3A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC3C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCR_1</td>
<td>Registers</td>
<td>Selection of ch1 to ch3 timer counter clearing sources and input clocks</td>
</tr>
<tr>
<td>TCR_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCR_3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMDR_1</td>
<td>Registers</td>
<td>Operation of ch1 to ch3 in PWM mode 1</td>
</tr>
<tr>
<td>TMDR_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMDR_3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRA_1</td>
<td>Registers</td>
<td>PWM period setting</td>
</tr>
<tr>
<td>TGRA_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRA_3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRB_1</td>
<td>Registers</td>
<td>Duty value setting</td>
</tr>
<tr>
<td>TGRB_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRB_3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRC_3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRD_3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3. Operation

Figure 3 illustrates the principles of operation of this sample task. Four-phase PWM output is performed from the ch1 to ch3 PWM output pins (TIOC1A, TIOC2A, TIOC3A/C) by SH7046 hardware and software processing as shown in the figure.

![Figure 3 Principles of Operation of PWM Waveforms](image-url)
## 4. Software

### (1) Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>pwm_1</td>
<td>PFC and PWM output setting</td>
</tr>
</tbody>
</table>

### (2) Arguments

<table>
<thead>
<tr>
<th>Label or Register Name</th>
<th>Function Assignment</th>
<th>Data Length</th>
<th>Module</th>
<th>Input/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>pul_cyc1</td>
<td>Used to set timer value for pulse period</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>pul_cyc2</td>
<td>Pulse period is calculated using following equation:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_cyc3</td>
<td>Pulse period (ns) = timer value × φ period</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(50.0 ns at 20.0 MHz operation)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty1b</td>
<td>Used to set TIOC pin output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty2b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty3b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty3c</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty3d</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### (3) Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function Assignment</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_STBY.MSTCR2</td>
<td>MTU module standby mode clearing</td>
<td>H'FFFF861E</td>
<td>H'd2fd</td>
</tr>
<tr>
<td>P_PORTE.PEIORL</td>
<td>Multiplex pins set as timer output pins TIOC1A, TIOC2A, TIOC3A, TIOC3C</td>
<td>H'FFFF83B4</td>
<td>H'0550</td>
</tr>
<tr>
<td>P_PORTE.PECRL1</td>
<td></td>
<td>H'FFFF83B8</td>
<td>H'0011</td>
</tr>
<tr>
<td>P_PORTE.PECRL2</td>
<td></td>
<td>H'FFFF83BA</td>
<td>H'1100</td>
</tr>
<tr>
<td>P_MTU1.TCR_1</td>
<td>Timer counter clearing sources cleared by</td>
<td>H'FFFF8280</td>
<td>H'20</td>
</tr>
<tr>
<td>P_MTU1.TGRA_1</td>
<td>Channel 1 PWM period setting</td>
<td>H'FFFF8288</td>
<td>pul_cyc1</td>
</tr>
<tr>
<td>P_MTU1.TGRB_1</td>
<td>Used to set timer counter value causing high output from TIOC1A</td>
<td>H'FFFF828A</td>
<td>pul_duty1b</td>
</tr>
<tr>
<td>P_MTU2.TGRA_2</td>
<td>Channel 2 PWM period setting</td>
<td>H'FFFF8282A</td>
<td>pul_cyc2</td>
</tr>
<tr>
<td>P_MTU2.TGRB_2</td>
<td>Used to set timer counter value causing high output from TIOC2A</td>
<td>H'FFFF82AA</td>
<td>pul_duty2b</td>
</tr>
<tr>
<td>P_MTU34.TGRA_3</td>
<td>Channel 3 PWM period setting</td>
<td>H'FFFF8218</td>
<td>pul_cyc3</td>
</tr>
<tr>
<td>P_MTU34.TGRB_3</td>
<td>Used to set timer counter value causing high output from TIOC3A</td>
<td>H'FFFF821A</td>
<td>pul_duty3b</td>
</tr>
<tr>
<td>P_MTU34.TGRC_3</td>
<td>Used to set timer counter value causing low output from TIOC3C</td>
<td>H'FFFF8224</td>
<td>pul_duty3c</td>
</tr>
<tr>
<td>P_MTU34.TGRD_3</td>
<td>Used to set timer counter value causing high output from TIOC3C</td>
<td>H'FFFF8226</td>
<td>pul_duty3d</td>
</tr>
<tr>
<td>Register Name</td>
<td>Function Assignment</td>
<td>Address</td>
<td>Set Value</td>
</tr>
<tr>
<td>---------------</td>
<td>-------------------------------------------------------------------------------------</td>
<td>-------------</td>
<td>-----------</td>
</tr>
<tr>
<td>P_MTU1.TIOR_1</td>
<td>Sets TGRA_1 initial output 0, 0 output on output compare, TGRB_1 initial output 0, 1 output on output compare</td>
<td>H’FFFF8282</td>
<td>H’02</td>
</tr>
<tr>
<td>P_MTU2.TIOR_2</td>
<td>Sets TGRA_2 initial output 0, 0 output on output compare, TGRB_2 initial output 0, 1 output on output compare</td>
<td>H’FFFF82A2</td>
<td>H’02</td>
</tr>
<tr>
<td>P_MTU34.TIORH_3</td>
<td>Sets TGRA_3 initial output 0, 0 output on output compare, TGRB_3 initial output 0, 1 output on output compare</td>
<td>H’FFFF8204</td>
<td>H’02</td>
</tr>
<tr>
<td>P_MTU34.TIORL_3</td>
<td>Sets TGRC_3 initial output 0, 0 output on output compare, TGRD_3 initial output 0, 1 output on output compare</td>
<td>H’FFFF8205</td>
<td>H’21</td>
</tr>
<tr>
<td>P_MTU1.TMDR_1</td>
<td>Used to set PWM mode 1 as operating mode</td>
<td>H’FFFF8281</td>
<td>H’c2</td>
</tr>
<tr>
<td>P_MTU2.TMDR_2</td>
<td></td>
<td>H’FFFF82A1</td>
<td>H’c2</td>
</tr>
<tr>
<td>P_MTU34.TMDR_3</td>
<td></td>
<td>H’FFFF8202</td>
<td>H’c2</td>
</tr>
</tbody>
</table>

(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.
5. Flowcharts

(1) Main routine

```
pwm_1

MSTCR2 ← H'd2fd

PEIORL ← H'00550
PECRL1 ← H'0011
PECRL2 ← H'11100

TCR_1 ← H'20
TCR_2 ← H'20
TCR_3 ← H'20

Set TGRA_1/2/3 as TCR counter clearing sources

TGRA_1 ← pul_cyc1
TGRA_2 ← pul_cyc2
TGRA_3 ← pul_cyc3

Set pulse periods in P_MTU1.TGRA_1,
P_MTU2.TGRA_2, P_MTU34.TGRA_3

TGRB_1 ← pul_duty1b
TGRB_2 ← pul_duty2b
TGRB_3 ← pul_duty3b
TGRB_3 ← pul_duty3c
TGRD_3 ← pul_duty3d

Set duty values in P_MTU1.TGRB_1,
P_MTU2.TGRB_2, P_MTU34.TGRB_3,
P_MTU34.TGRB_3, P_MTU34.TGRD_3

TIOR_1 ← H'02
TIOR_2 ← H'02
TIORL_3 ← H'21
TIORH_3 ← H'02

Set waveform output values in TIOR

TMDR_1 ← H'c2
TMDR_2 ← H'c2
TMDR_3 ← H'c2

Set PWM mode 1 in TMDR_1/2/3

TSTR ← H'46

Enable ch1/2/3 count operation with P_MTU34.TSTR
```

Clear MTU module standby mode

Perform TIOC1A, 2A, 3A, 3C output settings in P_PORTEP.PECRL1/2
6. Program Listing

/******************************************************************************/
/* INCLUDE FILE */
/******************************************************************************/
#include<machine.h>
#include"iodefine_7046.h"
/*******************************************************************************/
/* PROTOTYPE */
/******************************************************************************/
void pwm_1(void);
/*******************************************************************************/
/* RAM ALLOCATION */
/******************************************************************************/
#define pul_cyc1 (*(unsigned short *)0xffffd000)
#define pul_duty1b (*(unsigned short *)0xffffd002)
#define pul_cyc2 (*(unsigned short *)0xffffd004)
#define pul_duty2b (*(unsigned short *)0xffffd006)
#define pul_cyc3 (*(unsigned short *)0xffffd008)
#define pul_duty3b (*(unsigned short *)0xffffd00a)
#define pul_duty3c (*(unsigned short *)0xffffd00c)
#define pul_duty3d (*(unsigned short *)0xffffd00e)
/*******************************************************************************/
/* MAIN PROGRAM */
/******************************************************************************/
void pwm_1(void)
{
    P_STBY.MSTCR2.WORD = 0xd2fd; /* Clear module standby mode */
P_PORTE.PEIORL.WORD = 0x0550; /* TIOC1A/2A/3A/3C = output */
P_PORTE.PECRL1.WORD = 0x0011;
P_PORTE.PECRL2.WORD = 0x1100;

    P_MTU1.TCR_1.BYTE = 0x20; /* Counter clear by TGRA */
P_MTU1.TGRA_1 = pul_cyc1; /* set period */
P_MTU1.TGRB_1 = pul_duty1b; /* set duty */
P_MTU1.TIOR_1.BYTE = 0x02;
P_MTU1.TMDR_1.BYTE = 0xc2; /* PWM model */
P_MTU1.TCNT_1 = 0x0000;

    P_MTU2.TCR_2.BYTE = 0x20;
P_MTU2.TGRA_2 = pul_cyc2;
P_MTU2.TGRB_2 = pul_duty2b;
P_MTU2.TIOR_2.BYTE = 0x02;
P_MTU2.TMDR_2.BYTE = 0xc2;
P_MTU2.TCNT_2 = 0x0000;

    P_MTU34.TCR_3.BYTE = 0x20;
P_MTU34.TGRA_3 = pul_cyc3;
P_MTU34.TGRB_3 = pul_duty3b;
P_MTU34.TGRC_3 = pul_duty3c;
P_MTU34.TGRD_3 = pul_duty3d;
P_MTU34.TIORL_3.BYTE = 0x21;
P_MTU34.TIORH_3.BYTE = 0x02;
P_MTU34.TMDR_3.BYTE = 0xc2;
P_MTU34.TCNT_3 = 0x0000;

P_MTU34.TSTR.BYTE = 0x46; /* Timer counter start */
while(1);
}
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