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April 1\(^{st}\), 2010
Renesas Electronics Corporation

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1. Specifications

Positive-phase and negative-phase 3-phase pulse (duty pulse) output is performed that allows the pulse high width and duty to be varied, as shown in figure 1.

When operating with on-chip peripheral clock $P\phi = 20.0$ MHz, the output pulse period can be set arbitrarily in the range 100.0 ns to 3.27 ms.

![Positive-Phase/Negative-Phase PWM 3-Phase Output Waveforms](image)

**Figure 1** Positive-Phase/Negative-Phase PWM 3-Phase Output Waveforms
2. Functions Used

In this sample task, MTU ch3 and ch4 are used in combination, and 3-phase PWM waveform output is performed with one common transition point in the relationship between the positive phase and negative phase.

In reset-synchronized PWM mode, PWM waveforms are generated using buffer operation, with TGRA and TGRC operating as a pair, and TRGB and TGRD operating as a pair.

Figure 2 shows a block diagram of the MTU as used in this sample task.

![Block Diagram of MTU/ch3, ch4](image)

Table 1 shows the function assignments used in this task. PWM pulses are output by assigning MTU functions as shown in the table.

### Table 1 Function Assignments

<table>
<thead>
<tr>
<th>Pin or Register Name</th>
<th>Function</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIOC3B</td>
<td>Pin</td>
<td>PWM output 1</td>
</tr>
<tr>
<td>TIOC3D</td>
<td>Pin</td>
<td>Negative-phase waveform of PWM output 1</td>
</tr>
<tr>
<td>TIOC4A</td>
<td>Pin</td>
<td>PWM output 2</td>
</tr>
<tr>
<td>TIOC4B</td>
<td>Pin</td>
<td>PWM output 3</td>
</tr>
<tr>
<td>TIOC4C</td>
<td>Pin</td>
<td>Negative-phase waveform of PWM output 2</td>
</tr>
<tr>
<td>TIOC4D</td>
<td>Pin</td>
<td>Negative-phase waveform of PWM output 3</td>
</tr>
<tr>
<td>TCR_3</td>
<td>Register</td>
<td>Selection of ch3 timer counter clearing source and input clock</td>
</tr>
<tr>
<td>TMDR_3</td>
<td>Register</td>
<td>Ch3 set to operate in reset-synchronized PWM mode</td>
</tr>
<tr>
<td>TGRA_3</td>
<td>Register</td>
<td>PWM period setting</td>
</tr>
<tr>
<td>TGRB_3</td>
<td>Registers</td>
<td>Duty value setting</td>
</tr>
<tr>
<td>TGRA_4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGRB_4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3. Operation

Figure 3 illustrates the principles of operation of this sample task. Three-phase PWM waveforms are output from the PWM output pins (TIOC3B/D, TIOC4A/B/C/D) by SH7046 hardware and software processing as shown in the figure.

![Diagram showing the principles of operation of Reset-Synchronized PWM Waveforms](image)

**Figure 3** Principles of Operation of Reset-Synchronized PWM Waveforms
4. Software

(1) Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>rst_pwm</td>
<td>PFC and PWM output setting</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label or Register Name</th>
<th>Function</th>
<th>Data Length</th>
<th>Module</th>
<th>Input/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>pul_cyc1</td>
<td>Used to set timer value for pulse period</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td></td>
<td>Pulse period is calculated using following equation: Pulse period (ns) = timer value × φ/p</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(50.0 ns at 20.0 MHz operation)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty3b</td>
<td>Used to set TIOC pin output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty4a</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pul_duty4b</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(3) Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_PORTE.PEIORL</td>
<td>Used to set multiplex insert as timer output pins</td>
<td>H'FFFF83B4</td>
<td>H'fa00</td>
</tr>
<tr>
<td>P_PORTE.PECRL1</td>
<td>TIOC3B/D, TIOC4A/B/C/D</td>
<td>H'FFFF83B8</td>
<td>H'5544</td>
</tr>
<tr>
<td>P_MTU34.TCR_3</td>
<td>Used to select TGRA_3 compare match as timer counter clearing source, and Pφ/1 as input clock</td>
<td>H'FFFF8200</td>
<td>H'20</td>
</tr>
<tr>
<td>P_MTU34.TOCR</td>
<td>Enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output level setting</td>
<td>H'FFFF820B</td>
<td>H'43</td>
</tr>
<tr>
<td>P_MTU34.TGRA_3</td>
<td>PWM period setting</td>
<td>H'FFFF8218</td>
<td>pul_cyc1</td>
</tr>
<tr>
<td>P_MTU34.TGRB_3</td>
<td>Used to set timer counter value for toggle output from TIOC3B/D</td>
<td>H'FFFF821A</td>
<td>pul_duty3b</td>
</tr>
<tr>
<td>P_MTU34.TGRA_4</td>
<td>Used to set timer counter value for toggle output from TIOC4A/C</td>
<td>H'FFFF821C</td>
<td>pul_duty4a</td>
</tr>
<tr>
<td>P_MTU34.TGRB_4</td>
<td>Used to set timer counter value for toggle output from TIOC4B/D</td>
<td>H'FFFF821E</td>
<td>pul_duty4b</td>
</tr>
<tr>
<td>P_MTU34.TOER</td>
<td>Sets enabling of reset-synchronized PWM output</td>
<td>H'FFFF821E</td>
<td>H'ff</td>
</tr>
<tr>
<td>P_MTU34.TMDR_3</td>
<td>Sets reset-synchronized PWM mode</td>
<td>H'FFFF8202</td>
<td>H'c8</td>
</tr>
<tr>
<td>P_STBY.MSTCR2</td>
<td>Module standby mode clearing</td>
<td>H'FFFF861E</td>
<td>H'd2fd</td>
</tr>
</tbody>
</table>

(4) RAM Used

This sample application does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.
5. Flowcharts

(1) Main routine

```
rst_pwm

MSTCR2 ← H'd2fd

PEIORL ← H'fa00
PECRL1 ← H'5544

TSTR ← H'00

TCR_3 ← H'20

TCNT_3 ← H'0000
TCNT_4 ← H'0000

TGRA_3 ← pul_cyc1

TGRB_3 ← pul_duty3b
TGRA_4 ← pul_duty4a
TGRB_4 ← pul_duty4b

TOCR ← H'43

TMDR_3 ← H'c8

TOER ← H'ff

TSTR ← H'40
```

- Clear MTU module standby mode
- Set TIOC3B/D, TIOC4A/B/C/D pins as outputs in P_PORTE PECRL1
- Stop timer counter
- Set TGRA_3 as counter clearing source in TCR
- Clear timer counters 3/4
- Set pulse period in P_MTU34.TGRA_3
- Set duty values in P_MTU34.TGRB_3, TGRA/B_4
- Set enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output level, in P_MTU34.TOCR
- Set P_MTU34.TMDR to reset-synchronized PWM mode
- Enable reset-synchronized PWM output with P_MTU34.TOER
- Enable ch3 count operation with P_MTU34.TSTR
6. Program Listing

/*****************************/
/* INCLUDE FILE */
/*****************************/
#include<machine.h>
#include"iodefine_7046.h"
/*****************************/
/* PROTOTYPE */
/*****************************/
void rst_pwm(void);
/*****************************/
/* RAM ALLOCATION */
/*****************************/
#define pul_cyc1 (*(unsigned short *)0xffffd000)
#define pul_duty3b (*(unsigned short *)0xffffd002)
#define pul_duty4a (*(unsigned short *)0xffffd004)
#define pul_duty4b (*(unsigned short *)0xffffd006)
/*****************************/
/* MAIN PROGRAM */
/*****************************/
void rst_pwm(void)
{
    P_STBY.MSTCR2.WORD = 0xd2fd; /* Clear module standby mode */
    P_PORTE.PEIORL.WORD = 0xfa00; /* TIOC3B/D,TIOC4A/B/C/D output */
    P_PORTE.PECRL1.WORD = 0x5544;
    P_MTU34.TSTR.BYTE = 0x00;
    P_MTU34.TCR_3.BYTE = 0x20; /* Counter clear by TGRA_3 */
    P_MTU34.TCNT_3 = 0x0000; /* Clear timer counter3 */
    P_MTU34.TCNT_4 = 0x0000; /* Clear timer counter4 */
    P_MTU34.TGRA_3 = pul_cyc1; /* Set period */
    P_MTU34.TGRB_3 = pul_duty3b; /* Set duty */
    P_MTU34.TGRA_4 = pul_duty4a;
    P_MTU34.TGRB_4 = pul_duty4b;
    P_MTU34.TOCR.BYTE = 0x43; /* Set timer output control register */
    P_MTU34.TMDR_3.BYTE = 0xc8; /* Reset synchronized PWM mode */
    P_MTU34.TOER.BYTE = 0xff; /* Timer output enable */
    P_MTU34.TSTR = 0x40; /* Start timer counter */
    while(1);
}
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