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Renesas Electronics Corporation

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SH7046 Group

Positive-Phase/Negative Phase PWM 3-Phase Output

1. Specifications

Positive-phase and negative-phase 3-phase pulse (duty pulse) output is performed that allows the pulse high width and duty to be varied, as shown in figure 1.

When operating with on-chip peripheral clock Pϕ = 20.0 MHz, the output pulse period can be set arbitrarily in the range 100.0 ns to 3.27 ms.

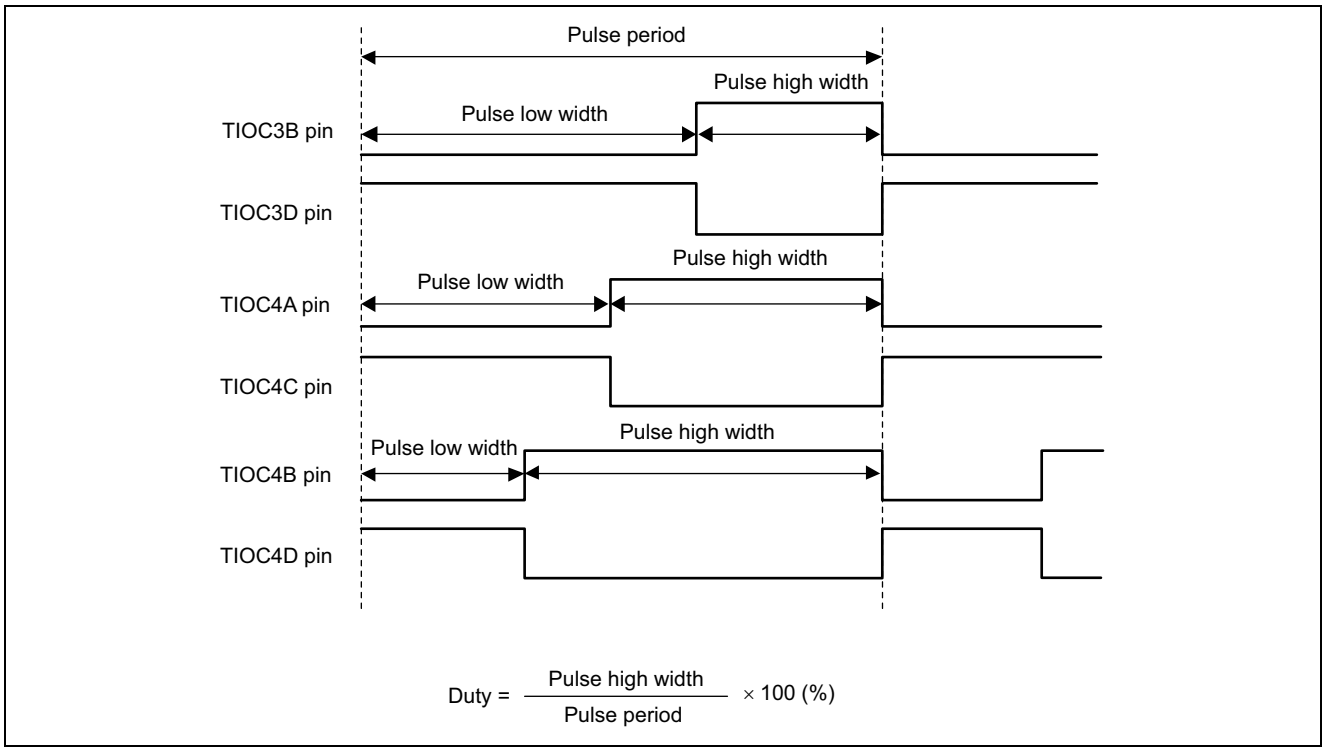


Figure 1 Positive-Phase/Negative-Phase PWM 3-Phase Output Waveforms

2. Functions Used

In this sample task, MTU ch3 and ch4 are used in combination, and 3-phase PWM waveform output is performed with one common transition point in the relationship between the positive phase and negative phase.

In reset-synchronized PWM mode, PWM waveforms are generated using buffer operation, with TGRA and TGRC operating as a pair, and TRGB and TGRD operating as a pair.

Figure 2 shows a block diagram of the MTU as used in this sample task.

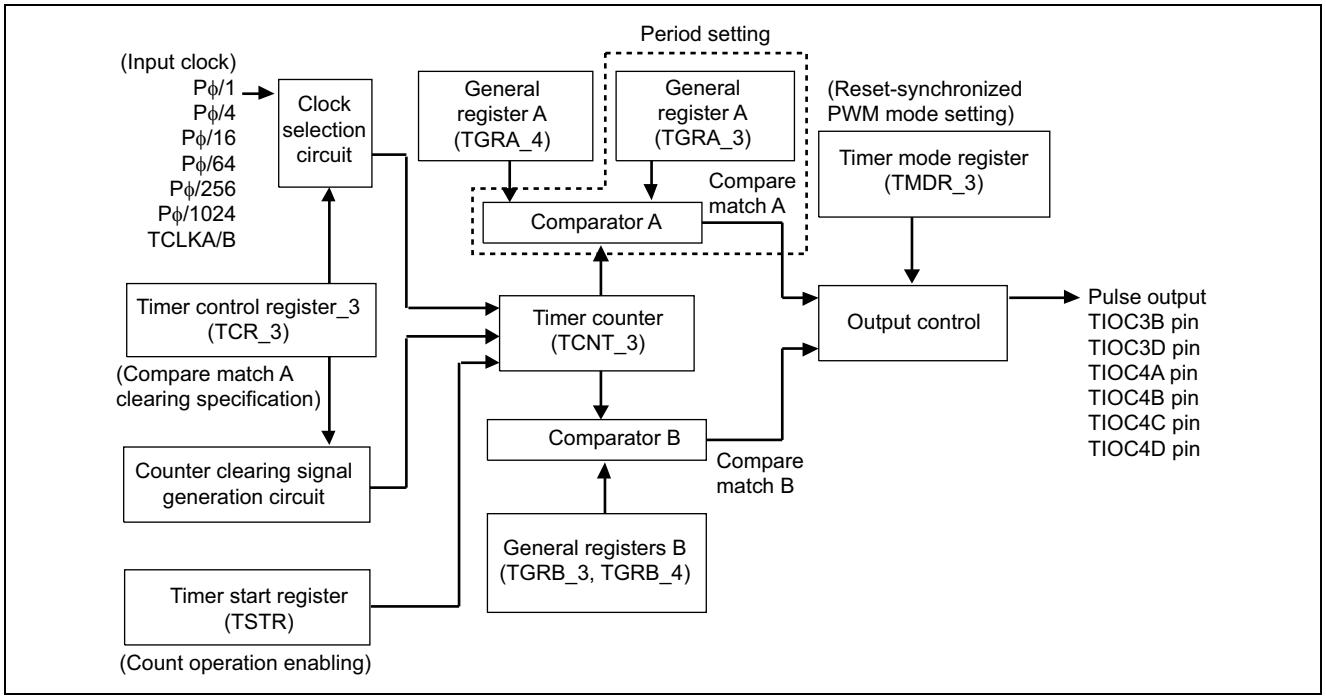


Figure 2 Block Diagram of MTU/ch3, ch4

Table 1 shows the function assignments used in this task. PWM pulses are output by assigning MTU functions as shown in the table.

Table 1 Function Assignments

Pin or Register Name	Function	Function Assignment
TIOC3B	Pin	PWM output 1
TIOC3D	Pin	Negative-phase waveform of PWM output 1
TIOC4A	Pin	PWM output 2
TIOC4B	Pin	PWM output 3
TIOC4C	Pin	Negative-phase waveform of PWM output 2
TIOC4D	Pin	Negative-phase waveform of PWM output 3
TCR_3	Register	Selection of ch3 timer counter clearing source and input clock
TMDR_3	Register	Ch3 set to operate in reset-synchronized PWM mode
TGRA_3	Register	PWM period setting
TGRB_3 TGRA_4 TGRB_4	Registers	Duty value setting

3. Operation

Figure 3 illustrates the principles of operation of this sample task. Three-phase PWM waveforms are output from the PWM output pins (TIOC3B/D, TIOC4A/B/C/D) by SH7046 hardware and software processing as shown in the figure.

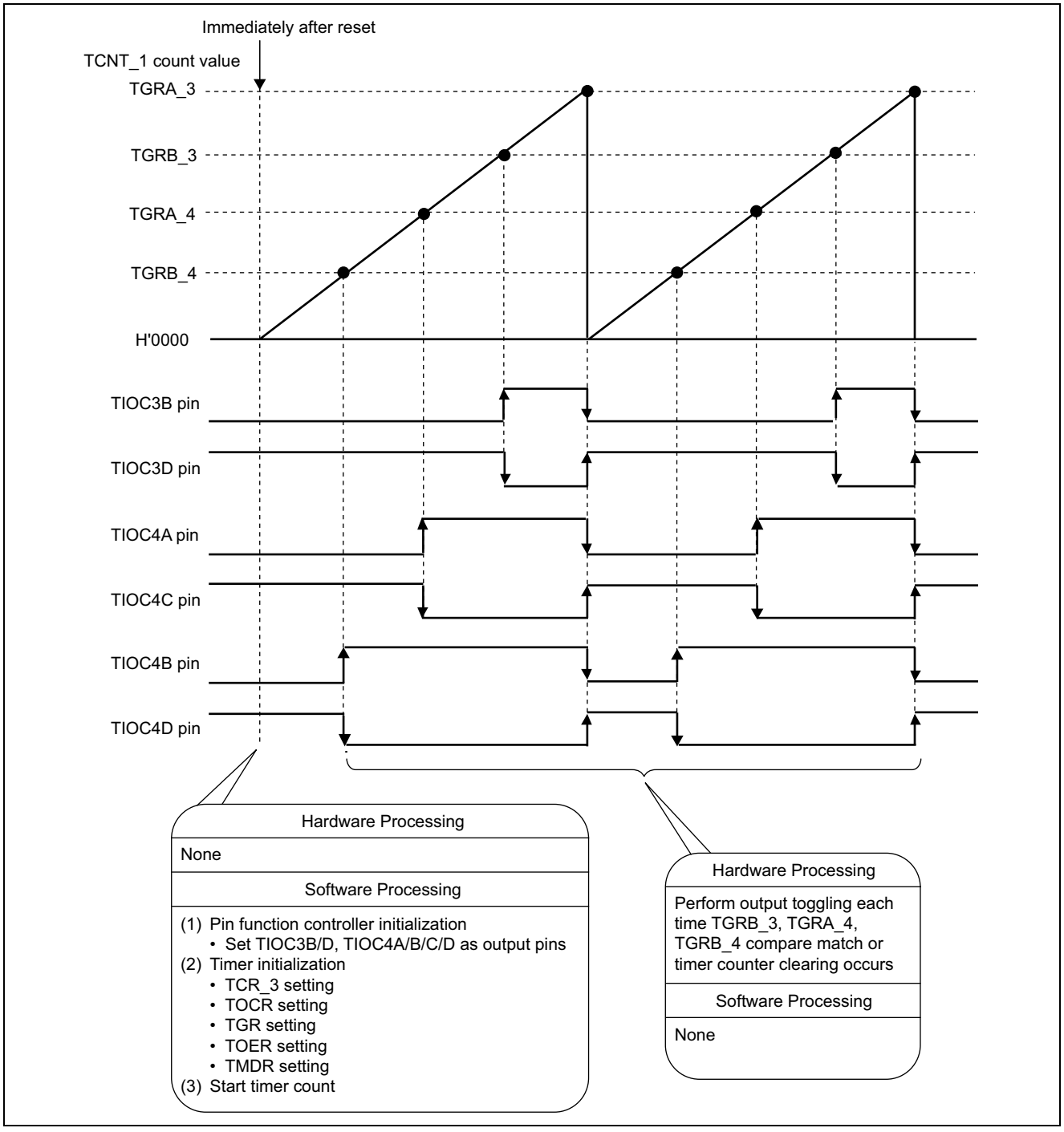


Figure 3 Principles of Operation of Reset-Synchronized PWM Waveforms

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	rst_pwm	PFC and PWM output setting

(2) Arguments

Label or Register Name	Function	Data Length	Module	Input/ Output
pul_cyc1	Used to set timer value for pulse period Pulse period is calculated using following equation: Pulse period (ns) = timer value × ϕ period (50.0 ns at 20.0 MHz operation)	1 word	Main routine	Input
pul_duty3b pul_duty4a pul_duty4b	Used to set TIOC pin output waveform transition timing			

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_PORTE.PEIORL P_PORTE.PECRL1	Used to set multiplex insert as timer output pins TIOC3B/D, TIOC4A/B/C/D	H'FFFF83B4 H'FFFF83B8	H'fa00 H'5544
P_MTU34.TCR_3	Used to select TGRA_3 compare match as timer counter clearing source, and Pϕ/1 as input clock	H'FFFF8200	H'20
P_MTU34.TOCR	Enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output level setting	H'FFFF820B	H'43
P_MTU34.TGRA_3	PWM period setting	H'FFFF8218	pul_cyc1
P_MTU34.TGRB_3	Used to set timer counter value for toggle output from TIOC3B/D	H'FFFF821A	pul_duty3b
P_MTU34.TGRA_4	Used to set timer counter value for toggle output from TIOC4A/C	H'FFFF821C	pul_duty4a
P_MTU34.TGRB_4	Used to set timer counter value for toggle output from TIOC4B/D	H'FFFF821E	pul_duty4b
P_MTU34.TOER	Sets enabling of reset-synchronized PWM output	H'FFFF821E	H'ff
P_MTU34.TMDR_3	Sets reset-synchronized PWM mode	H'FFFF8202	H'c8
P_STBY.MSTCR2	Module standby mode clearing	H'FFFF861E	H'd2fd

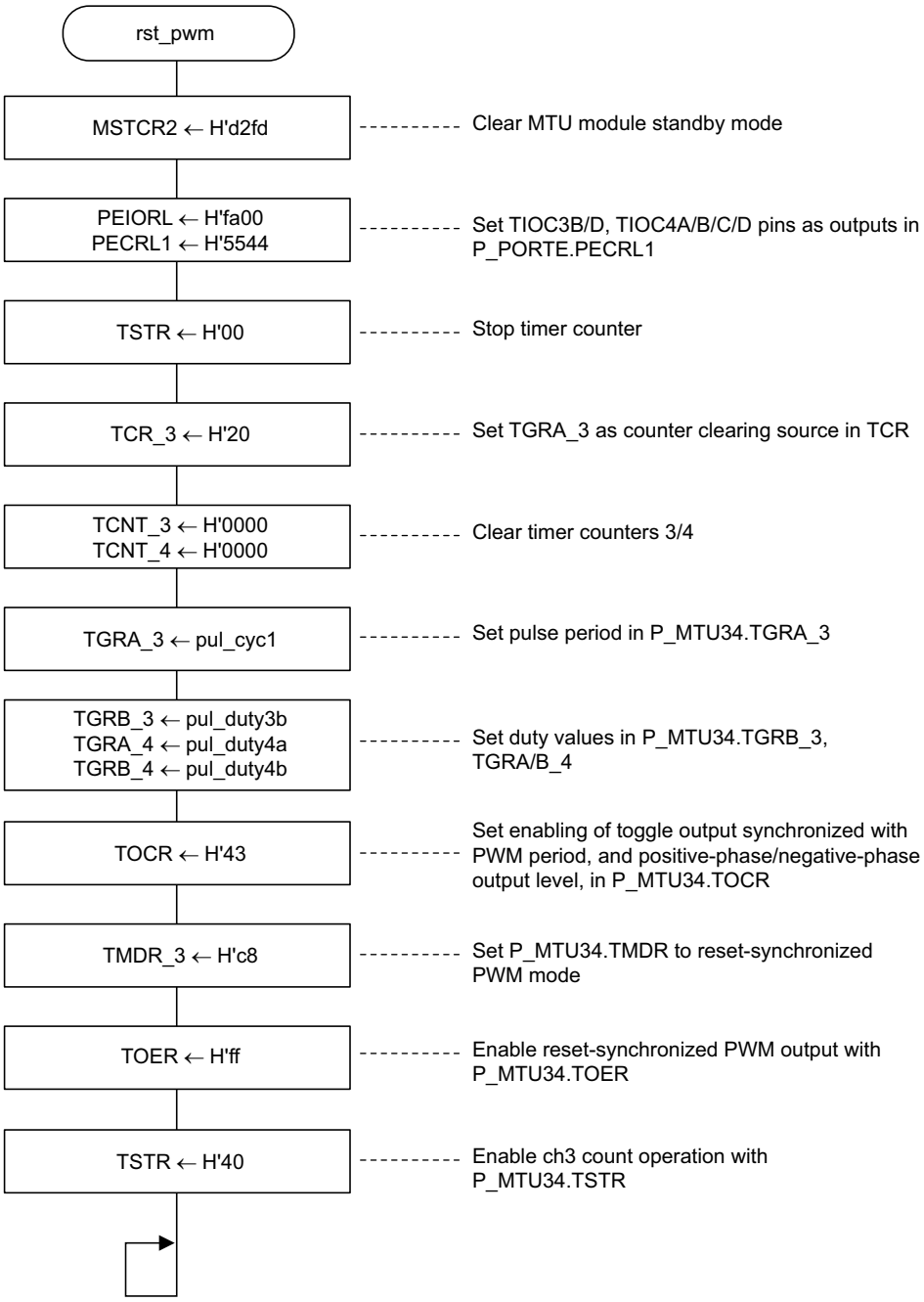
(4) RAM Used

This sample application does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```
/************************************************************************/
/*                              INCLUDE FILE                            */
/************************************************************************/
#include<machine.h>
#include"iodefine_7046.h"
/************************************************************************/
/*                              PROTOTYPE                               */
/************************************************************************/
void rst_pwm(void);
/************************************************************************/
/*                            RAM ALLOCATION                            */
/************************************************************************/
#define pul_cyc1  (*(unsigned short *)0xffffd000)
#define pul_duty3b  (*(unsigned short *)0xffffd002)
#define pul_duty4a  (*(unsigned short *)0xffffd004)
#define pul_duty4b  (*(unsigned short *)0xffffd006)
/************************************************************************/
/*                              MAIN PROGRAM                            */
/************************************************************************/
void rst_pwm(void)
 {
   P_STBY.MSTCR2.WORD = 0xd2fd;       /* Clear module standby mode */
   P_PORTE.PEIORL.WORD = 0xfa00;      /* TIOC3B/D,TIOC4A/B/C/D output */
   P_PORTE.PECRL1.WORD = 0x5544;
   P_MTU34.TSTR.BYTE = 0x00;
   P_MTU34.TCR_3.BYTE = 0x20;         /* Counter clear by TGRA_3 */
   P_MTU34.TCNT_3 = 0x0000;           /* Clear timer counter3 */
   P_MTU34.TCNT_4 = 0x0000;           /* Clear timer counter4 */
   P_MTU34.TGRA_3 = pul_cyc1;         /* Set period */
   P_MTU34.TGRB_3 = pul_duty3b;       /* Set duty */
   P_MTU34.TGRA_4 = pul_duty4a;
   P_MTU34.TGRB_4 = pul_duty4b;
   P_MTU34.TOCR.BYTE = 0x43;          /* Set timer output control register */
   P_MTU34.TMDR_3.BYTE = 0xc8;        /* Reset synchronized PWM mode */
   P_MTU34.TOER.BYTE = 0xff;          /* Timer output enable */
   P_MTU34.TSTR = 0x40;         /* Start timer counter */
   while(1);
 }
```

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