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April 1st, 2010
Renesas Electronics Corporation

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1. Specifications

Timer output waveform cutoff is performed by driving timer output waveforms to the high-impedance state in synchronization with the falling edge of an external signal, as shown in figure 1.

Figure 1  Example of Externally Triggered Waveform Cutoff
2. Functions Used

In this sample task, waveforms output by MTU ch3/4 (reset-synchronized PWM mode) are cut by being driven to the high-impedance state in synchronization with the falling edge of an external signal.

Figure 2 shows a block diagram of MTU/ch3 and ch4, and the POE.
Table 1 shows the function assignments used in this task. Waveform cutoff is performed by assigning MTU and POE functions as shown in the table.

<table>
<thead>
<tr>
<th>Pin or Register Name</th>
<th>Function</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIOC3B</td>
<td>Pins</td>
<td>Pulse output pins</td>
</tr>
<tr>
<td>TIOC3D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC4A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC4B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC4C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIOC4D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POE0</td>
<td>Pin</td>
<td>Waveform cutoff external signal input pin</td>
</tr>
<tr>
<td>TSTR_3</td>
<td>Register</td>
<td>Enabling/disabling of ch3 timer counter operation</td>
</tr>
<tr>
<td>TCR_3</td>
<td>Register</td>
<td>Selection of ch3 timer counter clearing source and input clock</td>
</tr>
<tr>
<td>TMDR_3</td>
<td>Register</td>
<td>Sets reset-synchronized PWM mode for ch3, ch4</td>
</tr>
<tr>
<td>TGRA_3</td>
<td>Register</td>
<td>PWM period setting</td>
</tr>
<tr>
<td>TGRB_3</td>
<td>Registers</td>
<td>Output waveform transition timing setting</td>
</tr>
<tr>
<td>TGRA_4</td>
<td>Register</td>
<td></td>
</tr>
<tr>
<td>TGRB_4</td>
<td>Register</td>
<td></td>
</tr>
<tr>
<td>TOER</td>
<td>Register</td>
<td>Enabling/disabling of TIOC3B/D and TIOC4A/B/C/D pin timer output</td>
</tr>
<tr>
<td>ICSR</td>
<td>Register</td>
<td>POE input mode selection</td>
</tr>
</tbody>
</table>
3. Operation

Figure 3 illustrates the principles of operation of this sample task. Waveform cutoff is performed automatically by hardware. (See the section on positive-phase/negative-phase PWM 3-phase output in this Application Note for information on the principles of reset-synchronized PWM operation.)

Figure 3  Principles of Operation of Externally Triggered Waveform Cutoff
4. Software

(1) Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label</th>
<th>Function Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>down</td>
<td>DC motor control waveform generation</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label or Register Name</th>
<th>Function Assignment</th>
<th>Data Length</th>
<th>Module</th>
<th>Input/Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>cycle</td>
<td>PWM period setting</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>duk1</td>
<td>Used to set TIOC3B/D output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>duk2</td>
<td>Used to set TIOC4A/C output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>duk3</td>
<td>Used to set TIOC4B/D output waveform transition timing</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(3) Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function Description</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_STBY.MSTCR2</td>
<td>MTU module standby mode clearing, and setting of MTU to operational status</td>
<td>H'FFFF861E</td>
<td>H'd2fd</td>
</tr>
<tr>
<td>P_PORTE.PEIORL</td>
<td>Sets TIOC3B/D, TIOC4A/B/C/D as output pins</td>
<td>H'FFFF83B4</td>
<td>H'fa00</td>
</tr>
<tr>
<td>P_PORTE.PECRL1</td>
<td>Sets TIOC3B/D, TIOC4A/B/C/D as MTU output pins</td>
<td>H'FFFF83B8</td>
<td>H'5544</td>
</tr>
<tr>
<td>P_PORTB.PBCR2</td>
<td>Sets POE0 pin</td>
<td>H'FFFF839A</td>
<td>H'0020</td>
</tr>
<tr>
<td>P_MTU34.TCR_3</td>
<td>Selection of timer counter clearing source and input clock</td>
<td>H'FFFF8200</td>
<td>H'20</td>
</tr>
<tr>
<td>P_MTU34.TOCR</td>
<td>Enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output level setting</td>
<td>H'FFFF820B</td>
<td>H'00</td>
</tr>
<tr>
<td>P_MTU34.TGRA_3</td>
<td>PWM period setting</td>
<td>H'FFFF8218</td>
<td>cycle</td>
</tr>
<tr>
<td>P_MTU34.TGRB_3</td>
<td>Used to set TIOC3B, TIOC3D output waveform transition timing</td>
<td>H'FFFF821A</td>
<td>duk1</td>
</tr>
<tr>
<td>P_MTU34.TGRA_4</td>
<td>Used to set TIOC4A, TIOC4C output waveform transition timing</td>
<td>H'FFFF821C</td>
<td>duk2</td>
</tr>
<tr>
<td>P_MTU34.TGRB_4</td>
<td>Used to set TIOC4B, TIOC4D output waveform transition timing</td>
<td>H'FFFF821E</td>
<td>duk3</td>
</tr>
<tr>
<td>P_MTU34.TOER</td>
<td>Sets TIOC3B/D, TIOC4A/B/C/D as MTU output pins</td>
<td>H'FFFF820A</td>
<td>H'ff</td>
</tr>
<tr>
<td>P_MTU34.TMDR_3</td>
<td>Sets reset-synchronized PWM mode</td>
<td>H'FFFF8202</td>
<td>H'c8</td>
</tr>
<tr>
<td>P_MTU.ICSR1</td>
<td>Sets high-impedance output synchronized with falling edge of POE0 pin input signal</td>
<td>H'FFFF83C0</td>
<td>H'0000</td>
</tr>
</tbody>
</table>

(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.
5. Flowcharts

(1) Main routine

- MSTCR2 ← H'd2fd  
  Clear MTU module standby mode

- ICSR1 ← H'0000  
  Set high-impedance output in synchronization with fall of POE0 pin input signal in ICSR1

- PEIORL ← H'fa00  
  Set TIOC3B/D, TIOC4A/B/C/D as output pins in PEIORL

- PECRL1 ← H'5544  
  Set TIOC3B/D, TIOC4A/B/C/D as MTU output pins in PECRL1

- PBCR2 ← H'0020  
  Set POE0 enabling in PBCR2

- TSTR ← H'00  
  Stop TCNT_3/4

- TCR_3 ← H'20  
  Set TGRA_3 as counter clearing source in TCR_3

- TCNT_3 ← H'0000
  TCNT_4 ← H'0000  
  Clear TCNT_3/4

- TGRA_3 ← cycle  
  Set pulse period in TGRA_3

- TGRB_3 ← duk1
  TGRA_4 ← duk2
  TGRB_4 ← duk3  
  Set duty values in TGRB_3, TGRA_4, TGRB_4

- TOCR ← H'00  
  Set enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output levels, in TOCR

- TMDR_3 ← H'c8  
  Set reset-synchronized PWM mode in TMDR_3

- TOER ← H'ff  
  Set TIOC3B/D, TIOC4A/B/C/D as MTU output pins in TOER

- TSTR ← H'40  
  Enable MTU/ch3 count operation with TSTR
6. Program Listing

```c
/*-----------------------------------------------*/
/* INCLUDE FILE */
/*-----------------------------------------------*/
#include <machine.h>
#include "iodefine_7046.h"
/*-----------------------------------------------*/
/* PROTOTYPE */
/*-----------------------------------------------*/
void down(void);
/*-----------------------------------------------*/
/* RAM ALLOCATION */
/*-----------------------------------------------*/
#define cycle (*(unsigned short *)0xffffd000)
#define duk1 (*(unsigned short *)0xffffd002)
#define duk2 (*(unsigned short *)0xffffd004)
#define duk3 (*(unsigned short *)0xffffd006)
/*-----------------------------------------------*/
/* MAIN PROGRAM */
/*-----------------------------------------------*/
void down(void)
{
  P_STBY.MSTCR2.WORD = 0xd2fd; /* MTU module stop mode clear */
  P_PORTE.PEIORL.WORD = 0xfa00; /* TIOC3B/D,TOC4A/B/C/D output */
  P_PORTE.PECRL1.WORD = 0x5544; /* TIOC3B/D,TOC4A/B/C/D output */
  P_PORTB.PBIOR.WORD = 0x0000; /* POE enable */
  P_PORTB.PBCR1.WORD = 0x0000; /* POE enable */
  P_MTU34.TOCR.BYTE = 0x00; /* stop timer POE0 falling edge */
  P_MTU34.TOCR.BYTE = 0x00;
  P_MTU34.TSTB_3.BYTE = 0x00;
  P_MTU34.TCR_3.BYTE = 0x20; /* timer clear input capture TGRA_3 */
  P_MTU34.TCNT_3 = 0x0000; /* set timer counter3 0x0000 */
  P_MTU34.TCNT_4 = 0x0000; /* set timer counter4 0x0000 */
  P_MTU34.TGRA_3 = cycle; /* period set */
  P_MTU34.TGRB_3 = duk1; /* duty set */
  P_MTU34.TGRB_4 = duk2;
  P_MTU34.TGRB_4 = duk3;
  P_MTU34.TOCR.BYTE = 0x00; /* set output level */
  P_MTU34.TMDR_3.BYTE = 0xc8; /* reset-synchronized pwm mode */
  P_MTU34.TOCR.BYTE = 0xff; /* set timer3,4 output */
  P_MTU34.TSTR.BYTE = 0x40; /* start timer3 */

  while(1); /* loop */
}
```
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