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Renesas Electronics Corporation

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SH7046 Group

Complementary PWM 3-Phase Output

1. Specifications

Three-phase complementary PWM waveform output is performed with a non-overlap time (dead time) between positive and negative phases, as shown in figure 1.

In this task, duty values are set in a data table, and the duty ratio can be changed by interrupt handling.

In this task, 2.0 ms is set for the period, and 0.1 ms for the dead time.

$$\text{Duty} = \frac{\text{Pulse high width}}{\text{Pulse period}} \times 100\ (\%)$$

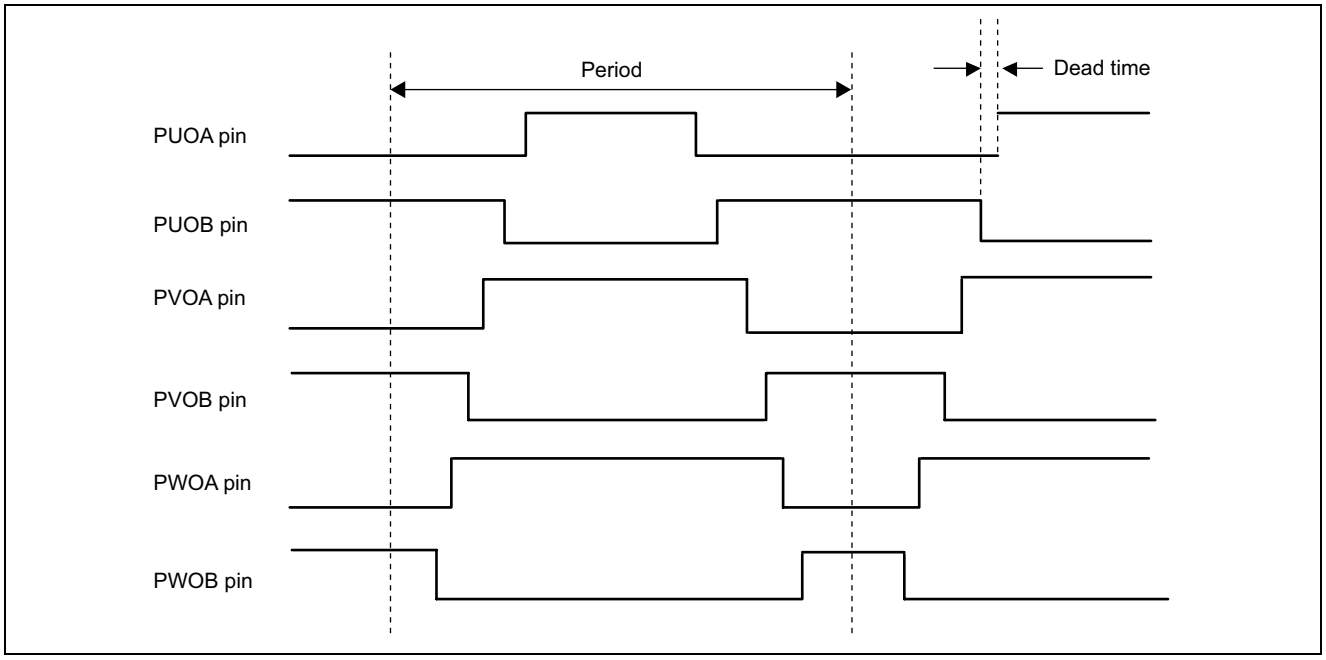


Figure 1 Complementary PWM 3-Phase Output Waveforms

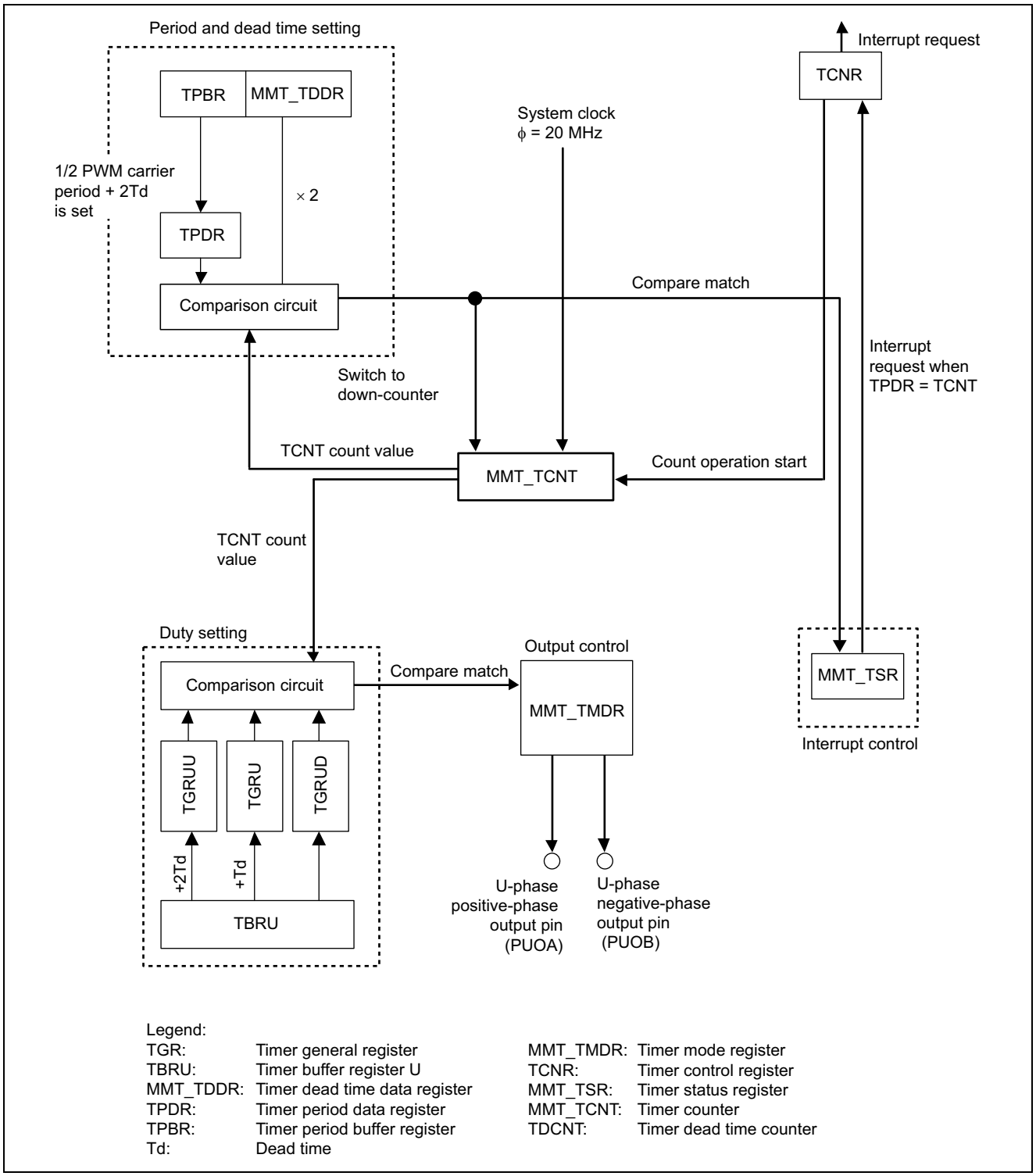
2. Functions Used

In this sample task, 3-phase PWM waveforms with a non-overlap time are output from pins PU0A, PU0B, PV0A, PV0B, PW0A, and PW0B, using the complementary PWM waveform output function.

Figure 2 shows a block diagram of the complementary PWM waveform output function for the U-phase.

The block diagram of the U-phase complementary PWM waveform output function is described below.

- The timer counter (MMT_TCNT) is a 16-bit counter that counts up/down on an input clock.
- The timer period buffer register (TPBR) is a 16-bit readable/writable register that functions as a buffer register for the timer period data register. A register value of 1/2 PWM carrier period is set. In this task, a setting of 2.0 ms is used.
- The timer period data register (TPDR) is a 16-bit read-only register that is compared with MMT_CNT in the operating mode. When the TPDR value matches the MMT_CNT value, MMT_CNT switches direction from up-counting to down-counting, and the TGFM bit in MMT_TSR is set to 1. The TPDR value is [TPBR value + 2Td].
- The timer dead time data register (MMT_TDDR) is a 16-bit readable/writable register that is used to set the non-overlap time (dead time) between positive and negative phases. In this task, a dead time setting of 0.1 ms is used.
- The timer mode register (MMT_TMDR) is an 8-bit readable/writable register that is used for positive-phase/negative-phase output level selection and operating mode setting.
- The timer control register (TCNR) is an 8-bit readable/writable register that selects operation/halting of MMT_CNT, and, when the TGFM bit in MMT_TSR is set to 1, enables/disables interrupt requests.
- Timer buffer register U is a 16-bit readable/writable register that functions as the TGR buffer register. A value written to TBR is transferred to TGR at the timing set by MD1 and MD0 in MMT_TMDR. However, a value written to the TBR free-operation register is transferred to TGR immediately. In this task, the free-operation register is used.
- Timer general register UD (TGRUD) is a 16-bit read-only register to which the TBRU value is transferred. MMT_CNT is compared with TGRUD when counting down.
- Timer general register U (TGRU) is a 16-bit read-only register to which the value of TBRU+Td is transferred. TGRU is constantly compared with MMT_CNT.
- Timer general register UU (TGRUU) is a 16-bit read-only register to which the value of TBRU+2Td is transferred. MMT_CNT is compared with TGRUU when counting up.
- The PWM U-phase (positive-phase) output pin (PU0A) outputs the U-phase positive-phase waveform.
- The PWM U-phase (negative-phase) output pin (PU0B) outputs the U-phase negative-phase waveform.



Legend:

TGR:	Timer general register	MMT_TMDR:	Timer mode register
TBRU:	Timer buffer register U	TCNR:	Timer control register
MMT_TDDR:	Timer dead time data register	MMT_TSR:	Timer status register
TPDR:	Timer period data register	MMT_TCNT:	Timer counter
TPBR:	Timer period buffer register	TDCNT:	Timer dead time counter
Td:	Dead time		

Figure 2 MTU U-Phase Block Diagram

Table 1 shows the function assignments used in this task.

Table 1 Function Assignments

Pin or Register Name	Function	Function Assignment
PUOA	Pin	PWM U-phase output (positive phase)
PUOB	Pin	PWM U-phase output (negative phase)
TBRU	Register	TGRUD, TGRU, TGRUU buffer register
MMT_TDDR	Register	Setting of non-overlap time (Td: dead time) between positive and negative phases
TPBR	Register	TPDR buffer register. Value of 1/2 PWM carrier period is set
TPDR	Register	1/2 PWM period + 2Td
MMT_TSR	Register	Indicates TCNT/TPDR, 2Td compare match occurrence
TCNR	Register	Interrupt request enabling/disabling control Register access enabling/disabling selection Counter operation/halting selection
MMT_TMDR	Register	Operating mode setting, PWM output level selection

3. Operation

Figure 3 illustrates the principles of operation of complementary PWM waveform output by SH7046 hardware and software processing.

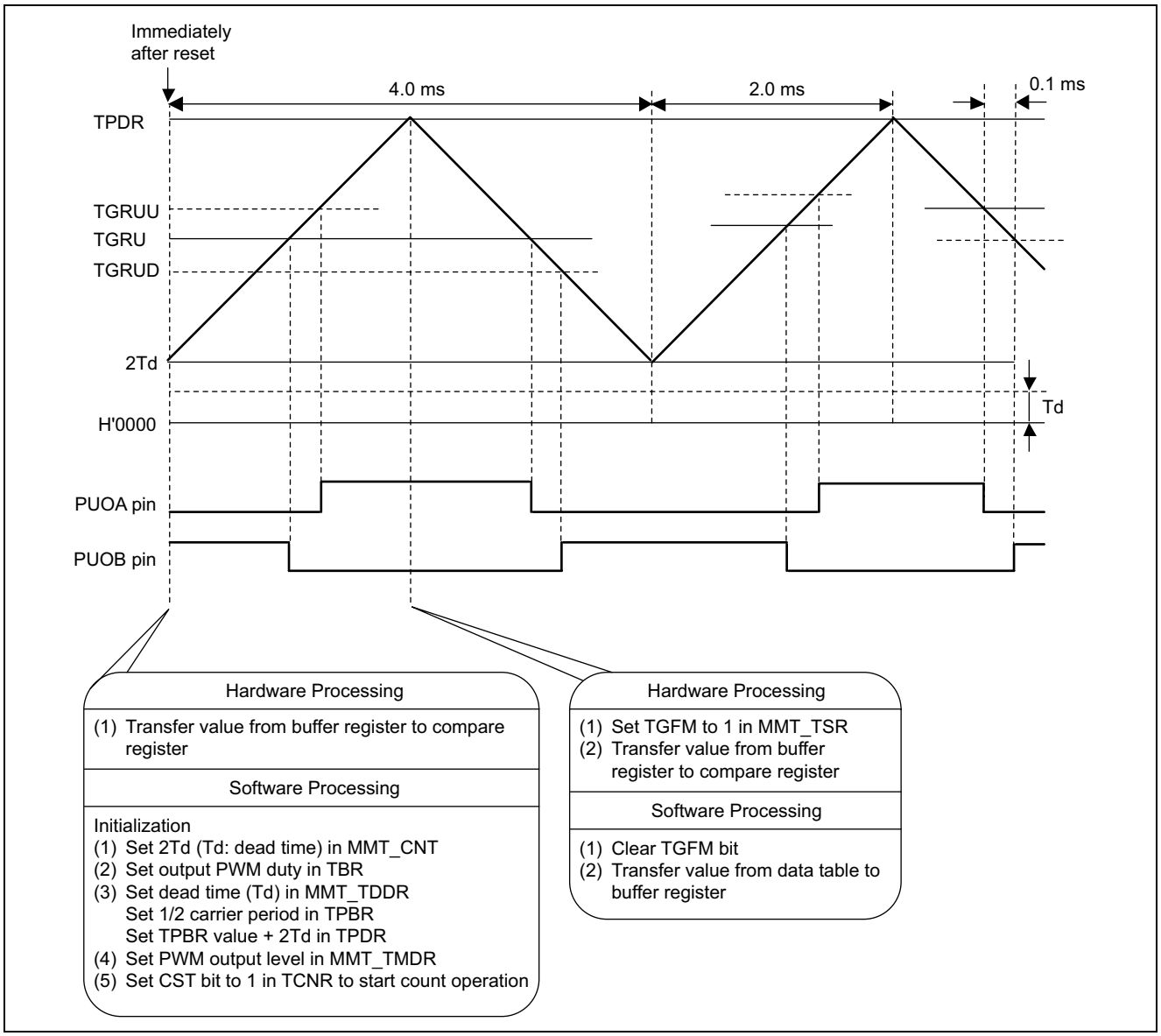


Figure 3 Principles of Operation of Complementary PWM Waveform Output

Figure 4 shows the PWM waveform output method. When complementary PWM mode is set, the following rules apply to data transfer and compare operations.

- Data Transfer
  - In the operating mode, a buffer register is used when updating compare register data. The update data is fetched from a data table.
  - Regarding the timing of data transfer from the data table to the buffer register, transfer is performed by interrupt handling when TGFM is set to 1 by a compare match between MMT_TCNT and TPDR.
  - In this sample task TBRU free operation addresses are used, and therefore buffer register data is transferred to the compare register immediately.
- Compare Output Waveform (for U-Phase)

  Regarding the compare output waveform, MMT_TCNT is compared with TGRU, TGRUU, and TGRUD, and a PWM waveform is generated.

  U-phase A
  - In period T1 (during TCNT up-counting), MMT_TCNT and TGRUU are compared.
  - In period T2 (during TCNT down-counting), MMT_TCNT and TGRU are compared.

  U-phase B
  - In period T1 (during TCNT up-counting), MMT_TCNT and TGRU are compared.
  - In period T2 (during TCNT down-counting), MMT_TCNT and TGRUD are compared.
- Period Setting

  In case of 20 MHz operation:

  Set while 1/2 period (TPBR) = H'0000 to H'FFFF (3.27675 ms) – 4Td.

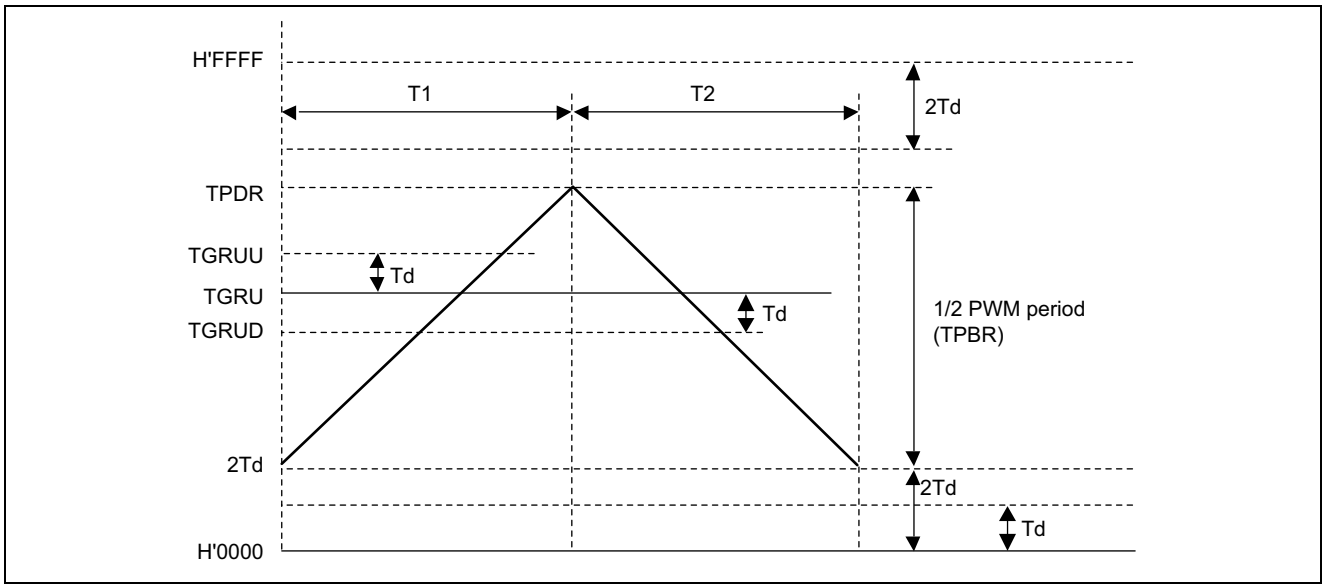


Figure 4 Principles of Operation of PWM Waveform Output Method

Figure 5 illustrates the principles of operation. Complementary PWM waveform output is performed by SH7046 hardware and software processing. In this sample task TBRU free operation addresses are used.

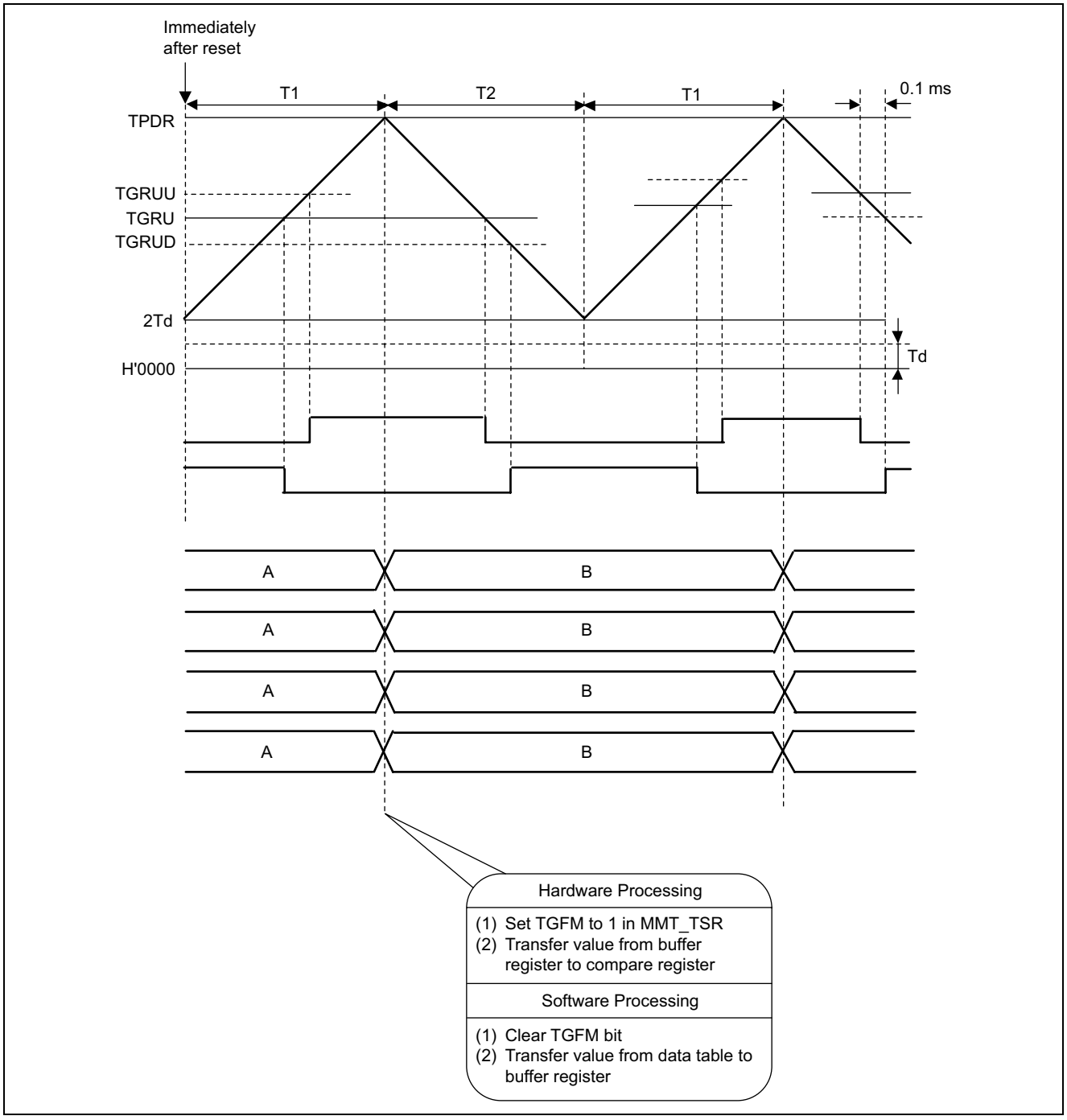


Figure 5 Principles of Operation of Complementary PWM U-Phase Waveform

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	mmt	MMT initialization
Duty change routine call	UP	Calls U-phase/V-phase/W-phase duty switching routine when TGFM interrupt occurs
U-phase duty change	set_u	Changes U-phase duty ratio each time TGFM interrupt occurs
V-phase duty change	set_v	Changes V-phase duty ratio each time TGFM interrupt occurs
W-phase duty change	set_w	Changes W-phase duty ratio each time TGFM interrupt occurs

(2) Arguments

This sample task does not use any arguments.

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_STBY.MSTCR2	MTU module standby mode clearing	H'FFFF861E	H'b2fd
P_PORTE.PECRH	Sets port E pins as MMT output pins	H'FFFF83BC	H'0555
P_PORTE.PEIORH	Sets port E pins as output pins	H'FFFF83B6	H'003f
P_MMT.MMT_TCNT	2Td (Td: dead time) is set	H'FFFF8A06	H'0fa0
P_MMT.TBRU_F	Used to set U-phase PWM duty (PWM duty – Td)	H'FFFF8A1C	H'2710
P_MMT.TBRV_F	Used to set V-phase PWM duty (PWM duty – Td)	H'FFFF8A2C	H'55f0
P_MMT.TBRW_F	Used to set W-phase PWM duty (PWM duty – Td)	H'FFFF8A3C	H'84b0
P_MMT.MMT_TDDR	Dead time setting	H'FFFF8A0C	H'07d0
P_MMT.TPBR	Setting of 1/2 PWM carrier period	H'FFFF8A0A	H'9c40
P_MMT.MMT_TMDR	Operating mode setting	H'FFFF8A00	H'0e
P_MMT.TCNR	Enables TGFM interrupts	H'FFFF8A02	H'41

(4) RAM Used

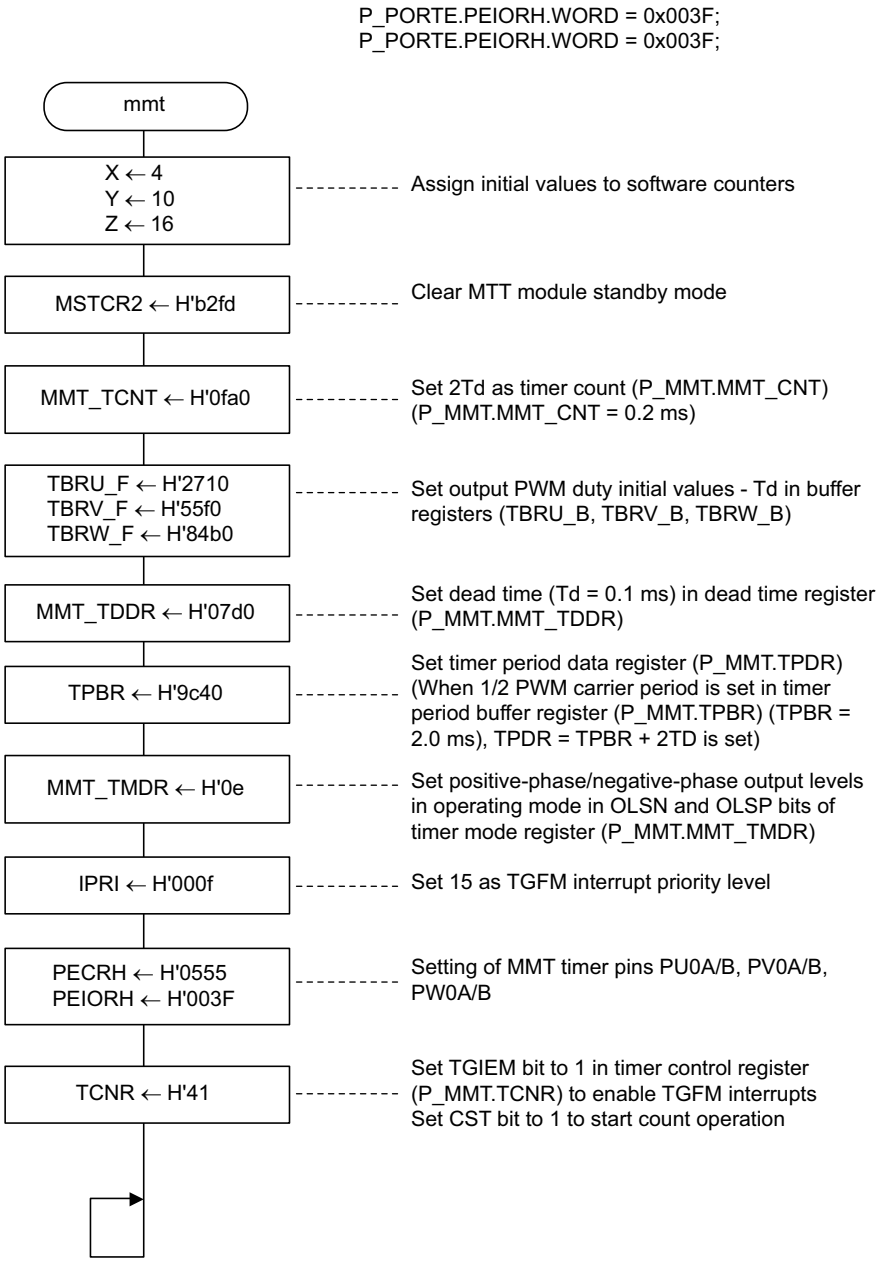
Label	Function	Address	Module
X	U-phase duty change counter	H'FFFFD000	set_u
Y	V-phase duty change counter	H'FFFFD001	set_v
Y	W-phase duty change counter	H'FFFFD002	set_w

(5) Data Table

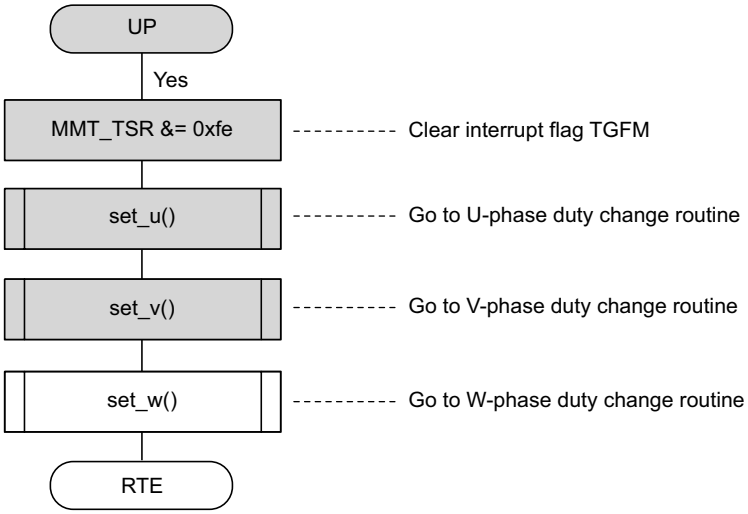
In this task, a data table (t_data) is referenced and the PWM duty ratio of each phase is changed by interrupt handling.

5. Flowcharts

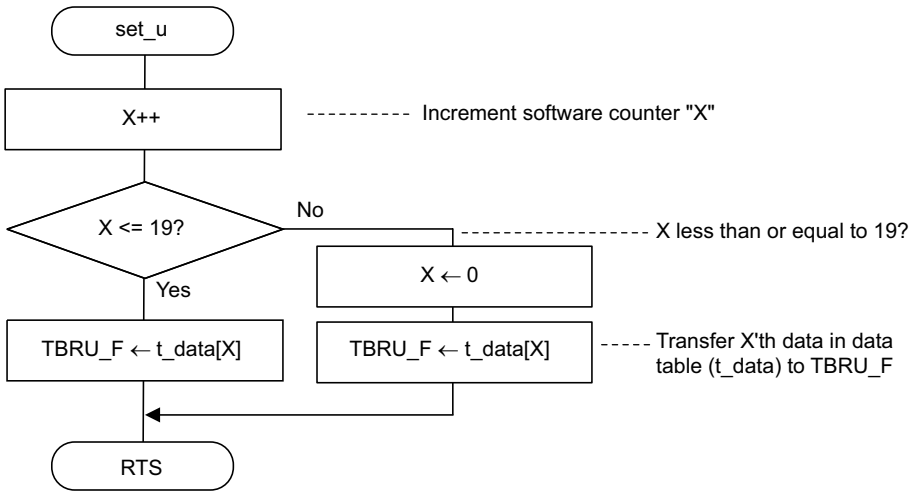
(1) Main routine



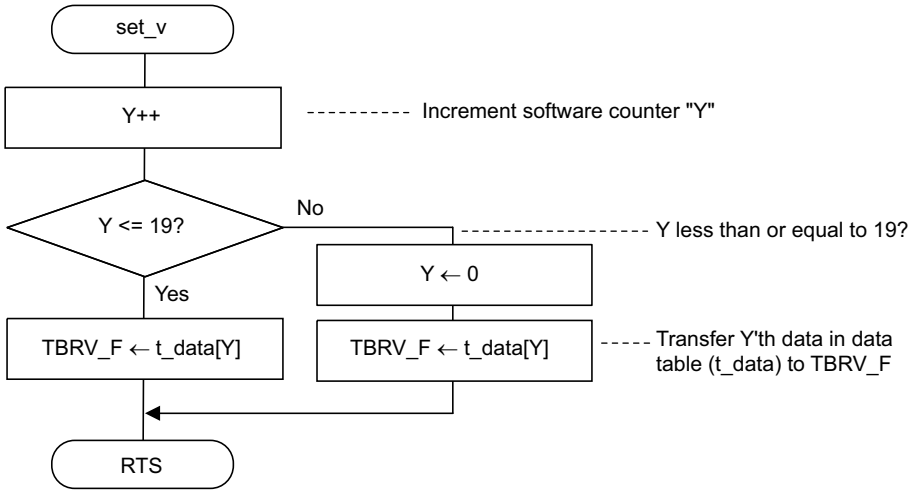
(2) Interrupt routine



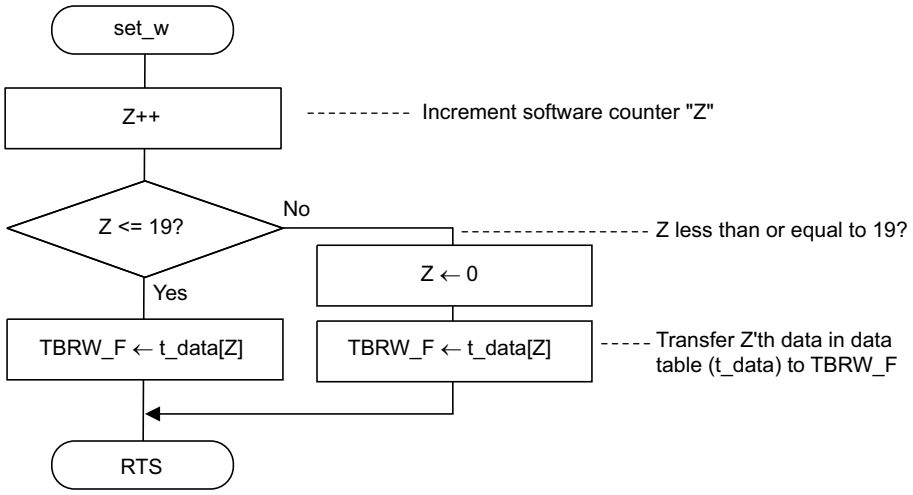
(3) U-phase output



(4) V-phase output



(5) W-phase output



6. Program Listing

```
/*----------------------------------------------------------------------*/
/*                          INCLUDE FILE                                */
/*----------------------------------------------------------------------*/
#include <machine.h>
#include "iodefine_7046.h"
/*----------------------------------------------------------------------*/
/*                            PROTOTYPE                                 */
/*----------------------------------------------------------------------*/
void mmt(void);
void set_u(void);
void set_v(void);
void set_w(void);
#pragma interrupt(UP)
/*----------------------------------------------------------------------*/
/*                            MAIN PROGRAM                              */
/*----------------------------------------------------------------------*/
const short t_data[20] = {0x07d0,0x1770,0x2710,0x36b0,
                          0x4650,0x55f0,0x6590,0x7530,
                          0x84d0,0x9470,0xa410,0x9470,
                          0x84d0,0x7530,0x6590,0x55f0,
                          0x4650,0x36b0,0x2710,0x1770
                          };

  unsigned char X ;
  unsigned char Y ;
  unsigned char Z ;

void mmt(void)
{
   X=4 ;
   Y=10 ;
   Z=16 ;
   P_STBY.MSTCR2.WORD = 0xb2fd; /* MMT module stop mode clear */

   P_MMT.MMT_TCNT = 0x0FA0;
   P_MMT.TBRU_F = 0x2710;
   P_MMT.TBRV_F = 0x55F0;
   P_MMT.TBRW_F = 0x84B0;
   P_MMT.MMT_TDDR = 0x07D0;
   P_MMT.TPBR = 0x9C40;
   P_MMT.MMT_TMDR.BYTE = 0x0E;  /* output level High, mode2 */
   P_INTC.IPRI.WORD = 0x000f;   /* set interrupt level=15 */
   P_PORTE.PECRH.WORD = 0x0555; /* PUOA/B,PVOA/B,PWOA/B output */
   P_PORTE.PEIORH.WORD = 0x003F;       /* PUOA/B,PVOA/B,PWOA/B output */
   P_MMT.TCNR.BYTE = 0x41;      /* timer counter start, TGFM interrupt enable */
   set_imask(0x0);      /* set imask level=0 */
   while(1);     /* loop */
 }

void UP()
{
   P_MMT.MMT_TSR.BYTE &= 0xfe;         /* TGFM flag clear */
```

```
   set_u();  /* change duty Phase U */
   set_v();  /* change duty Phase V */
   set_w();  /* change duty Phase W */
}

void set_u()
{
      X++;   /* increment software counter X */
      if(X <= 19){     /* X<=19? */
              P_MMT.TBRU_F = t_data[X];      /* Phase U duty = t_data[X] */
              }
      else{
              X = 0;   /* Clear software counter X */
              P_MMT.TBRU_F = t_data[X];      /* Phase U duty = t_data[X] */
              }

}
void set_v()
{
      Y++;   /* increment software counter Y */
      if(Y <= 19){     /* Y<=19? */
              P_MMT.TBRV_F = t_data[Y];      /* Phase V duty = t_data[Y] */
              }
      else{
              Y = 0;   /* Clear software counter Y */
              P_MMT.TBRV_F = t_data[Y];      /* Phase V duty = t_data[Y] */
              }
}

void set_w()
{
     Z++;    /* increment software counter Z */
     if(Z <= 19){   /* Z<=19? */
             P_MMT.TBRW_F = t_data[Z];       /* Phase W duty = t_data[Z] */
             }
     else{
             Z = 0;    /* Clear software counter Z */
             P_MMT.TBRW_F = t_data[Z];       /* Phase W duty = t_data[Z] */
             }
}
```

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