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Renesas Electronics Corporation

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SH7000 Series

Multi-Bit Shift of 32-Bit Data (Logical Left Shift)

Label: SHLLN

Functions Used: SHLL2 Instruction
SHLL8 Instruction
SHLL16 Instruction

Contents

1. Function

Performs a multi-bit (0–31) logical left shift of 32-bit data.

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Number of shift bits (0–31)	R0	4
	32-bit data before shift	R1	4
Output	32-bit data after shift	R1	4

3. Internal Register Changes and Flag Changes

	(Before Execution) → (After Execution)
R0	Number of shift bits → No change
R1	32-bit data before shift → 32-bit data after shift
R2	
R3	
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

T bit | * |

— : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
36
Data memory (bytes)
0
Stack (bytes)
0
Number of states
19
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Notes

The number of states indicated in the programming specifications is the value when a 31-bit shift is performed.

6. Description

(1) Function

Details of the arguments are as follows.

R0: As the input argument, set the number of shift bits (0–31).
R1: Set the 32-bit data before the shift as the input argument.
Holds the 32-bit data after the shift as the output argument.

Figure 1 shows a software SHLLN execution example.

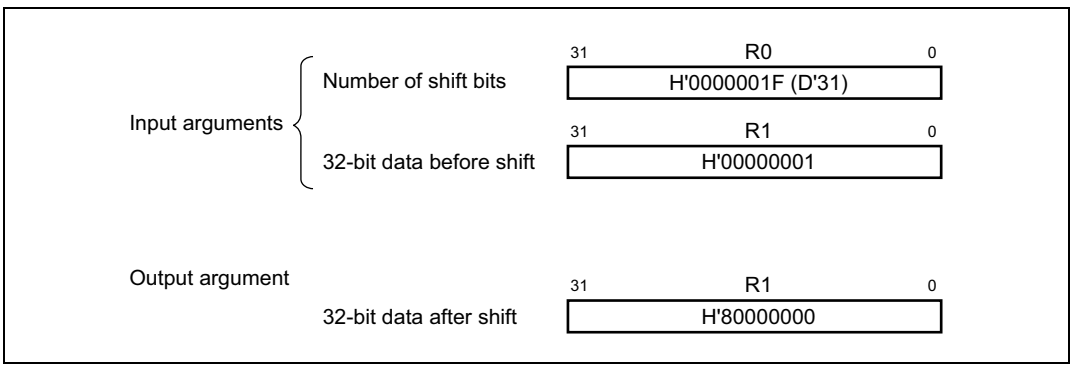


Figure 1 Software SHLRN Execution Example

(2) Usage Notes

The contents of R1, which holds the 32-bit data before the shift, are destroyed after the shift when the 32-bit data after the shift is stored there. If the value for the 32-bit data before the shift will be needed after the software SHLLN instruction is executed, it should be saved beforehand.

(3) RAM Used

No RAM is used by the software SHLLN instruction.

(4) Usage Example

After the number of shift bits and the 32-bit data before the shift have been set in the input arguments, the software SHLLN instruction is executed by a subroutine call.

```
        MOV     #H'05,R0        ....Sets number of shift bits in input argument (R0)
        BSR     SHLLN           ....Subroutine call to software SHLLN
        MOV.L   DATA,R1         ....Sets 32-bit data before shift in input argument (R1)
                .
                .
                .
                .
      .align    4
DATA  .data.l   H'00000001
```

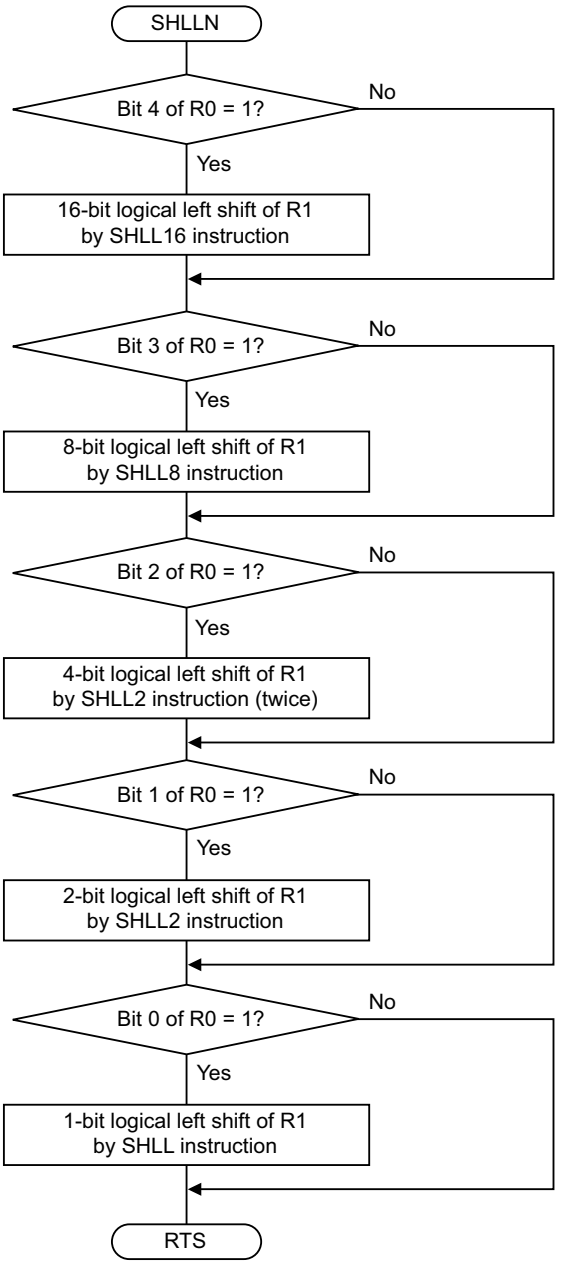
(5) Operating Principle

(a) Bits 4 to 0 in R0, which is set to the number of shift bits, are tested. If any of them have a value of 1, a shift corresponding to the weighting of the bits in question is performed using the 16-bit logical left shift command (SHLL16), the 8-bit logical left shift command (SHLL8), the 2-bit logical left shift command (SHLL2), and the 1-bit logical left shift command (SHLL).

Table 1 Number of Shift Bits and Instructions Used for Each Bit

Bit Number	Weighting	Instruction
Bit 4	$2^4 = 16$	SHLL16
Bit 3	$2^3 = 8$	SHLL8
Bit 2	$2^2 = 4$	SHLL2 (twice)
Bit 1	$2^1 = 2$	SHLL2
Bit 0	$2^0 = 1$	SHLL

7. Flowchart


SHLLN
Bit 4 of R0 = 1?
No
Yes
16-bit logical left shift of R1
by SHLL16 instruction
Bit 3 of R0 = 1?
No
Yes
8-bit logical left shift of R1
by SHLL8 instruction
Bit 2 of R0 = 1?
No
Yes
4-bit logical left shift of R1
by SHLL2 instruction (twice)
Bit 1 of R0 = 1?
No
Yes
2-bit logical left shift of R1
by SHLL2 instruction
Bit 0 of R0 = 1?
No
Yes
1-bit logical left shift of R1
by SHLL instruction
RTS

8. Program Listing

```
 1                      1   ;*************************************************************
 2                      2   ;*                                                           *
 3                      3   ;*       NAME ; n BITS SHIFT LOGICAL LEFT (SHLLN)            *
 4                      4   ;*                                                           *
 5                      5   ;*************************************************************
 6                      6   ;*                                                           *
 7                      7   ;*      ENTRY : R0   (NUMBER OF BIT SHIFTED)                 *
 8                      8   ;*              R1   (32 BIT DATA)                           *
 9                      9   ;*    RETURNS : R1   (SHIFT RESULT)                          *
10                     10   ;*                                                           *
11                     11   ;*************************************************************
12 00001000            12           .SECTION A,CODE,LOCATE=H'1000
13          00001000   13   SHLLN   .EQU    $               ; Entry point
14 00001000            14   SHLLN1                          ;
15 00001000 CB10       15           TST     #B'00010000,R0  ; Bit 4 = 1?
16 00001002 8900       16           BT      SHLLN2          ; No
17 00001004 4128       17           SHLL16  R1              ; 16 bit shift logical left
18 00001005            18   SHLLN2                          ;
19 00001006 C808       19           TST     #B'00001000,R0  ; Bit 3 = 1?
20 00001008 8900       20           BT      SHLLN3          ; No
21 0000100A 4118       21           SHLL8   R1              ; 8 bit shift logical left
22 0000100C            22   SHLLN3                          ;
23 0000100C C804       23           TST     #B'00000100,R0  ; Bit 2 = 1?
24 0000100E 8901       24           BT      BHLLN4          ; No
25 00001010 4108       25           SHLL2   R1              ; 4 bit shift logical left
26 00001012 4108       26           SHLL2   R1              ;
27 00001014            27   SHLLN4                          ;
28 00001014 C802       28           TST     #B'00000010,R0  ; Bit 1 = 1?
29 00001016 8900       29           BT      SHLLN5          ; No
30 00001018 4108       30           SHLL2   R1              ; 2 bit shift logical left
31 0000101A            31   SHLLN5                          ;
32 0000101A C801       32           TST     #B'00000001,R0  ; Bit 0 = 1?
33 0000101C 8900       33           BT      SHLLN_END       ; No
34 0000101E 4100       34           SHLL    R1              ; 1 bit shift logical left
35 00001020            35   SHLLN_END                       ;
36 00001020 000B       36           RTS                     ;
37 00001022 0009       37           NOP                     ;
38                     38           .END
*****TOTAL ERRORS    0
*****TOTAL WARNINGS  0
```

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