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April 1\(^{st}\), 2010
Renesas Electronics Corporation

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SH7000 Series
Multi-Bit Shift of 32-Bit Data (Arithmetic Right Shift)

Label: SHARN

Functions Used: SHLR2 Instruction
                SHLR8 Instruction
                SHLR16 Instruction

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1. Function

Performs a multi-bit (0–31) arithmetic right shift of 32-bit data.

2. Arguments

<table>
<thead>
<tr>
<th>Description</th>
<th>Storage Location</th>
<th>Data Length (Bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Number of shift bits</td>
<td>R0</td>
<td>4</td>
</tr>
<tr>
<td>32-bit data before shift</td>
<td>R1</td>
<td>4</td>
</tr>
<tr>
<td>Output 32-bit data after shift</td>
<td>R1</td>
<td>4</td>
</tr>
</tbody>
</table>

3. Internal Register Changes and Flag Changes

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>(Before Execution)</th>
<th>(After Execution)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>Number of shift bits</td>
<td></td>
<td>Change</td>
</tr>
<tr>
<td>R1</td>
<td>32-bit data before shift</td>
<td></td>
<td>32-bit data after shift</td>
</tr>
<tr>
<td>R2</td>
<td>Work</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>Work</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R15</td>
<td></td>
<td>(SP)</td>
<td></td>
</tr>
</tbody>
</table>

T bit  
* : No change
* : Change
0 : Fixed 0
1 : Fixed 1
4. Programming Specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Program memory (bytes)</td>
<td>74</td>
</tr>
<tr>
<td>Data memory (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Stack (bytes)</td>
<td>8</td>
</tr>
<tr>
<td>Number of states</td>
<td>38</td>
</tr>
<tr>
<td>Reentrant</td>
<td>Yes</td>
</tr>
<tr>
<td>Relocation</td>
<td>Yes</td>
</tr>
<tr>
<td>Intermediate interrupt</td>
<td>Yes</td>
</tr>
</tbody>
</table>

5. Notes

The number of states indicated in the programming specifications is the value when a 31-bit shift is performed.
6. Description

(1) Function

Details of the arguments are as follows.

R0: As the input argument, set the number of shift bits (0–31).
R1: Set the 32-bit data before the shift as the input argument.

Holds the 32-bit data after the shift as the output argument.

Figure 1 shows a software SHARN execution example.

<table>
<thead>
<tr>
<th>Input arguments</th>
<th>Output argument</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of shift bits</td>
<td>31 0</td>
</tr>
<tr>
<td>R0</td>
<td>H'00000001F (D'31)</td>
</tr>
<tr>
<td>32-bit data before shift</td>
<td>31 0</td>
</tr>
<tr>
<td>R1</td>
<td>H'80000000</td>
</tr>
<tr>
<td>32-bit data after shift</td>
<td>31 0</td>
</tr>
<tr>
<td>R1</td>
<td>H'FFFFFFFF</td>
</tr>
</tbody>
</table>

Figure 1   Software SHARN Execution Example

(2) Usage Notes

The contents of R1, which holds the 32-bit data before the shift, are destroyed after the shift when the 32-bit data after the shift is stored there. In addition, execution of the software SHARN instruction changes the setting of R0, which specified the number of shift bits.

If the values for the 32-bit data before the shift and the number of shift bits will be needed after the software SHARN instruction is executed, they should be saved beforehand.

(3) RAM Used

No RAM is used by the software SHARN instruction.
(4) Usage Example

After the number of shift bits and the 32-bit data before the shift have been set in the input arguments, the software SHARN instruction is executed by a subroutine call.

```assembly
MOV    #H'05, R0 .... Sets number of shift bits in input argument (R0)
BSR    SHARN .... Subroutine call to software SHARN
MOV.L  DATA, R1 .... Sets 32-bit data before shift in input argument (R1)

.align 4
DATA   .data.l H'80000000
```

(5) Operating Principle

(a) Bits 4 to 0 in R0, which is set to the number of shift bits, are tested. If any of them have a value of 1, a shift corresponding to the weighting of the bits in question is performed using the 16-bit logical right shift command (SHLR16), the 8-bit logical right shift command (SHLR8), the 2-bit logical right shift command (SHLR2), and the 1-bit logical right shift command (SHLR).

Table 1 Number of Shift Bits and Instructions Used for Each Bit

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Weighting</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 4</td>
<td>$2^4 = 16$</td>
<td>SHLR16</td>
</tr>
<tr>
<td>Bit 3</td>
<td>$2^3 = 8$</td>
<td>SHLR8</td>
</tr>
<tr>
<td>Bit 2</td>
<td>$2^2 = 4$</td>
<td>SHLR2 (twice)</td>
</tr>
<tr>
<td>Bit 1</td>
<td>$2^1 = 2$</td>
<td>SHLR2</td>
</tr>
<tr>
<td>Bit 0</td>
<td>$2^0 = 1$</td>
<td>SHLR</td>
</tr>
</tbody>
</table>
(b) Since the 32-bit data before the shift is shifted 16 bits, 8 bits, 2 bits, and 1 bit by the logical right shift instructions, when the MSB of 32-bit data before shift is 1, the empty MSB following the shift becomes not 1 but 0.

Therefore, if R2 contains H'FFFFFFFF, as shown in figure 2, and this data is shifted logically right by the same number of bits as the 32-bit data before the shift, and if the MSB before the shift is 1, after the shift the top bits of the shifted portion are set to 1 by a logical OR with the inverted R2 value.

![Figure 2 - Multiple Bit Shift](image-url)
7. Flowchart

```
SHARN
  Save registers
  Set R2 to H'FFFF FFFF
  Save MSB (sign bit) of 32-bit data before shift to LSB of R3
    Bit 4 of R0 = 1?
      No
      16-bit logical right shift of R1 and R2 by SHLR16 instruction
    Bit 3 of R0 = 1?
      No
      8-bit logical right shift of R1 and R2 by SHLR8 instruction
    Bit 2 of R0 = 1?
      No
      4-bit logical right shift of R1 and R2 by SHLR2 instruction (twice)
    Bit 1 of R0 = 1?
      No
      2-bit logical right shift of R1 and R2 by SHLR2 instruction
    Bit 0 of R0 = 1?
      No
      1-bit logical right shift of R1 and R2 by SHLR instruction
    MSB (LSB of R3) of 32-bit data before shift is 1?
      No
      Invert R2
      Logically OR R1 and R2 and store in R1
      Restore registers
      RTS
```
8. Program Listing

NAME: n BITS SHIFT ARITHMETIC RIGHT (SHARN)
ENTRY: R0 (NUMBER OF BIT SHIFTED)
          R1 (32 BIT DATA)
RETURNS: R1 (SHIFT RESULT)

```assembly
1 ; 00001000 12 .SECTION A, CODE,LOCATE=H'1000
13 00001000 13 SHARN .EQU $ ; Entry point
14 00001000 2F26 14 MOV.L R2,0-R15 ; Escape register
15 00001000 2F36 15 MOV.L R3,0-R15 ;
16 00001000 16 SHARN1 ;
17 00001000 3228 17 SUB R2,R2 ; R2 ← H'FFFFFFFF
18 00001000 4104 18 NOT R2,R2 ;
19 00001000 19 SHARN2 ;
20 00001000 4104 20 ROTL R1 ; R3 ← MSB of 32 bit data
21 00001000 4129 21 MOV.R R3 ;
22 00001000 4105 22 ROTR R1 ;
23 00001000 19 SHARN3 ;
24 00001000 C810 24 TST #B'00010000,R0 ; Bit4=1?
25 00001000 8901 25 BT SHARN4 ; No
26 00001000 4129 26 SHR16 R1 ; 16 bit shift logical right
27 00001000 4229 27 SHR16 R2 ;
28 00001000 28 SHARN4 ;
29 00001000 C808 29 TST #B'00001000,R0 ; Bit3=1?
30 00001000 8901 30 BT SHARN5 ; No
31 00001000 4119 31 SHR8 R1 ; 8 bit shift logical right
32 00001000 4219 32 SHR8 R2 ;
33 00001000 33 SHARN5 ;
34 00001000 C804 34 TST #B'00000100,R0 ; Bit2=1?
35 00001000 8903 35 BT SHARN6 ; No
36 00001000 4109 36 SHR2 R1 ; 4 bit shift logical right
37 00001000 4209 37 SHR2 R2 ;
38 00001000 4209 38 SHR2 R2 ;
39 00001000 39 SHARN6 ;
40 00001000 40 SHARN6 ;
41 00001000 C802 41 TST #B'00000010,R0 ; Bit1=1?
42 00001000 8901 42 BT SHARN7 ; No
43 00001000 4109 43 SHR2 R1 ; 2 bit shift logical right
44 00001000 4209 44 SHR2 R2 ;
45 00001000 45 SHARN7 ;
```

SH7000 Series
Multi-Bit Shift of 32-Bit Data
(Arithmetic Right Shift)
SH7000 Series
Multi-Bit Shift of 32-Bit Data
(Arithmetic Right Shift)

46 00001032 C801  46  TST  #B'00000001,R0 ; Bit 0 = 1?
47 00001034 8901  47  BT   SHARN8 ; No
48 00001036 4101  48  SHLR R1 ; 1 bit shift logical right
49 00001038 4201  49  SHLR R2 ;
50 0000103A 6033  50  MOV  R3,R0 ;
51 0000103A 6033  51  MOV  R3,R0 ; MSB of 32 bit data = 1?
52 0000103C 8901  52  BT   SHARN_END ; No
53 00001040 6227  53  NOT  R2,R2 ;
54 00001042 212B  54  OR   R2,R1 ;
55 00001044 63F6  55  MOV.L @R15+,R3 ; Return register
56 00001046 000B  56  RTS  ;
57 00001048 62F6  57  MOV.L @R15+,R2 ;
58 0000104A 6036  58  .END

*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
SH7000 Series
Multi-Bit Shift of 32-Bit Data
(Arithmetic Right Shift)

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