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SH7000 Series

Multi-Bit Shift of 32-Bit Data (Arithmetic Right Shift)

Label: SHARN

Functions Used: SHLR2 Instruction
SHLR8 Instruction
SHLR16 Instruction

Contents

1. Function

Performs a multi-bit (0–31) arithmetic right shift of 32-bit data.

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Number of shift bits (0–31)	R0	4
	32-bit data before shift	R1	4
Output	32-bit data after shift	R1	4

3. Internal Register Changes and Flag Changes

	(Before Execution) → (After Execution)
R0	Number of shift bits → Change
R1	32-bit data before shift → 32-bit data after shift
R2	Work
R3	Work
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	(SP)

T bit [*]
— : No change
* : Change
0 : Fixed 0
1 : Fixed 1

4. Programming Specifications

Program memory (bytes)
74
Data memory (bytes)
0
Stack (bytes)
8
Number of states
38
Reentrant
Yes
Relocation
Yes
Intermediate interrupt
Yes

5. Notes

The number of states indicated in the programming specifications is the value when a 31-bit shift is performed.

6. Description

(1) Function

Details of the arguments are as follows.

R0: As the input argument, set the number of shift bits (0–31).
R1: Set the 32-bit data before the shift as the input argument.

Holds the 32-bit data after the shift as the output argument.

Figure 1 shows a software SHARN execution example.

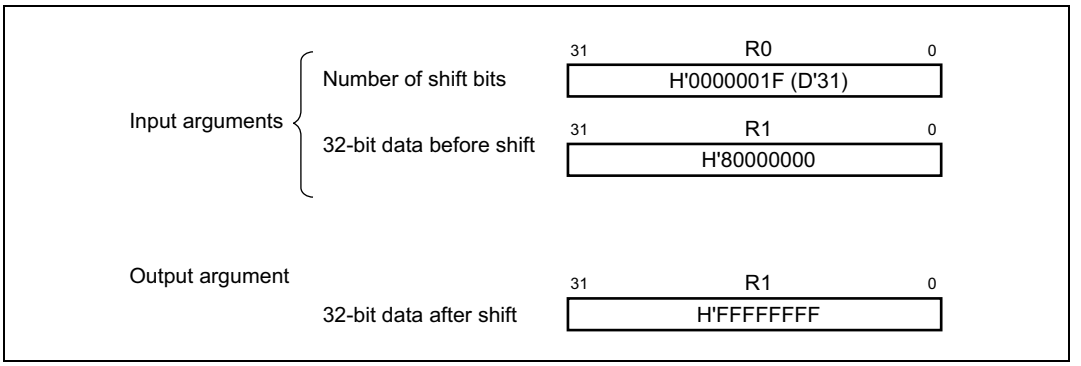


Figure 1 Software SHARN Execution Example

(2) Usage Notes

The contents of R1, which holds the 32-bit data before the shift, are destroyed after the shift when the 32-bit data after the shift is stored there. In addition, execution of the software SHARN instruction changes the setting of R0, which specified the number of shift bits.

If the values for the 32-bit data before the shift and the number of shift bits will be needed after the software SHARN instruction is executed, they should be saved beforehand.

(3) RAM Used

No RAM is used by the software SHARN instruction.

(4) Usage Example

After the number of shift bits and the 32-bit data before the shift have been set in the input arguments, the software SHARN instruction is executed by a subroutine call.

```
        MOV     #H'05,R0      .... Sets number of shift bits in input argument (R0)
        BSR     SHARN         .... Subroutine call to software SHARN
        MOV.L   DATA,R1       .... Sets 32-bit data before shift in input argument (R1)
                .
                .
                .
                .
      .align    4
DATA  .data.l   H'80000000
```

(5) Operating Principle

(a) Bits 4 to 0 in R0, which is set to the number of shift bits, are tested. If any of them have a value of 1, a shift corresponding to the weighting of the bits in question is performed using the 16-bit logical right shift command (SHLR16), the 8-bit logical right shift command (SHLR8), the 2-bit logical right shift command (SHLR2), and the 1-bit logical right shift command (SHLR).

Table 1 Number of Shift Bits and Instructions Used for Each Bit

Bit Number	Weighting	Instruction
Bit 4	$2^4 = 16$	SHLR16
Bit 3	$2^3 = 8$	SHLR8
Bit 2	$2^2 = 4$	SHLR2 (twice)
Bit 1	$2^1 = 2$	SHLR2
Bit 0	$2^0 = 1$	SHLR

(b) Since the 32-bit data before the shift is shifted 16 bits, 8 bits, 2 bits, and 1 bit by the logical right shift instructions, when the MSB of 32-bit data before shift is 1, the empty MSB following the shift becomes not 1 but 0.

Therefore, if R2 contains H'FFFFFFFF, as shown in figure 2, and this data is shifted logically right by the same number of bits as the 32-bit data before the shift, and if the MSB before the shift is 1, after the shift the top bits of the shifted portion are set to 1 by a logical OR with the inverted R2 value.

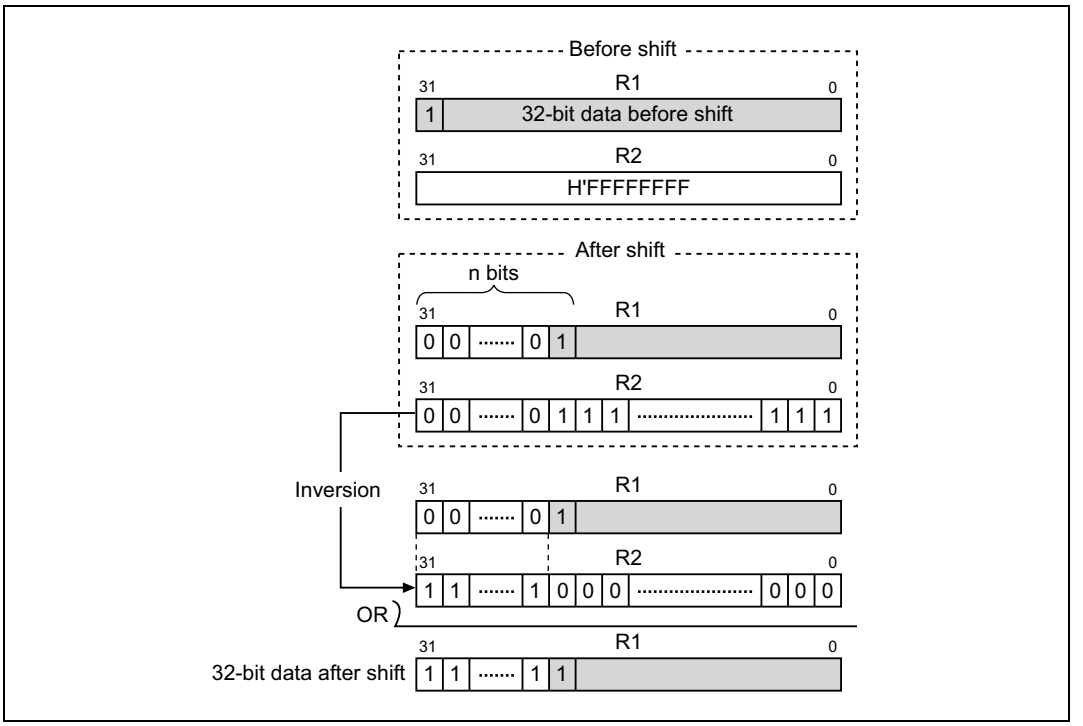
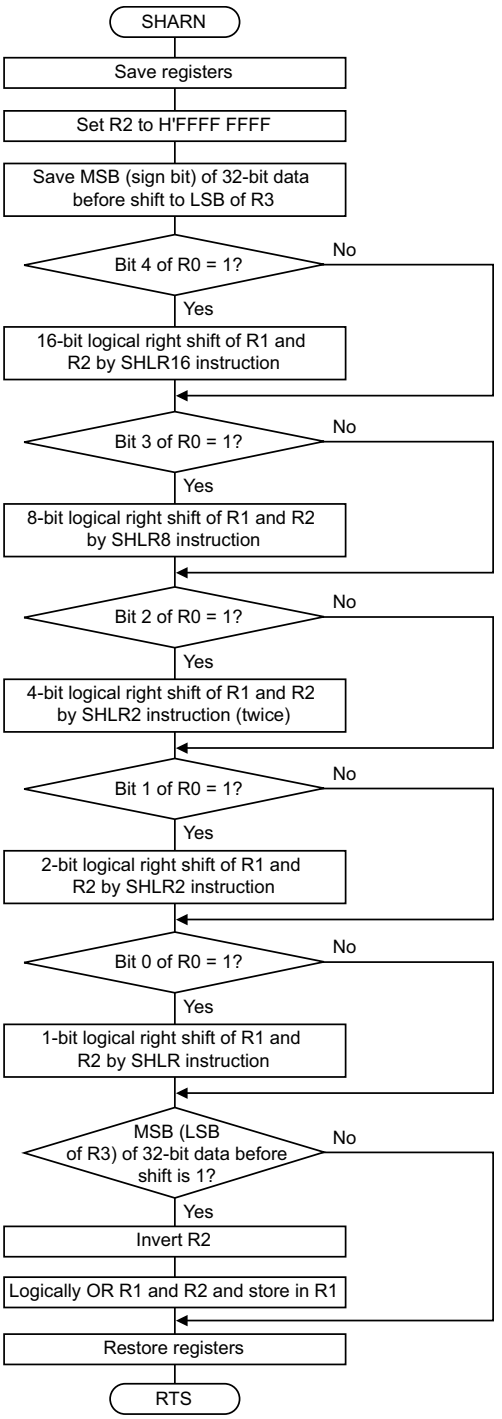


Figure 2 Multiple Bit Shift

7. Flowchart


SHARN
Save registers
Set R2 to H'FFFF FFFF
Save MSB (sign bit) of 32-bit data before shift to LSB of R3
Bit 4 of R0 = 1?
No
Yes
16-bit logical right shift of R1 and R2 by SHLR16 instruction
Bit 3 of R0 = 1?
No
Yes
8-bit logical right shift of R1 and R2 by SHLR8 instruction
Bit 2 of R0 = 1?
No
Yes
4-bit logical right shift of R1 and R2 by SHLR2 instruction (twice)
Bit 1 of R0 = 1?
No
Yes
2-bit logical right shift of R1 and R2 by SHLR2 instruction
Bit 0 of R0 = 1?
No
Yes
1-bit logical right shift of R1 and R2 by SHLR instruction
MSB (LSB of R3) of 32-bit data before shift is 1?
No
Yes
Invert R2
Logically OR R1 and R2 and store in R1
Restore registers
RTS

8. Program Listing

```
NAME:    n BITS SHIFT ARITHMETIC RIGHT (SHARN)
ENTRY:   R0 (NUMBER OF BIT SHIFTED)
         R1 (32 BIT DATA)
RETURNS: R1 (SHIFT RESULT)
  1                       1                                ;
  2                       2                                ;
  3                       3                                ;
  4                       4                                ;
  5                       5                                ;
  6                       6                                ;
  7                       7                                ;
  8                       8                                ;
  9                       9                                ;
 10                      10                                ;
 11                      11                                ;
 12 00001000             12   .SECTION A, CODE,LOCATE=H'1000
 13          00001000    13   SHARN .EQU      $              ; Entry point
 14 00001000 2F26        14           MOV.L   R2,@-R15       ; Escape register
 15 00001002 2F36        15           MOV.L   R3,@-R15       ;
 16 00001004             16   SHARN1                         ;
 17 00001004 3228        17           SUB     R2,R2          ; R2 ← H'FFFFFFFF
 18 00001006 6227        18           NOT     R2,R2          ;
 19 00001008             19   SHARN2                         ;
 20 00001008 4104        20           ROTL    R1             ; R3 ← MSB of 32 bit data
 21 0000100A 0329        21           MOVT    R3             ;
 22 0000100C 4105        22           ROTR    R1             ;
 23 0000100E             23   SHARN3                         ;
 24 0000100E C810        24           TST     #B'00010000,R0 ; Bit 4 = 1?
 25 00001010 8901        25           BT      SHARN4         ; No
 26 00001012 4129        26           SHLR16  R1             ; 16 bit shift logical right
 27 00001014 4229        27           SHLR16  R2             ;
 28 00001016             28   SHARN4                         ;
 29 00001016 C808        29           TST     #B'00001000,R0 ; Bit 3 = 1?
 30 00001018 8901        30           BT      SHARN5         ; No
 31 0000101A 4119        31           SHLR8   R1             ; 8 bit shift logical right
 32 0000101C 4219        32           SHLR8   R2             ;
 33 0000101E             33   SHARN5                         ;
 34 0000101E C804        34           TST     #B'00000100,R0 ; Bit 2 = 1?
 35 00001020 8903        35           BT      SHARN6         ; No
 36 00001022 4109        36           SHLR2   R1             ; 4 bit shift logical right
 37 00001024 4109        37           SHLR2   R1             ;
 38 00001026 4209        38           SHLR2   R2             ;
 39 00001028 4209        39           SHLR2   R2             ;
 40 0000102A             40   SHARN6                         ;
 41 0000102A C802        41           TST     #B'00000010,R0 ; Bit 1 = 1?
 42 0000102C 8901        42           BT      SHARN7         ; No
 43 0000102E 4109        43           SHLR2   R1             ; 2 bit shift logical right
 44 00001030 4209        44           SHLR2   R2             ;
 45 00001032             45   SHARN7
```

```
46 00001032 C801        46          TST     #B'00000001,R0  ; Bit 0 = 1?
47 00001034 8901        47          BT      SHARN8          ; No
48 00001036 4101        48          SHLR    R1              ; 1 bit shift logical right
49 00001038 4201        49          SHLR    R2              ;
50 0000103A             50  SHARN8                          ;
51 0000103A 6033        51          MOV     R3,R0           ;
52 0000103C C801        52          TST     #B'00000001;R0  ; MSB of 32 bit data = 1?
53 0000103E 8901        53          BT      SHARN_END       ; No
54 00001040 6227        54          NOT     R2,R2           ;
55 00001042 212B        55          OR      R2,R1           ;
56 00001044             56  SHARN_END                       ;
57 00001044 63F6        57          MOV.L   @R15+,R3        ; Return register
58 00001046 000B        58          RTS                     ;
59 00001048 62F6        59          MOV.L   @R15+,R2        ;
60                      60          .END
*****TOTAL ERRORS   0
*****TOTAL WARNINGS 0
```

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