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Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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SH7000 Series
64 Bit + 64 Bit = 64 Bit (Unsigned)

Label: ADDU64

Functions Used: ADDC Instruction

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1. Function

Add the augend (unsigned 64 bits) and addend (unsigned 64 bits), and determine the sum (unsigned 64 bits). At this time, whether or not any carry is generated is set in the T bit.

2. Arguments

<table>
<thead>
<tr>
<th>Description</th>
<th>Storage Location</th>
<th>Data Length (Bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Upper 32 bits of augend</td>
<td>R0</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower 32 bits of augend</td>
<td>R1</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Upper 32 bits of addend</td>
<td>R2</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower 32 bits of addend</td>
<td>R3</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Upper 32 bits of sum</td>
<td>R0</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower 32 bits of sum</td>
<td>R1</td>
<td>4</td>
</tr>
<tr>
<td>(unsigned 64 bits)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>With/without carry</td>
<td>T bit (SR)</td>
<td>4</td>
</tr>
<tr>
<td>(with: T = 1, without: T = 0)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 3. Internal Register Changes and Flag Changes

<table>
<thead>
<tr>
<th>Register</th>
<th>(Before Execution)</th>
<th>→</th>
<th>(After Execution)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>Upper 32 bits of augend</td>
<td>→</td>
<td>Upper 32 bits of sum</td>
</tr>
<tr>
<td>R1</td>
<td>Lower 32 bits of augend</td>
<td>→</td>
<td>Lower 32 bits of sum</td>
</tr>
<tr>
<td>R2</td>
<td>Upper 32 bits of addend</td>
<td>→</td>
<td>No change</td>
</tr>
<tr>
<td>R3</td>
<td>Lower 32 bits of addend</td>
<td>→</td>
<td>No change</td>
</tr>
<tr>
<td>R4</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R6</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R8</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R10</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R11</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R12</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R13</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td></td>
<td>→</td>
<td></td>
</tr>
<tr>
<td>R15</td>
<td></td>
<td>→</td>
<td>(SP)</td>
</tr>
</tbody>
</table>

T bit
- *: Change
- 0: Fixed 0
- 1: Fixed 1
- —: No change
4. Programming Specifications

<table>
<thead>
<tr>
<th>Program memory (bytes)</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data memory (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Stack (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Number of states</td>
<td>5</td>
</tr>
<tr>
<td>Reentrant</td>
<td>Yes</td>
</tr>
<tr>
<td>Relocation</td>
<td>Yes</td>
</tr>
<tr>
<td>Intermediate interrupt</td>
<td>Yes</td>
</tr>
</tbody>
</table>

5. Description

(1) Function

Details of the arguments are as follows.

R0: Set the upper 32 bits of the augend (unsigned 64 bits) as the input argument. Holds the upper 32 bits of the sum (unsigned 64 bits) as the output argument.

R1: Set the lower 32 bits of the augend (unsigned 64 bits) as the input argument. Holds the lower 32 bits of the sum (unsigned 64 bits) as the output argument.

R2: Set the upper 32 bits of the addend (unsigned 64 bits) as the input argument.

R3: Set the lower 32 bits of the addend (unsigned 64 bits) as the input argument.

T bit (SR): Indicates the presence or absence of a carry after execution of the software instruction ADDU64.
- T bit = 1: Indicates a carry was generated.
- T bit = 0: Indicates no carry was generated.

Figure 1 shows a software ADDU64 execution example.
(2) Usage Notes

Since the sum is set in R1 and R2, which contained the augend settings, the augend data is destroyed. If the value for the augend will be needed after the software ADDU64 instruction is executed, it should be saved beforehand.

(3) RAM Used

No RAM is used by the software ADDU64 instruction.

(4) Usage Example

After the augend and addend are set in input arguments, the software instruction ADDU64 is executed by a subroutine call.

```assembly
MOV.L DATA1,R0 .... Sets augend (upper 32 bits) in input argument
MOV.L DATA2,R1 .... Sets augend (lower 32 bits) in input argument
MOV.L DATA3,R2 .... Sets addend (upper 32 bits) in input argument
BSR ADDU64 .... Subroutine call to ADDU64
MOV.L DATA4,R3 .... Sets addend (lower 32 bits) in input argument
BT ERROR .... Branches to error-processing subroutine if carry occurs
```

```
DATA1 .data.l H'FFFFFFFF
DATA2 .data.l H'FFFFFFFF
DATA3 .data.l H'10000000
DATA4 .data.l H'10000000
```

Figure 1  Software ADDU64 Execution Example
(5) Operating Principle

As shown in figure 2, the add with carry instruction (ADDC) is used repeatedly to perform addition in 32-bit units, starting from the LSB.

![Figure 2 Unsigned Addition](image)

6. Flowchart

```
ADDU64

Clear T bit

Add lower 32 bits of augend and addend using ADDC instruction

Add upper 32 bits of augend and addend using ADDC instruction

RTS
```
7. Program Listing

1 1 ;***************************************************************
2 2 ;*
3 3 ;* NAME : 64 BIT UNSIGNED BINARY ADDITION (ADDU64) *
4 4 ;*
5 5 ;***************************************************************
6 6 ;*
7 7 ;* ENTRY : R0 (UPPER 32 BIT AUGEND) *
8 8 ;* R1 (LOWER 32 BIT AUGEND) *
9 9 ;* R2 (UPPER 32 BIT ADDEND) *
10 10 ;* R3 (LOWER 32 BIT ADDEND) *
11 11 ;* RETURNS : R0 (UPPER 32 BIT SUM) *
12 12 ;* R1 (LOWER 32 BIT SUM) *
13 13 ;* T BIT (CARRY -> TRUE; T=1, FALSE; T=0) *
14 14 ;*
15 15 ;***************************************************************
16 16 .SECTION A,CODE,LOCATE=H'1000
17 17 ADDU64 .EQU $ ; Entry point
18 18 CLRT ; Clear T bit
19 19 ADDC R3,R1 ; Lower 32 bit augend + Lower 32 bit addend
20 20 RTS ;
21 21 ADDC R2,R0 ; Upper 32 bit augend + Upper 32 bit addend
22 22 .END

*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
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