SH2A Family, RX Family

Signal Processing Library

Introduction

Renesas developed the Signal Processing Library or SPL for a class of microprocessors and microcontrollers which have floating-point units. The SPL is a collection of primitive DSP functions such as FIR, IIR and FFT. These libraries are offered on a variety of Renesas CPU families, tool chains and OS configurations. These functions are fine-tuned so as to spare the end-users of the intrinsic details of these CPU and FPU architectures, assembly language details, pipeline conflicts that are unique to each of these processors and devices. Using these fine-tuned optimized libraries, signal processing application developers can better concentrate on their system design.

Target Device

SH2A Family (SH7264, SH7216)

RX Family (RX62N)

Contents

1. Installation

Signal Processing Library (SPL) Product Version 2.0.0 for SH2A and RX processors is distributed as an install shield package for Microsoft Windows 2000/XP host systems.

The SPL package includes the following items:

- o SPL Library for the SH2A processor (SPLib_sh2afpu.lib)
- o SPL Library for the RX processor (SPLib_rx600_sl.lib)
- o "C" Header file (rtadsplib.h)
- o Documentation for the SPL APIs (reu11b0002_splibum.pdf)
- o Documentation for the Sample SH2A HEW workspace (reu12b0001_sh2asplibum.pdf)
- o Documentation for the Sample RX HEW workspace (reu12b0002_rx600splibum.pdf)
- o Sample HEW workspace for the SH7264 Denali RSK
- o Sample HEW workspace for the SH7216 reference platform
- o Sample HEW workspace for the RX62N reference platform (R0K5562N0C010BR)
- o Click-through Licesing Agreement

To install SPL for the SH2A and RX processors run the setup.exe that came with the distribution. This will install the signal processing library to the "C:\Renesas" folder on the user host system.

2. License

The SPL End-User License Agreement combines Evaluation and Mass Production License. By going through the click-through process, the user from all regions and countries can utilize the SPL.

3. Usage and system diagram

A typical user system block diagram using the signal processing library is depicted in the following figure.
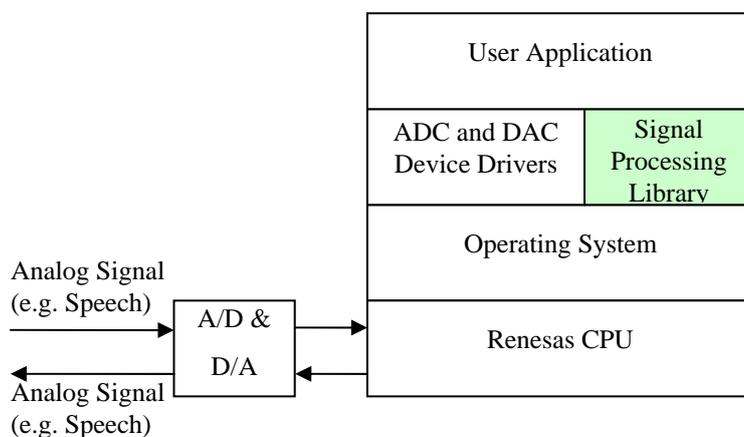

Figure 1. User System Block Diagram

4. Target Devices and Configurations

The library may be used for the following target configurations.

Item	Target HW	Compiler	Compiler Version	Endian	OS	Floating-Point Precision
1	SH2A w/ FP	SHC	9.03.00	Big	No OS (Bare Metal Hardware)	Single

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2		SHC	9.03.00	Big	uCOS	Single
3		SHC	9.03.00	Big	ThreadX	Single
4		SHC	9.03.00	Big	uiTRON	Single
5	RX600	Renesas RX C	1.00.00.001	Big	No RTOS	Single

5. Signal Processing Library Performance for SH2A-FPU and RX Devices

The following table shows the signal processing library performance on two of the reference platforms based on the SH2A-FPU device and the RX device.

CPU (Reference Platform)	DSP Function	Parameters and Data Size	Performance (CPU Cycles)
SH7264 RSK	— rta_cfft1d	• 64 Samples	• 3258
	rta_rfft1d	64 Samples	5125
	rta_dsplib_fir	100 Samples, 64 Coefficients	8669
	rta_dsplib_iirBiquad	100 samples, 5 Stages	7126
SH7216 RSK+	— rta_cfft1d	• 64 Samples	• 3892
—	rta_rfft1d	64 Samples	5875
—	rta_dsplib_fir	100 Samples, 64 Coefficients	3585
—	rta_dsplib_iirBiquad	100 samples, 5 Stages	9582
RX62N RSK	— rta_cfft1d	• 64 Samples	• 7954
—	rta_rfft1d	128 Samples	12199
—	rta_dsplib_fir	100 Samples, 64 Coefficients	55122
—	rta_dsplib_iirBiquad	100 samples, 5 Stages	19841

Website

Renesas Electronics Website
   http://www.renesas.com/

Inquiries
   http://www.renesas.com/inquiry

Support

A form at www.renesas.com will route the support questions to the maintainer of the SPL and regional strategists. The support questions are responded in the order received. If you need immediate assistance please contact Renesas sales for priority support.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.17.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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